11.4 Towards Terahertz Operation of CMOS

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The electromagnetic spectrum between 300GHz and 3THz is broadly referred as terahertz [1]. The utility of this portion of spectrum for detection of chemicals and bio agents, for imaging of concealed weapons, cancer cells and manufacturing defects [1, 2], and for studying chemical species using electron paramagnetic resonance, as well as, in short range radars and secured high data rate communications has been demonstrated. However, high cost and low level of integration for III-V devices needed for the systems have limited their wide use. The improvements in the high frequency capability of CMOS have made it possible to consider CMOS as a lower cost alternative for realizing the systems that can greatly expand the use of this spectrum range.

A conceptual diagram of a THz spectrometer for chemical detection shown in Fig. 11.4.1 consists of a transmitter with a tunable signal generator and an antenna, and a receiver with an antenna, a detector or a mixer followed by a low noise amplifier/filter. The key components are signal generator, diode detector or mixer, and antennas. This paper reports a new polysilicon gate separated Schottky barrier diode structure (PGS SBD) which enables operation of receivers at frequencies higher than that limited by the transistors; examples of the building blocks with on-chip antennas operating at 100 to 400GHz, which suggest the use of CMOS in THz applications; and a potential path to realize 1THz operation in CMOS.

Figure 11.4.2 shows the projected requirements for NMOS unity current gain and power gain frequencies (f_T and f_{max}) from the 2006 International Road Map for Semiconductors (ITRS). It also shows the measured f_T and f_{max} in the literature. Despite the concern for the slow down in ITRS, the industry has kept up with the road map to date. The highest f_T and f_{max} of bulk transistors are 360 and 420GHz, while the highest f_T of SOI transistors is 485GHz. If this can be kept up for another three years, NMOS transistors with f_T and f_{max} close to 600GHz will be available. With such devices, amplifiers tuned at 300GHz or at the lower limit of the THz region will be possible.

Figure 11.4.3 shows a cross section of new PGS SBD's fabricated in logic CMOS without any process modifications that can increase the circuit operating frequency beyond that limited by the transistors. The cathode and anode are separated by a polysilicon gate layer. The measured cut-off frequency (f_T) at the 130nm generation is ~2THz. The f_T of this diode unlike that of the shallow trench separated (STS) SBD's [3] also in Fig. 11.4.3 should scale better with technology scaling due to the elimination of the n-well region below the Schottky contact surrounded by an STI ring. Such diodes will enable frequency multipliers, detectors and mixers operating at ~600GHz.

A 250GHz modulated signal generator with an on-chip patch antenna is demonstrated in a 90nm logic CMOS technology with 9 copper layers and a pad layer (Fig. 11.4.4). Its maximum measured radiated power at 250GHz is -32dBm (Fig. 11.4.6). The spectrum is measured using a Bruker 113V Fourier Transform Infrared Spectroscopy System, while the power is measured with a silicon bolometer. The 10 to 30MHz square wave modulation signal is generated by a ring oscillator using differential inverters with programmable delays. The ring oscillator output turns on and off the PMOS current source of a push-push VCO with NMOS cross-coupled topology [4] shown in Fig. 11.4.4 to amplitude/frequency modulate the output. At the virtual ground nodes, the fundamental signal is attenuated, and the 2nd harmonic is extracted. Matching networks using coplanar waveguides with a ground plane (metal 1 and metal 2 shunted together) provide high impedance at the 2nd harmonic frequency. The pad layer is used for the signal line. The extracted 2nd harmonic is radiated through a patch antenna formed using a pad layer with a size of 330 x 315μm^2. The ground plane once again is formed using the metal 1 and 2 layers. The dielectric thickness from the ground plane to patch is ~7μm. The simulated antenna efficiency is 32% at 250GHz. A die micrograph is shown at the bottom of Fig. 11.4.7.

As a step toward realizing diode circuits operating in the THz regime, a 250GHz Schottky detector is also fabricated using 90nm CMOS (Fig. 11.4.5 and left side of Fig. 11.4.7). The diode is formed with 14 0.28 x 0.28μm^2 cells of PGS SBD's. The detector consists of an on-chip patch antenna, a matching circuit, a Schottky diode, a low-pass filter, and an amplifier. The diode is connected in shunt to reduce the impact of parasitics of the n-well. The diode is forward biased through a 2.5kΩ (R_1) resistor. TL_1, TL_2 and C_1 comprise a matching circuit. C_1 and C_2 provide isolation between RF and baseband signals. The antenna and transmission lines are similar to that of the 250GHz signal generator. The simulated performance parameters are listed in Fig. 11.4.6.

STS SBD's are also used to demonstrate a 110 to 140GHz frequency doubler in 130nm logic CMOS with measured output power of -1.5dBm and conversion efficiency of ~10% at 125GHz (Fig. 11.4.6). The diode has a large n^+ cathode contact area for lower resistance [3]. This increases the n-well to substrate capacitance. To mitigate the effects of this, a balanced topology with two shunt diodes [5] (32 × 0.64 × 0.64μm^2) with grounded n-wells is utilized. The diode size is chosen to optimize the grading coefficient, m_j (0.49) and cut-off frequency (680GHz) for lower conversion loss. The matching and filtering networks are formed with 50 and 72Ω coplanar waveguides with a ground plane. Quarter wave open stubs at input and output are used to attenuate the second order harmonic and fundamental signals (center of Fig. 11.4.7). The diode is reverse biased for higher efficiency.

Combining the recent 410GHz push-push oscillator result [4] with frequency quadrupling [6] and second-harmonic odd mode coupling for quadrature generation [7], an 800GHz phase-locked loop (PLL) is being developed. The 410GHz oscillator [4] was fabricated using low leakage transistors in a 45nm CMOS technology (top right side of Fig. 11.4.7). The schematic is the same as the oscillator core in Fig. 11.4.4. The low radiated power of -49dBm (Fig. 11.4.6) is mostly due to the losses of thin metal and dielectric layers. If the top metal layer thickness and the dielectric layer thickness to ground are increased to ~3 and 6μm, the resulting increases for Q's of inductors and transmission lines, and the increase of antenna efficiency are expected to raise the power to ~ -20dBm. Using injection locked frequency dividers that divide the 200GHz fundamental signal to 50GHz followed by static dividers in a PLL [8], it should be possible to lock the frequency-doubled 400GHz signal. The measurements, simulations, and projection indicate that CMOS should be able to handle THz applications, and 1THz operation of a CMOS circuit will be possible within the next few years.

Acknowledgements:
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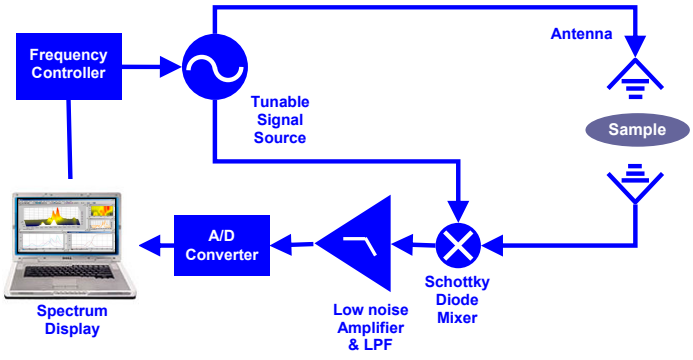


Figure 11.4.1: Conceptual diagram of THz spectrometer.

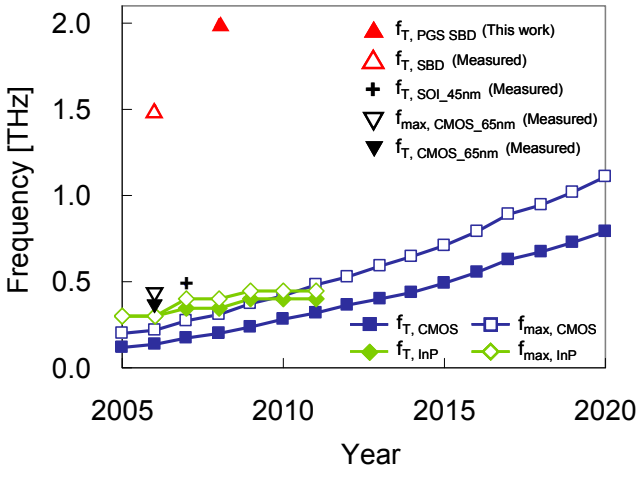
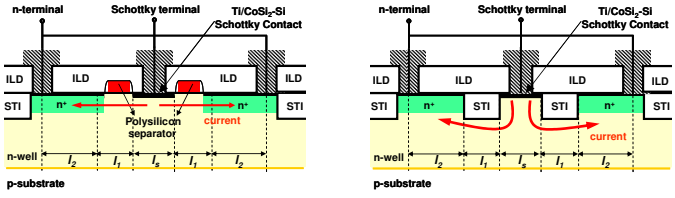


Figure 11.4.2: High frequency capabilities of NMOS transistors and PGS SBD's.



Polysilicon gate separated Schottky barrier diode.

Shallow trench separated Schottky barrier diode.

Figure 11.4.3: PGS and STS SBD's.

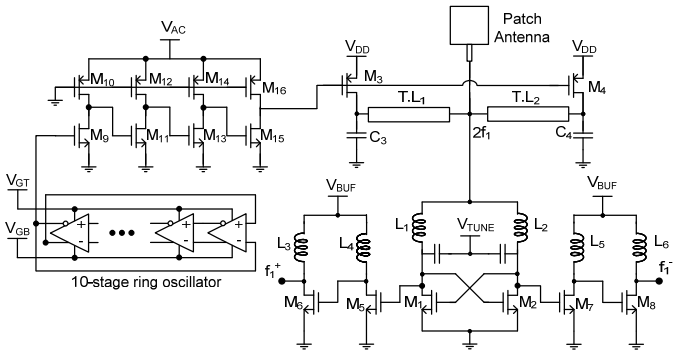


Figure 11.4.4: Schematic of 250GHz modulated signal generator.

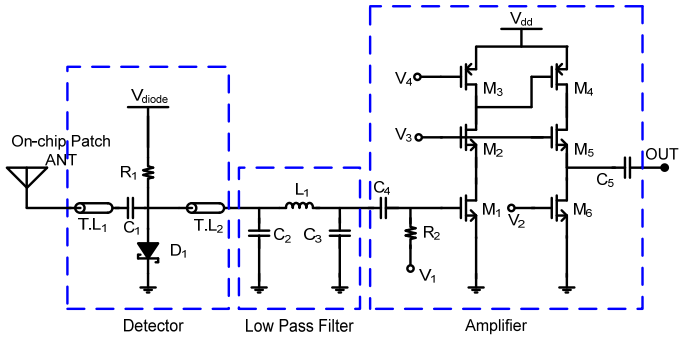


Figure 11.4.5: Schematic of 250GHz diode detector.

	Freq. Doubler (Meas.)	250GHz Diode Detector (Simulated)		250GHz Mod. Signal Generator (Meas.)	410GHz Oscillator (Meas.)
Topology	Shunt type	Shunt type	Topology	Push-Push	Push-Push
Nonlinear device	STS SBD	PGS SBD	V_{DD}	1.6 V	1.5 V
Diode cutoff frequency	~0.7THz		Current	13 mA	11 mA
Diode size	38 x 0.64 x 0.64 μm²	16 x 0.28 x 0.28 μm²	Power consumption	20.8 mW	16.5 mW
$\|S_{11}\|$ less than -10 dB	61 ~ 66GHz		Tuning range	4GHz	3GHz
Output frequency	110 ~ 140GHz	1-300MHz	Antenna efficiency (Simulated)	32 %	22 %
Bias voltage	-2 V		Output frequency	250.4GHz	410GHz
Minimum conversion loss	10 dB @ f_{out}=125GHz		Modulation frequency	10-30MHz	
Maximum output power	-1.5 dBm @ f_{out}=125GHz, P_{in} = 8.5 dBm		Output power	-32 dBm	-49 dBm
Chip size (mm²)	1.1 x 0.7	1.1 x 0.5	Chip size (mm²)	1.1 x 0.67	0.39 x 0.64
Technology	130nm CMOS	90nm CMOS	Technology	90nm CMOS	45nm CMOS

Figure 11.4.6: Performance summary.

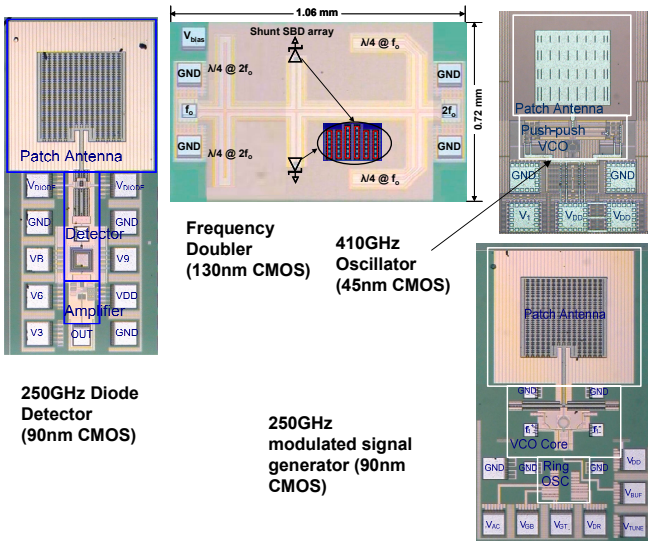


Figure 11.4.7: Die micrographs.

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