Multi-Level Amplitude Modulation of a 16.8-GHz Class-E Power Amplifier With Negative Resistance Enhanced Power Gain for 400-Mbps Data Transmission

Hsin-Ta Wu, Ruonan Han, Wuttichai Lerdsitsomboon, Changhua Cao, and Kenneth K. O

***Abstract*—Multi-level modulation of a 16.8-GHz class-E power amplifier with negative resistance enhanced power gain is demonstrated in a 130-nm CMOS process. The circuit achieves power gain of ∼30 dB, and power-added efficiency (PAE) of 16% for the highest output power level of 6.8 dBm. The average efficiency for a random data pattern is ∼8%. The circuit also exhibits 10-dBm saturated output power and ∼22% maximum PAE. By realigning the highest output power level to the 10-dBm saturated output power, the efficiency can be improved. For a random data pattern, this PA should achieve ∼2X higher efficiency than Class A PAs. The circuit supports seven amplitude levels for 400 Megabits per second (Mbps) data transmission. The multi-level output signal levels follow a square-root relation. The circuit including an address decoder occupies ∼ 1.4 mm^2.**

***Index Terms*—Class-E, CMOS, multi-level modulation, power amplifiers.**

I. Introduction

HYBRID electric vehicles (HEVs) with ∼2 times higher fuel efficiency are starting to be widely utilized [1]. Engine controller boards in HEVs have a high voltage (hundreds of volts) motor driver section (M1 and M2 in Fig. 1) and low voltage (less than 10 V) control section (D1 in Fig. 1). The low voltage section generates pulsewidth modulated signals for motor control and delivers them to the high voltage section. The floating potential of signal return path of high voltage/motor drive section can differ by several hundreds of volts from that for the low voltage section. Because of this, the signals are interfaced between the two sections using photo-couplers that isolate the return paths. The photo-couplers can support data transmission rate of ∼1 Mbps.

Wireless interconnection using two separate transceiver integrated circuits can also operate in the presence of large potential difference between the return paths. It can support the new higher data transmission rate target of 50-Mbps per channel.

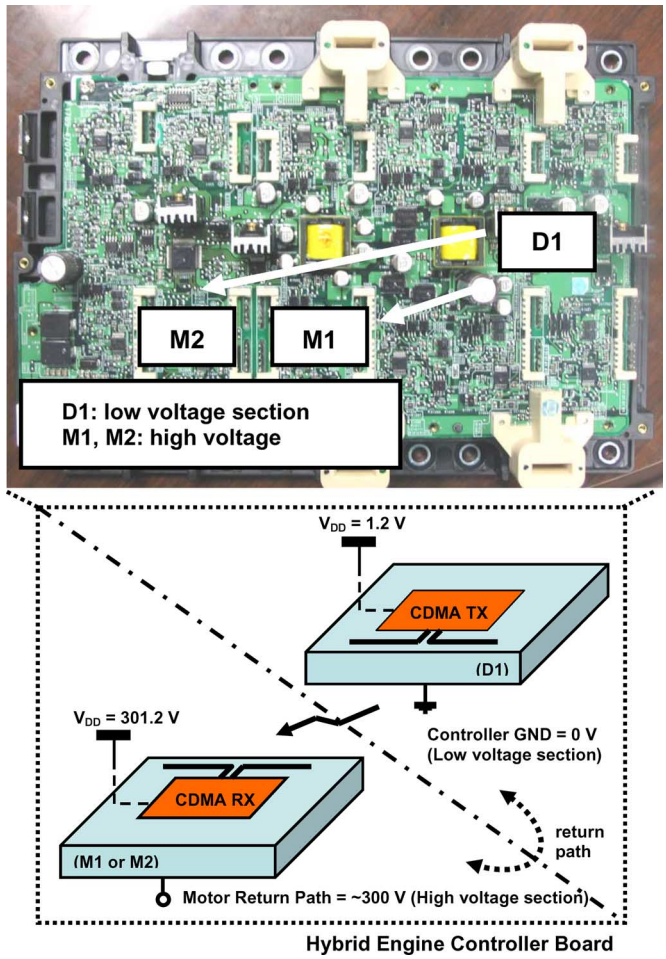

Fig. 1. Hybrid engine controller board including a high voltage motor driver section and a low voltage control section.

On-chip antennas are integrated with the transmitter (TX) and receiver (RX) to accomplish the wireless communications between the controller and motor sections, as shown in Fig. 1. Expected transmission range is ∼15 cm. The lower die cost and elimination of wire traces on the PC board should also reduce cost. Because the system is placed in a metallic enclosure, the spectrum can be utilized free from the restrictions of government regulations. Code division multiple access (CDMA) is chosen for transmission from the low voltage section to high

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TABLE I
COMPARISONS OF POWER AMPLIFIERS OPERATING NEAR 20 GHz

	Freq.	Technology	Classification	V_{DD}	Small Signal Gain	P_{out}	PAE
[2]	18 GHz	0.13-μm CMOS	Class E	1.5 V	> 30dB	10.9 dBm	23.5 %
[2]	20 GHz	0.13-μm CMOS	Class E	1.5 V	26 dB	10.2 dBm	20.5 %
[3]	17 GHz	0.13-μm CMOS	Class A	1.5 V	11 dB	5 dBm ($@OP_{1dB}$)	2.4% ($@OP_{1dB}$)
[4]	17 GHz	0.13-μm CMOS	Class B	1.5 V	14.5 dB	17.1 dBm	9.3 %
[5]	24 GHz	0.18-μm CMOS	N/A	2.8 V	7 dB	14.5 dBm	5~6 %
This work	16.8 GHz	0.13-μm CMOS	Class E	1.5 V	~ 30 dB	10 dBm	< 22 %

voltage section to mitigate the effects of multi-path rich environment in the hybrid engine controller board and to simplify the transmitter design. The receiver at motor side amplitude detects and decodes the CDMA signal.

A multi-level (seven) power amplifier (PA) is a key block for implementing the CDMA transmitter. This PA takes constant power 16.8-GHz local oscillator signal as the input and generates modulated output. Since a form of multiple level amplitude shift keying (ASK) is used for CDMA, an obvious topology choice for a PA is a linear type. Instead, this paper reports use of a nonlinear class-E PA with negative resistance enhanced output power which is typically used for constant envelope modulation systems for improved power efficiency [2]–[5] (Table I). The PA efficiency of this work is comparable to PAs operating at similar frequencies. Because of the high data rate (400 Mbps), supply modulation could not be used and weighted attenuator switching is selected for level control. The class-E PA operates at 16.8 GHz and fabricated in a 130-nm CMOS process.

II. CIRCUIT DESIGN

In this section, design considerations are discussed. In Section II-A, methods for implementing the multi-levels are described. The digital control scheme is described in II-B. The design challenges and solutions for improving the switching performance are discussed in Section II-C. Finally, issues for controlling the self oscillation resulting from the use of negative resistance enhanced power gain are presented in Section II-D.

A. Multiple Level Implementation

There are several ways to realize multi-level amplitude modulation at the PA output. One is to modulate the supply voltage to control output power of PA [6], [7]. The PA can be linear or nonlinear [8]–[11]. Supply modulation requires a dc-dc converter to implement a dynamic voltage supply. The converter significantly increases the chip area. The required chip rate of 400 Mchips/sec for the wireless interconnect system instead of hundreds of kHz or 10's of MHz for cellular applications makes use of a supply modulated power amplifier particularly difficult. It is also sensitive to supply variations and requires a feedback loop for tracking and adjusting the PA envelope.

The second way for realizing multi-level amplitude modulation is to use a current-steering technique [12] to modulate the gate bias of pre-drivers. A similar idea was used to lower quiescent current at low output power to improve PA efficiency (adaptive bias control) [10], [11]. However, based on simulations, fall times are long and precise gain control is difficult by adjusting only gate bias without closed-loop control. The closed-loop control will complicate the design. Adaptive closed-loop bias control for WCDMA applications [13], [14] uses a power sensor to precisely control the gate bias of PA stage. Use of this is expected to be challenging for the desired data rate of 400 Mbps. A simpler approach is required for a PA operating at the desired carrier frequency of 16.8 GHz, and to achieve sufficient response time.

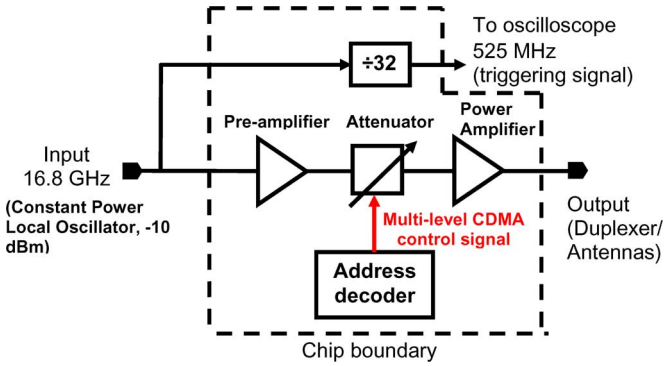

Fig. 2. Block diagram of multiple level amplitude modulated power amplifier.

Another approach to multi-level modulate a PA is to incorporate switchable attenuators. As shown in Fig. 2, the attenuators can be placed at the signal path to adjust the signal level into the PA stage [15], [16] as well as the negative resistance seen by the PA. Each level control is accomplished by turning on/off appropriate combinations of attenuators, which can modulate the signal swing at the gate of the fourth pre-driver and implement the required multi-level control signals. The truth table for the coding scheme is shown in Table II. Consequently, the multi-level signals for 400 Mbps data can be formed at the gate of PA stage as well as its output. Since the switched capacitances of attenuators are smaller, the PA can readily support the modulation for the required data rate of 400 Mbps.

Fig. 3(a) shows the schematic of single-ended CDMA PA. It includes four pre-drivers and a PA stage. The first three pre-drivers are implemented using cascode amplifiers and the fourth pre-driver is a common-source amplifier. The pre-drivers are designed to achieve high voltage gain, while the last PA stage

TABLE II
TRUTH TABLE OF ADDITIVE/SUBTRACTIVE CODING SCHEME, AND THE RATIO BETWEEN LEVELS AT TX SIDE AND AFTER RX DETECTION

"additive/subtractive"	att_0	att_1	att_2	att_3	att_4	att_5	att_6
Level 6	0	0	0	0	0	0	1
Level 5	0	0	0	0	0	1	1
Level 4	0	0	0	0	1	1	1
Level 3	0	0	0	1	1	1	1
Level 2	0	0	1	1	1	1	1
Level 1	0	1	1	1	1	1	1
Level 0	1	1	1	1	1	1	1

	Ideal ratio at TX side	After RX detection
Level 2 / Level 1	$\sqrt{2}$	2
Level 3 / Level 1	$\sqrt{3}$	3
Level 4 / Level 1	$\sqrt{4}$	4
Level 5 / Level 1	$\sqrt{5}$	5
Level 6 / Level 1	$\sqrt{6}$	6

is designed for maximizing output power and efficiency. The common-source fourth pre-driver allows larger output voltage swing.

To minimize power consumption and increase efficiency, the values of output matching components [C_1, C_2, and L_1 in Fig. 3(a)] are chosen such that the drain current of M_8 should be low when V_x (voltage across the drain and source of M_8) is high [17]. The simulated threshold voltage of transistor in the 130-nm process is 0.38 V. The gate bias of PA stage is set to 0.6 V. Due to the large voltage swing at the gate of M_8, the transistor operates in mostly the switching mode for levels 3–6. As discussed, the attenuator setting at the gate of pre-driver is used to set the signal level at the gate of the fourth pre-driver. Varying the over drive changes the duration in switching mode, and output level.

Fig. 3(b) shows a simulated output waveform. As expected, the voltage (V_{ds}) and current (I_D) waveforms at the drain of M_8 are out of phase [shown in Fig. 3(c)], which reduces the power dissipation and improves the efficiency compared to using a PA with conduction angle of 360 degree. Assuming equal probability for output levels (1–6), the simulated average PAE of class E PA is $\sim$14% instead of $\sim$6.6% for a class A PA. The PAE calculation includes all the pre-driver stages power consumption. Regardless of the design for output matching network to make V_{ds} and I_D of M_8 to be out of phase, the multi-level PA does not operate in the pure Class-E mode for levels 3 to 6. This is mainly due to the difficulty for providing a perfect square waveform at the gate of PA stage at the required high operating frequencies. The maximum V_{ds} can only achieve $\sim$2X V_{DD} [shown in Fig. 3(c)] instead of the ideal value of 3.56X V_{DD}.

As shown in Fig. 3(a), there are seven attenuators with varying transistor sizes to set the seven PA output levels. The gate node of each attenuator is connected to a decoder output. There are six attenuators connected at the gate of the fourth pre-driver stage. There is also an attenuator connected at the gate of second stage. The decoder provides control pulses to turn on or off appropriate combinations of attenuators. Since the signal swing and transistor sizes at the second stage is smaller than that at the fourth stage, the attenuator size for level 0 can be made smaller by placing at an earlier pre-amplifier stage. This decreases the transistor size needed to control level 0, which reduces the loading in the signal path and drivability requirement for the decoder. The attenuators are simple nMOS switches. For better level tracking with process variation, the switches are formed using a varying number of parallel connected unit cells $(0.25\ \mu m/0.12\ \mu m)$. Level 6 requires a unit cell attenuator.

B. Digital Control Scheme

A thermometer decoding (additive/subtractive coding scheme) is selected over simple decoding scheme in which one attenuator is turned on while another one is turned off to reduce glitches during transitions and to suppress the self oscillation. The truth table is shown in Table II. For the additive/subtractive coding scheme, all the attenuators are turned on to set level 0. On the other hand, for level 6, only one attenuator is turned on. The ratios of numbers of turned on switches between level N and level 1 (N = 2, 3, 4, 5 6) implement the square-root function (Table II) to accommodate the squaring in a receiver using a diode detector [18], [19]. Consequently, receiver outputs with a roughly constant voltage step are generated. Lastly, for post fabrication digital calibration of the level ratios (att_1 to att_5), five small switches consisting of a varying number of parallel connected unit cells $(0.25\ \mu m/0.12\ \mu m)$ with AND gates are added as shown in Fig. 4. D-flip-flops added at the output of binary thermometer decoder help synchronize decoder outputs.

C. Rise and Fall Times

Another design requirement is controlling the rise and fall times of output envelope. The target for rise and fall times of an envelope is $\sim$10% or $\sim$250 ps. These transition times are determined by the *RC* time constants associated with switching the attenuators at the gates for second and fourth stages. Since the additive/subtractive coding scheme has been chosen, the following discussion is limited for this coding case.

For this coding scheme, levels are changed by turning on additional necessary attenuators or turning off some necessary attenuators instead of turning all off and turning on a new set. For example, for the level 4 to level 6 transition, the extra switches needed to be turned off are switches 4 and 5 only as can be seen

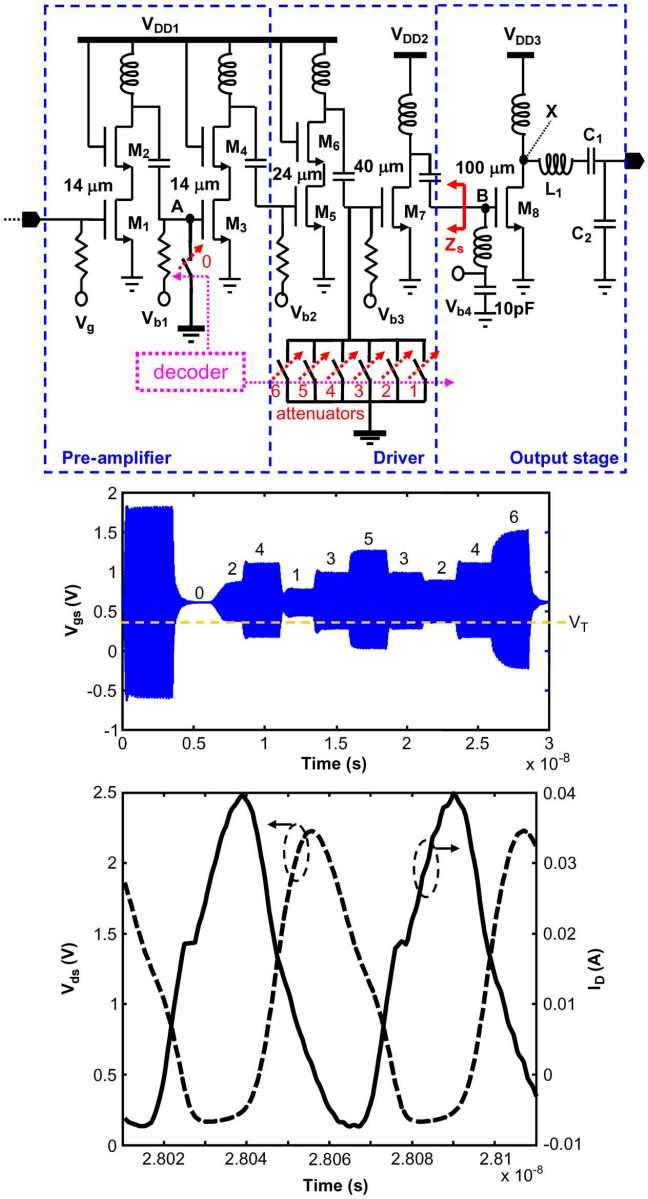

Fig. 3. (a) Schematic of a single-ended five-stage class-E CMOS power amplifier. (b) Simulated V_{gs} waveform at the gate of PA transistor [node B in Fig. 3(a)]. (c) Simulated waveforms of V_{ds} and I_D of the PA transistor [node X in Fig. 3(a)].

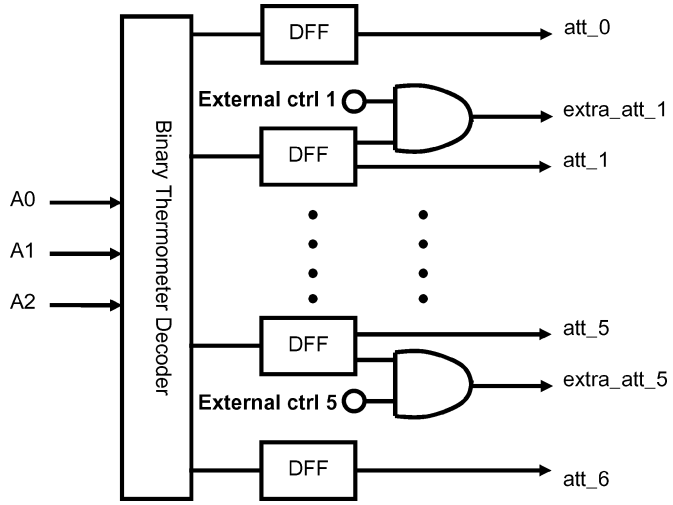

Fig. 4. Decoder block diagram with external bias control for AND gates to turn on extra attenuators for post fabrication digital calibration.

TABLE III
SWITCH SIZES FOR THE ADDITIVE/SUBTRACTIVE CODING SCHEMES (THE SWITCH (ATTENUATOR) SIZES ARE FOR THE SINGLE-ENDED PA.)

additive/subtractive	Switch size
att_6	(0.25 µm / 120 nm) x 1 = 0.25-µm width
att_5	(0.25 µm / 120 nm) x 3 = 0.75-µm width
att_4	(0.25 µm / 120 nm) x 5 = 1.25-µm width
att_3	(0.25 µm / 120 nm) x 6 = 1.5-µm width
att_2	(0.25 µm / 120 nm) x 6 = 1.5-µm width
att_1	(0.25 µm / 120 nm) x 9 = 2.25-µm width
att_0	(0.25 µm / 120 nm) x 36 = 9-µm width

from Table II. The sizes of switches (attenuators) for the additive/subtractive coding scheme are shown in Table III. That means the capacitance required to be switched is mainly from switches 4 and 5. The smaller switched capacitance leads to shorter rise and fall times. The switch sizes are chosen to be as small as possible to keep reducing rise and fall times. Meanwhile, it has to be sufficiently large to provide the necessary attenuation and implement the square-root function.

Presently, longer transition times are the rise times for level 0 to level N (N = 1–6) which are largely determined by the gate bias resistor at the second pre-driver stage. The gate bias resistor is 5 kΩ. This value is chosen to prevent the loading of 16.8-GHz carrier signal. However, this increases the *RC* time constant of the equivalent network at the gate of second pre-driver, thus the rise and fall times. Varying the attenuator settings change the equivalent *RC* network as shown in Fig. 5. When the switch is OFF, the parasitic capacitance of switch added to node A is $(C_{db} + C_{gd})$. When the switch is ON, the parasitic capacitance is still around $(C_{db} + C_{gd})$. However, the on resistance of the switch is much smaller compared to the 5-kΩ bias resistor. Therefore, the equivalent resistance (R_{eq}) is dominated by the on resistance of attenuator switch. The total equivalent capacitance at node A is relatively constant, which is roughly the sum of C_{db} and C_{gd} of attenuator, C_{gg} of the pre-driver, and other parasitic capacitance (Fig. 5). These are lumped and represented as C_{eq}. During a transition from level 0 to level N (N = 1–6), the equivalent resistance changes from several tens of ohms to 5 kΩ. The rise time is $\sim 2R_{eq}C_{eq}$ and the largest when the attenuator is off.

D. Self Oscillation Control

As mentioned earlier, the bias of class-E PA (V_{b4}) is applied through an inductor. The inductor along with C_{gd} of the last PA stage can generate negative resistance, which increases the PA gain and efficiency [2], [20], [21]. However, a concern is the self oscillation at the last PA stage that can increase the level zero output power. The self oscillation must be properly controlled to set the required lower level signals. Fig. 6 shows the small-signal model of the last PA stage [2]. Turning on and off of varying combinations of attenuators at the input of the fourth pre-driver stage modifies the impedance looking back toward the drain of stage (Z_s in Fig. 3(a)). Use of a common-

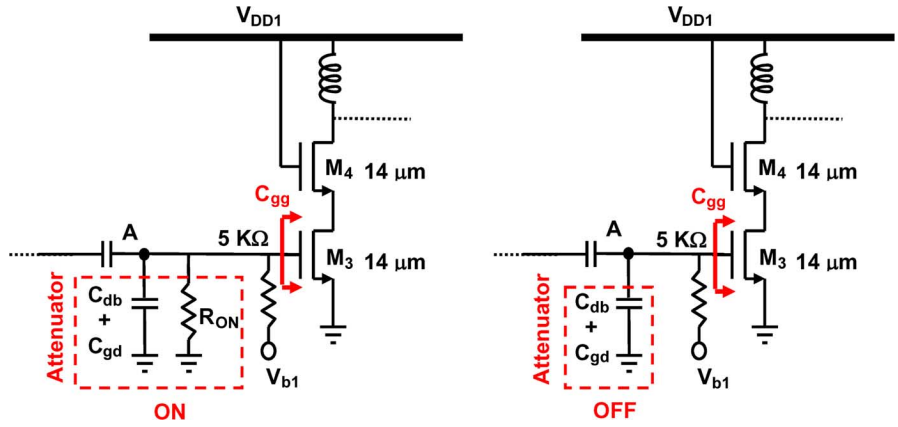

Fig. 5. Lumped circuit models with the attenuator switched ON and OFF. The rise and fall times depend on the *RC* time constant of equivalent network at the gate node of second pre-driver [Node A in Fig. 3(a)].

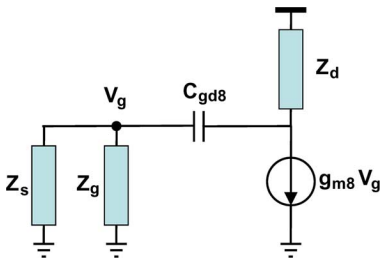

Fig. 6. Small-signal model of the last PA stage (common-source amplifier). Z_s is the impedance looking back toward the fourth pre-driver stage. Z_g is the impedance of the bias inductor. Z_d is the drain load inductor.

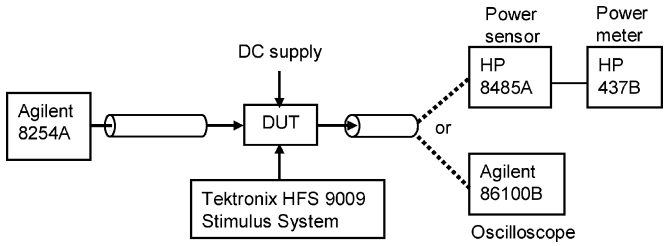

Fig. 7. PA measurement setups for frequency and time domain characterization.

source fourth pre-driver stage because of relatively high S_{12}, increases the impact of input termination to the output impedance of stage, Z_s.

The open loop gain of PA stage is

$$T(s) = -g_{m8}\left\{Z_d // \left[(Z_g // Z_s) + \frac{1}{sC_{gd8}}\right]\right\} \bullet \frac{(Z_g // Z_s)}{(Z_g // Z_s) + \frac{1}{sC_{gd8}}} \quad (1)$$

$$Z_s \propto \frac{1}{g_{m7}}\left(1 + \frac{1}{sC_{gd7} \bullet (Z_{att} // Z_{gs7})}\right) \quad (2)$$

Z_{att} represents the impedance associated with the attenuators at the gate of the fourth pre-driver stage. Z_{gs7}, C_{gd7} and g_{m7} are the impedance of gate to source capacitance, gate to drain capacitance and transconductance for transistor M7, respectively. When attenuators are turned on Z_{att} decreases and the real part of Z_s increases. This in turn lowers the open loop gain, $|T(s)|$ and modifies the phase. The oscillation starts when the loop gain is greater than 1 and the phase is equal to 360 degree [2]. When all the attenuators are turned on to set level 0, the oscillation is suppressed.

The circuit is near this oscillation condition without any 16.8-GHz RF sinusoidal input and all the attenuators turned off. The circuit oscillates at ~21 GHz. With an RF input greater than −35 dBm, the self oscillation is suppressed. In the frequency domain, only one single desired frequency peak is observed. For level 0 when all the attenuators are on, the self oscillation is suppressed to provide a near zero amplitude output. In Section III, experimental verification of this is presented.

III. Measurement Results

Fig. 7 shows the large signal measurement setup for the frequency and time domain characterization. For frequency domain measurements, the output is connected to a power meter through an HP8485A power sensor. For time domain measurements, the output is connected to an Agilent 86100B wide bandwidth oscilloscope. To characterize the time domain response of multi-level PA, an on-chip divide-by-32 block is included to generate 525-MHz signal for oscilloscope triggering. The three address decoder inputs are fed from a Tektronix HFS 9009 Stimulus System, which can provide 4 synchronized signals up to 400 MHz. The clock frequency is 400 MHz and the frequency of inputs for the address decoder is 200 MHz. The inputs can be randomly chosen using the stimulus system. For illustration, a randomly chosen pattern (0241353246) is used for the dynamic measurements.

At 1.5-V supply voltage for the driver stages and 1.2-V supply voltage for the PA stage, Fig. 8 shows the single-ended PA is able to achieve power gain of ~30 dB, 10-dBm saturated power and ~22-% maximum PAE at 16.8 GHz while drawing 30.5 mA and consuming 45.8 mW. The drain efficiency of last PA stage is ~38%. Fig. 8 shows that it is possible to provide sufficient linear power. The output $P_{1\,dB}$ ($OP_{1\,dB}$) is ~7.5 dBm, which corresponds to ~10.5-dBm $OP_{1\,dB}$ for a differential PA structure. In actual operation, the PA will operate below the $OP_{1\,dB}$ point much of the time to implement the multi-level amplitude modulation.

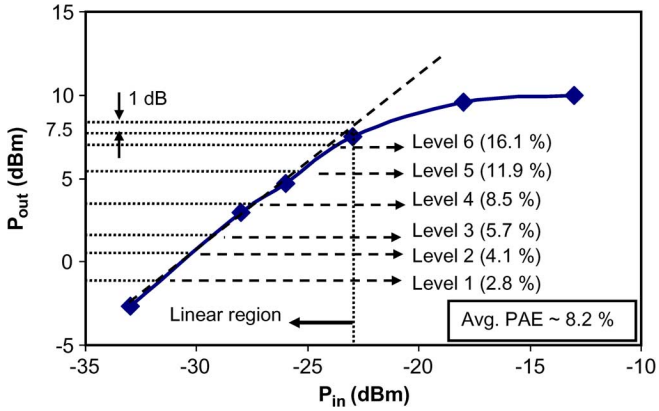

Fig. 8. Output power of single ended PA versus input power at $V_{DD} = 1.5$ V for the driver stages and 1.2-V supply for the PA stage. $OP_{1\ dB}$ is 7.5 dBm (with all the attenuators off).

By applying constant DC inputs to the address decoder, static level test can be performed. Fig. 9(a) shows the static time domain measurement results for level 0 and level 6. The input power level to the PA is ~ -10 dBm. The frequency of output sinusoidal waveform is 16.8 GHz, which is the same as the PA input frequency. When the PA output is connected to a spectrum analyzer, no other peaks except the desired 16.8-GHz peak are seen at all output levels. The output power at level 0 is approximately -20 dBm. This means the self oscillation is suppressed for level 0. Level 2 to level 5 measurement results are summarized in Table IV. After de-embedding the probe and cable losses, the corresponding output power for level 6 is $\sim$7 dBm, which means the single-ended PA operates close to the $OP_{1\ dB}$ point. This is consistent with the original design. When a differential PA is used, $OP_{1\ dB}$ will be $\sim$10 dBm. The current consumption for each level is also summarized in Table IV. The PAE performance for level 1 to level 6 is marked in Fig. 8 with the average efficiency of $\sim$8%. By realigning the highest output power level to the 10-dBm saturated output power, the efficiency can be further improved. By using a differential PA integrated in the CDMA TX chain, expected link margin can be around 20 dB assuming RX noise figure of 8 dB, bandwidth of 50 MHz (one of eight channels), minimum signal to noise ratio of 14.5 dB, and propagation/antenna loss of 55 dB at 15-cm separation with a metal cover [22].

Fig. 9(b) is the dynamic measurement results for the chosen random pattern (0241353246). The rise and fall times of the 3 inputs and clock are set to 200 ps, which is the minimum for the stimulus system. There are built-in inverter buffer chains on chip for squaring the input waveform. The PA output is AC-coupled. Because of this, the waveform in Fig. 9(b) is symmetrical with respect to the time axis. Each level has a period of $\sim$2.5 ns to support the 400-Mbps data rate. Table IV also summarizes the measurement results of level ratio between level N ($N = 6$, 5, 4, 3, 2) and level 1, and the percent error is compared with the ideal. The measured rise and fall times for some of the transitions are listed in Table V.

The level 0 output voltage is only 31 mV which should be acceptable. The 19-dB difference between level 0 and level 1 is sufficiently large for the ASK receiver to distinguish between

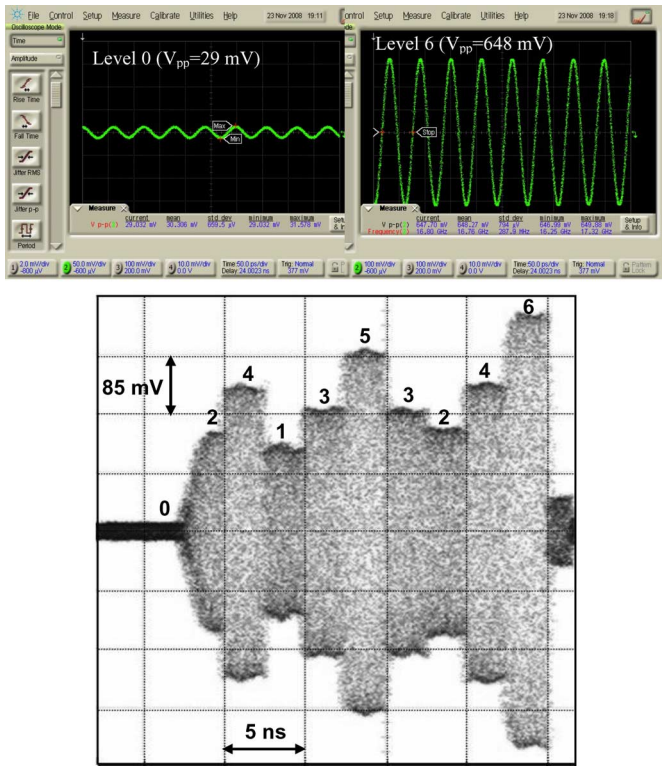

Fig. 9. (a) Time domain measurement results for static level 0 and level 6 operating at 16.8 GHz. (The value of V_{pp} is before de-embedding cable loss). (b) Time domain measurement results for a dynamic input pattern of 0241353246.

the 2 levels. More importantly, the frequency of signal is the same as that for the input of 16.8 GHz, which indicates that this is due to the feed through of input signal. As explained in Section II, self oscillation can occur at the last PA stage, it can be suppressed by properly setting the impedance Z_s [Fig. 3(a)]. This has been experimentally verified. The maximum percent error of the level ratio is $\sim$16% (level 3 to level 1). The error can be fixed by re-tuning the attenuator sizes. A switch (attenuator) array using an even smaller unit cell will be useful for post fabrication tuning to improve the level ratio accuracy. From the measurements, the worst rise time is $\sim$800 ps (level 0 to level 2 transition), which is largely determined by the gate bias resistor at the second pre-driver stage as discussed in Section II. This rise time can be decreased by lowering the bias resistor at the gate of second pre-amplifier to 0.8 kΩ. This however reduces the signal level at the input of second stage and another amplification stage is needed following the second stage to maintain the output power of PA. This in conjunction with decreasing the level-0 switch size reduces the rise time (level 0 to level 2) to $\sim$300 ps in simulations. The rise and fall times for other level transitions are $\sim$200 ps, which are shorter than the original target.

Fig. 10 shows the die micrograph and the test printed circuit board (PCB). The differential class-E PA with an address decoder and bond pads occupies $\sim$ 1.4 mm^2. The circuit was measured on a printed circuit board to improve the reliability of measurements. However, due to the bonding scenario of the test chip on a printed circuit board, only the single-ended measurements mentioned earlier were made.

TABLE IV
MEASUREMENT RESULTS SUMMARY OF STATIC CASE (ADDITIVE/SUBTRACTIVE CODING)

	V_{peak} (mV)	Power (dBm)	Current (mA)
Level 0	31.0	-20.2	
Level 1	268.2	-1.4	19.6
Level 2	331.5	0.4	20.2
Level 3	390.4	1.8	20.3
Level 4	478.6	3.6	20.4
Level 5	577.4	5.2	21.2
Level 6	692.6	6.8	22.5

Ideal ratio		Measured ratio results	Error (%)
Level 2 / Level 1	$\sqrt{2}$	1.24	-12.3
Level 3 / Level 1	$\sqrt{3}$	1.45	-16.0
Level 4 / Level 1	$\sqrt{4}$	1.79	-10.8
Level 5 / Level 1	$\sqrt{5}$	2.15	-3.9
Level 6 / Level 1	$\sqrt{6}$	2.58	5.3

TABLE V
MEASUREMENT RESULTS SUMMARY OF RISE AND FALL TIMES OF SOME LEVEL TRANSITIONS

Transitions	Rise or Fall time (ps)
Level 0 – level 2	830
Level 2 – level 3	180
Level 3 – level 1	180
Level 1 – level 3	180
Level 3 – level 5	240
Level 5 – level 3	180
Level 3 – level 2	180
Level 2 – level 4	180
Level 4 – level 6	300
Level 6 – level 0	360
Level 0 – level 6	660
Level 4 – level 1	240
Level 6 – level 2	180

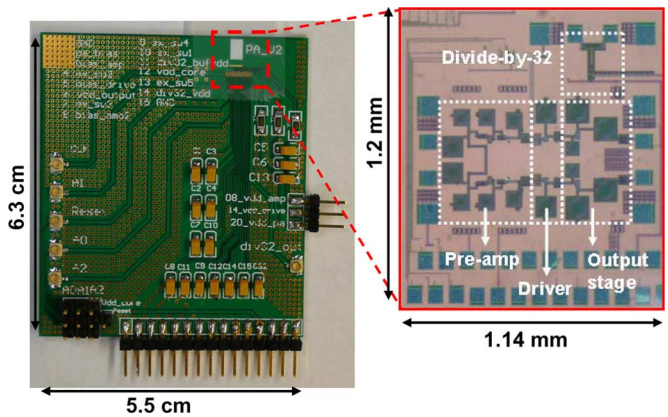

Fig. 10. Test printed circuit board (6.3×5.5 cm^2). Die micrograph of the differential multi-level power amplifier (1.14×1.2 mm^2).

IV. CONCLUSION

A technique to support 400-Mbps data rate using multiple-level amplitude modulation of a nonlinear power amplifier with negative resistance enhanced power gain is proposed and demonstrated in a 16.8-GHz seven-level amplitude modulated class-E PA. This is accomplished by adding attenuators that both reduce the signal level as well as that change the impedance seen by the PA stage for suppression of self-oscillation at low output power levels. The single-ended PA fabricated in a 130-nm foundry logic CMOS process achieves power gain of ~30 dB, and power-added efficiency (PAE) of 16% for the highest output power level of 6.8 dBm. The average efficiency for a random data pattern is ~8%. The circuit also exhibits 10-dBm saturated output power and ~22% maximum PAE while consuming 45.8 mW. By realigning the highest output power level to the 10-dBm saturated output power, the efficiency can be improved. The drain efficiency of last PA stage is ~38%. Lastly, this work suggests that by using a combination of switched attenuators and a nonlinear Class-E PA, power efficiency of multiple-level amplitude modulated PAs can be improved over linear PAs.

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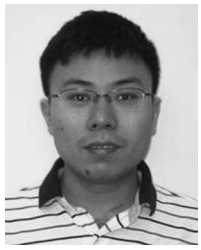

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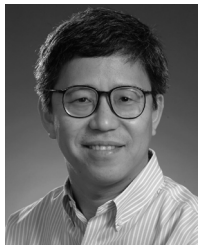

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