Progress and Challenges Towards Terahertz CMOS Integrated Circuits

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***Abstract*—Key components of systems operating at high millimeter wave and sub-millimeter wave/terahertz frequencies, a 140-GHz fundamental mode voltage controlled oscillator (VCO) in 90-nm CMOS, a 410-GHz push-push VCO with an on-chip patch antenna in 45-nm CMOS, and a 125-GHz Schottky diode frequency doubler, a 50-GHz phase-locked loop with a frequency doubled output at 100 GHz, a 180-GHz Schottky diode detector and a 700-GHz plasma wave detector in 130-nm CMOS are demonstrated. Based on these, and the performance trends of nMOS transistors and Schottky diodes fabricated in CMOS, paths to terahertz CMOS circuits and systems including key challenges that must be addressed are suggested. The terahertz CMOS is a new opportunity for the silicon integrated circuits community.**

***Index Terms*—CMOS, detector, frequency doubler, on-chip patch antenna, Schottky barrier diode, VCO.**

I. INTRODUCTION

ELECTROMAGNETIC waves in the sub-millimeter wave or terahertz (300 GHz–3 THz) region of spectrum have been utilized in spectroscopy, in active and passive imaging for detection of concealed weapons, chemicals and biological agents, as well as in short range radars and secured high data rate communications [1]–[3]. A simplified block diagram of THz spectrometer for chemical detection shown in Fig. 1 consists of a transmitter with a tunable signal generator and an antenna, and a receiver with an antenna, a detector or a mixer followed by a low noise amplifier/filter. The signal generator is usually constructed with a tunable signal source operating around 10 GHz, a chain of III–V Schottky diode frequency multipliers with one of two amplifiers interspersed in the chain [2]. The detector usually uses a Schottky diode mixer to down convert input signal to intermediate frequency. The system is similar to a one-way communication system. Fig. 2 shows an example of sub-millimeter wave systems. The high cost and low level of integration of the devices have limited the proliferation of these applications. The devices are interconnected by waveguides, which makes them also bulky.

Recent progress in CMOS (Complementary Metal Oxide Silicon) integrated circuits (ICs) and SiGe HBT technologies has made it possible to consider silicon technology as an alternative means for realization of capable and economical systems that operate at 200 GHz and higher. This paper discusses the devices available in CMOS, and fundamental circuit building blocks of sub-millimeter wave systems (signal sources, detectors and antennas) operating between 100 and 700 GHz fabricated using the devices [4]. Based on these, this paper suggests paths for achieving terahertz CMOS circuits and systems as well as the challenges.

II. TRANSISTORS AND DIODES IN CMOS

The consideration for terahertz operation of circuits in CMOS is enabled by its scaling. This section briefly discusses the state of the art and projected high frequency performance of transistors and diode structures that can be use to fabricate sub-millimeter wave systems in CMOS.

A. Speed Performance of nMOS Transistor

Fig. 3 shows the projected high frequency performance requirements of nMOS transistors, and SiGe and InP hetero-junction bipolar transistors (HBTs) in manufacturing. These plots are extracted from the 2008 International Roadmap for Semiconductors (*ITRS*) [5]. By year 2013, the projected nMOS unity power gain frequency ($f_{\max}$) requirement is $\sim$ 510 GHz. With such transistors, it will be possible to increase the operating frequency of silicon amplifiers to above 300 GHz from $\sim$ 140–160 GHz [6], [7]. However, there has been a great deal of concern whether the CMOS technology scaling can continue. The reports of an nMOS transistor of a 65-nm bulk CMOS technology [8] with $f_{\max}$ of 420 GHz in 2006, and an SOI (Silicon on Insulator) transistor of a 45-nm process with $f_{\rm T}$ of 450 GHz [9] in 2007 suggest that the industry has been able to

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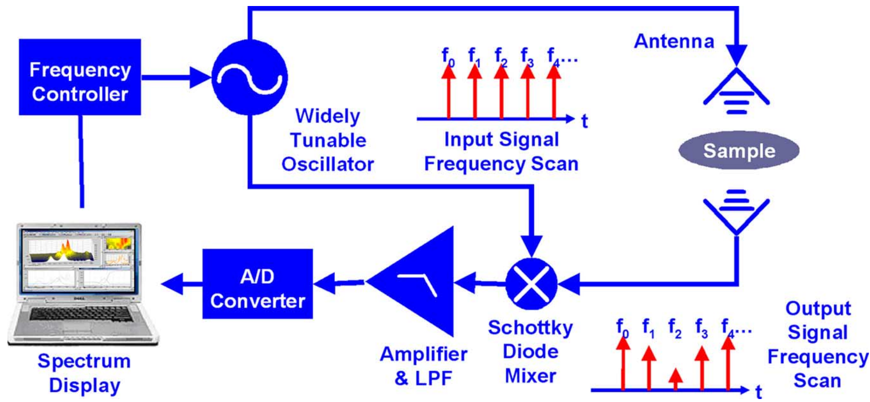

Fig. 1. Block diagram of a sub-millimeter wave spectrometer.

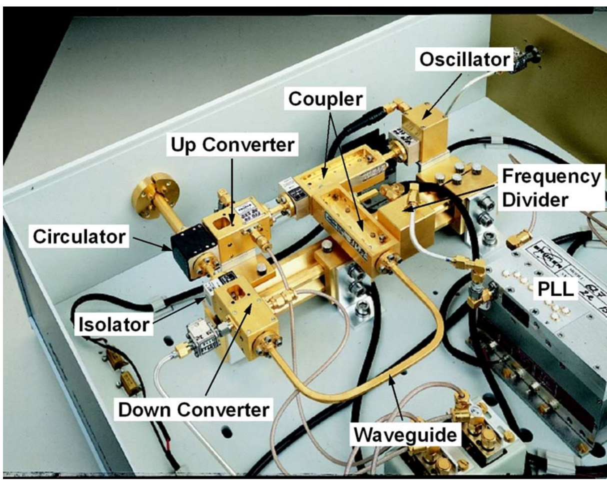

Fig. 2. Photograph of a sub-millimeter wave system.

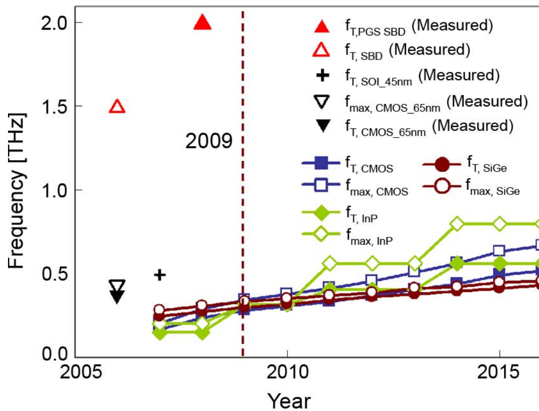

Fig. 3. Projected performance requirements of nMOS transistors from 2008 International Road Map for Semiconductors [4] and the data from the literature.

keep up with the *ITRS*. These are higher than that reported for SiGe HBTs.

B. Schottky Diodes for THz Operation

In the near term, at frequencies higher than ~ 400 GHz, it will be difficult to achieve amplification using nMOS transistors. A way to deal with this is to use passive detectors and frequency multipliers as routinely done for sub-millimeter and

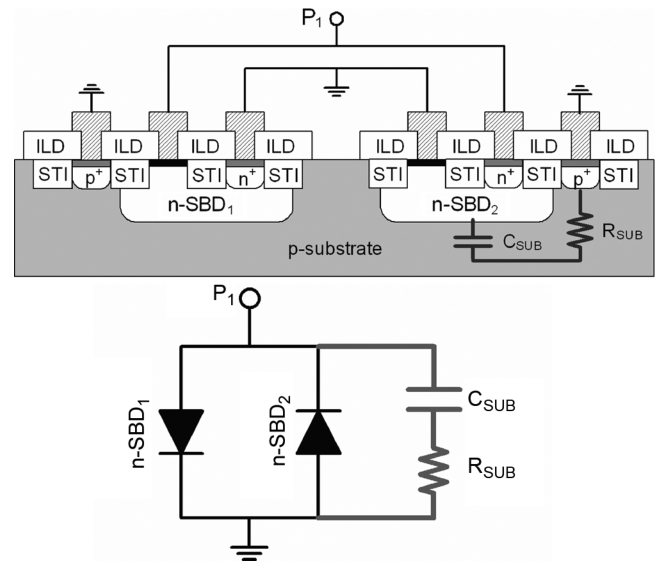

Fig. 4. Integrated Schottky diodes in CMOS.

THz systems [2]. In particular, Schottky diodes are widely used for this purpose. It is possible to implement THz diodes in CMOS without any process modifications. Fig. 4 shows a cross section. The Schottky contact is formed on a diffusion region where there are no source/drain implants. The ohmic contacts placed on n^+ implanted parts of an n-well form an n-terminal. Such a diode with a $CoSi_2$–silicon Schottky junction has been realized in a 130-nm CMOS process [10]. The Schottky contact area is set at the minimum to maximize the cut-off frequency. This type of diodes can also be used for frequency multiplication to generate sub-millimeter wave signals [2], [11]–[13].

A diode formed using sixteen $0.32\ \mu\mathrm{m} \times 0.32\ \mu\mathrm{m}$ cells connected in parallel has measured series resistance, $\mathrm{R_s} = 13\ \Omega$ and capacitance, $\mathrm{C} = 8$ fF. The corresponding cut-off frequency $(f_\mathrm{T} = (2\pi \mathrm{R_s C})^{-1})$ is ~ 1.5 THz. The resistance of structure is limited by that associated with the n-well region under the Schottky junction surrounded by the shallow trench isolation. This is particularly of concern because this will prevent scaling up of cut-off frequency with the technology scaling. This is exacerbated by the fact that the thickness of shallow trench has been scaling slower than the lateral dimensions. All these can effectively be eliminated by using a polysilicon gate separated

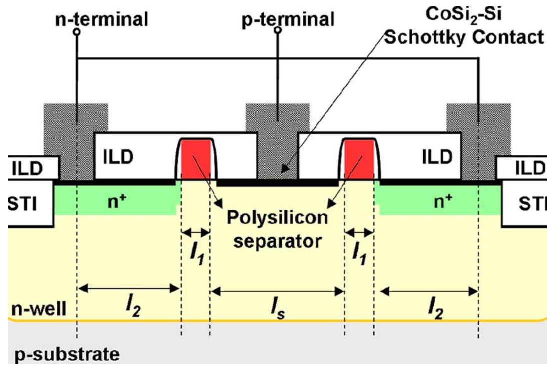

Fig. 5. Polysilicon gate separated Schottky barrier diode.

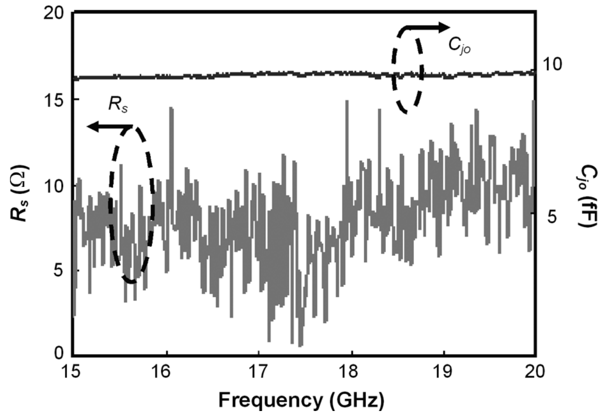

Fig. 6. Series resistance (R_s) and capacitance (C) of $160.4\ \mu m \times 0.4\ \mu m$ polysilicon gate separated (PGS) diodes. The corresponding cut-off frequency is ~ 2 THz.

Schottky diode structure shown in Fig. 5. Use of this structure however requires the unit Schottky diode area to be increased to $0.4 \times 0.4\ \mu m^2$ in the 130-nm CMOS process because of the polysilicon gate to contact spacing design rule. By using this structure, series resistance and capacitance of $8\ \Omega$ and 10 fF or cut-off frequency of ~ 2 THz have been measured [13]. Fig. 6 shows the series resistance and capacitance versus frequency (15–20 GHz) plots extracted from measured S-parameters. With such diodes, it should be possible to build detectors operating above 500 GHz.

Anti-parallel diode pairs (APDPs) are utilized in sub-harmonic mixers and frequency multipliers. If these are implemented using only the n-type SBDs (Fig. 4), the circuit operating frequency is limited by the parasitic capacitance to substrate and substrate resistance. To mitigate these, a shunt connected complementary APDP (C-APDP) using n- and p-type SBDs is proposed (Fig. 7). The measured cut-off frequency of shallow trench isolated C-APDP fabricated in a 0.13-μm CMOS logic process is ~ 470 GHz, which is sufficient for millimeter-wave frequency applications [14]. Using PGS SBDs, it should be possible to increase this to ~ 700 GHz.

III. CMOS Approach

Based on the discussions in Section II, it is likely that the nMOS transistors and Schottky diodes have or in near future will have sufficient bandwidth to support operation at the

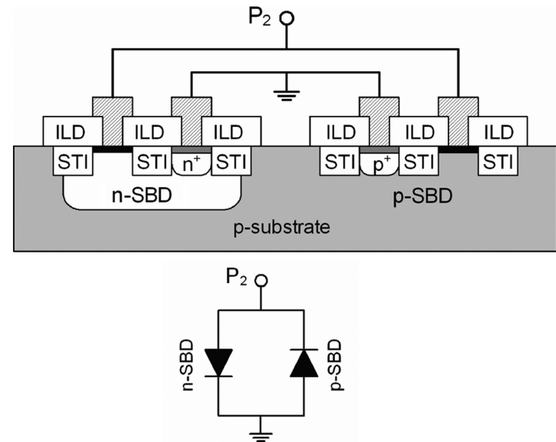

Fig. 7. Complementary antiparallel diode pair.

sub-millimeter-wave/terahertz frequencies. An obvious question is why use CMOS which has inferior transistor and passive performance than those of highly optimized components in III-V based technologies. The reasons are the familiar ones. They are essentially the same as those for RF and millimeter wave CMOS. If digital CMOS logic technologies or a version of CMOS with a few straightforward modifications can be utilized, the cost of developing a technology and fabrication infrastructure can be limited or largely avoided since they will be paid for by the digital applications. Additionally, all other capabilities of CMOS such as integration of sub-millimeter wave circuits with baseband analog and digital subsystems leading to a smaller size, digital calibration that corrects imperfections for higher yield and better performance, built-in self test and high yield will be available. More importantly, for CMOS to be viable, it must be able to support sufficient useful performance not the ultimate performance. If a moderate volume terahertz application can be defined, then use of CMOS could enable compact, affordable and practical terahertz systems. Lastly, CMOS can support a chip area greater than 2 cm × 2 cm, which makes it well suited for 2-D arrays with a large number of elements. Silicon technology is the only that could make such systems practical.

IV. Signal Generators

As mentioned earlier, a signal generator is a fundamental block for a wide variety of sub-millimeter wave systems. This section describes approaches for generating signals in sub-millimeter wave frequencies and terahertz in CMOS.

A. Fundamental Mode Voltage-Controlled Oscillator (VCO)

Fig. 8 shows the schematic of 140-GHz VCO fabricated in a 90-nm logic CMOS process [15]. It employs LC-resonators. Cross-coupled nMOS transistors (M_1, M_2) form the VCO core. Inductors (L_1, L_2), accumulation mode MOS capacitors/varactors (C_1, C_2), and the capacitances associated with M_1 and M_2 form the *LC* resonators. The inductors, L_1 and L_2, are built using a single loop circular inductor. The VCO utilizes lumped elements which are more compact and higher Q than those based on transmission lines [16]. The output frequency can be tuned from 139 to 140.2 GHz by changing the varactor voltage and

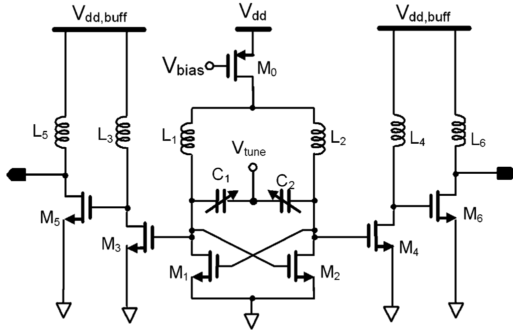

Fig. 8. Schematic of 140-GHz Voltage controlled oscillator.

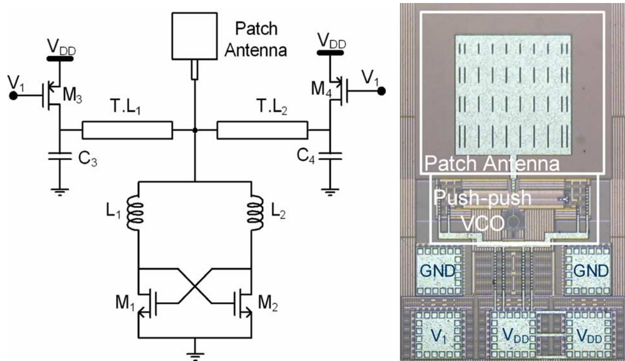

Fig. 9. Schematic and photograph of a 410-GHz push-push VCO in 45 nm.

bias current [15]. The measured output power is ~ -19 dBm. The key for achieving the high operating frequency is reduction of the parasitic capacitance in the L-C tank that allows increase of the core size transistor [16]. This is accomplished by using a tapered buffer, through optimal trade-off between gate-to-drain and drain-to-body capacitances ($\mathrm{C_{GD}}$ adds 4 times as much as $\mathrm{C_{DB}}$), and limiting the size of ground shield of inductor. The widths of transistors for the first and second buffer stages are $\sim$ 0.3X and 1.2X of that for the core transistors. The measured phase noise is ~ -85 dBc/Hz at 2-MHz offset from the carrier. The tuning range is limited because the design is targeted for high operating frequency. Using a similar oscillator topology in a 45-nm CMOS with low leakage transistors, 180-GHz fundamental signal with output power level of ~ -30 dBm has been generated [17].

B. Push-Push VCO

The frequency of signal generated in CMOS can be further increased using push techniques that multiplies the output frequency [17]–[25]. This technique can also lower the fundamental frequency of voltage controlled oscillators that can be exploited to increase the output frequency range and to increase varactor Q-factor for lower phase noise. Fig. 9 shows the schematic of 410-GHz push-push VCO fabricated in 45-nm CMOS [17]. The push-push VCO is the same as the 180-GHz fundamental VCO except that the buffers for the fundamental outputs are removed to increase the output frequency. At the virtual ground nodes, the antiphase fundamental signals cancel out and the second harmonic signal can be extracted. The

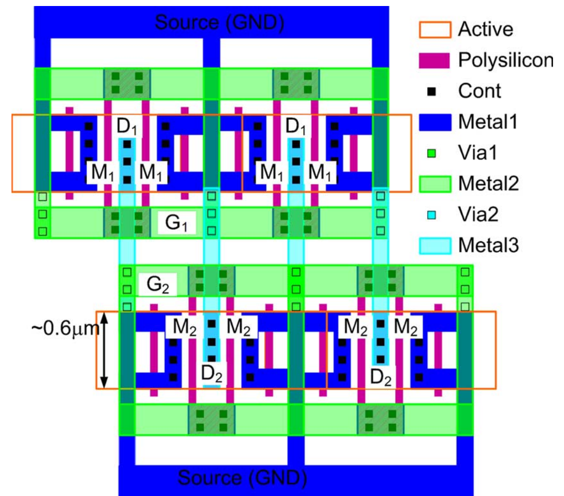

Fig. 10. Layout of cross-coupled transistors $\mathrm{M_1}$ and $\mathrm{M_2}$ in the 410-GHz push-push oscillator.

middle point of inductors $\mathrm{L_1}$ and $\mathrm{L_2}$ has the parasitic capacitance to ground with the lowest value and highest Q among the common-mode nodes. This makes the impedance at the resonant frequency the highest, and makes the node the preferred location to extract the push-push output [22]. A quarter wavelength transmission line tuned for the second harmonic frequency is usually used to increase the amplitude of second harmonic while suppressing the fundamental signal [22], [23]. The transmission line is formed using the grounded coplanar waveguide (GCPW) structure. Compared to the conventional CPW, the ground plane isolates the signal line from the lossy silicon substrate and reduces the insertion loss. The lines are formed using the top bond pad metal layer and the ground plane is formed by shunting metal layers 1 and 2.

Fig. 10 shows the layout of cross-coupled transistors $\mathrm{M_1}$ and $\mathrm{M_2}$. The width of transistors is 10 μm. The transistors utilize a multiple finger gate layout and their polysilicon gate fingers are contacted on both ends using two contacts to lower gate resistance. The gate fingers are connected using metal 2 lines. Cross-coupling of the transistors is accomplished using a metal 3 connection. The fixed polysilicon gate pitch along with the requirement for a dummy polysilicon gate in the process limits the flexibility to trade the larger drain to body capacitance for lower drain to gate overlap capacitance that allows use of larger transistors with more negative resistance [16]. The circuit occupies 640 μm $\times$ 390 μm including the bond pads. The die photograph is also shown in Fig. 9.

Measurements of $\sim$400 GHz oscillator outputs are challenging. Presently, there are no commercially available electronic probes for measurements at this frequency. Because of this, an optical technique is utilized. To enable this, an on-chip patch antenna is integrated with the oscillator. The antenna structure is discussed in more detail in Section V. The spectrum of VCO is measured using a Bruker 113 V Fourier Transform Infrared Spectroscopy system (Fig. 11). The absolute power level was measured using a silicon bolometer (HD-3, 1378) from Infrared Laboratories (Fig. 11). Fig. 12 shows an output spectrum. The total power measurement from the bolometer

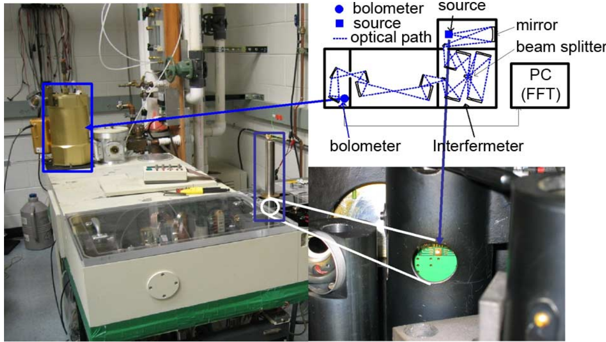

Fig. 11. Bruker 113 V Fourier Transform Infrared Spectrometer used to measure the 410-GHz oscillator. The green part on the lower right corner is the printed circuit board containing the oscillator. The bolometer is shown in the upper left part.

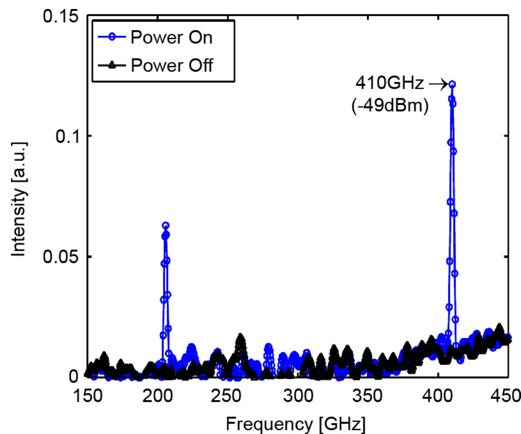

Fig. 12. Output spectrum of the 410-GHz push-push VCO when it is powered and powered off.

was converted to the power for each peak of the spectrum using the relative intensities. The measured signal level is −49 dBm at 411 GHz. The circuit consumes 17 mW at $V_{DD} = 1.5$ V. The power level is low mostly due to the losses of transistors and thin metal layers in the CMOS process, and the mismatch between the tuned frequencies of patch antenna and oscillator. Table I summarizes the measurement and simulation results. Excluding the losses associated with the antenna, output power is −42 dBm. Simulations suggest that if the Q of bypass capacitors C_3 and C_4 is increased to 5 at 200 GHz, and substrate resistance of transistors is increased to 1000 Ω, then the output power of the oscillator can be increased to −18 dBm. As will be discussed in Section V, it will also be possible to reduce the antenna loss.

The output frequency of 410 GHz is the highest for signals generated using transistors in any technologies including those based on compound semiconductors. An nth order harmonic signal can be generated using superposition of n signals with phase offsets of $360°/n$ [24], [25] Applying this technique in 45-nm CMOS should result signal generation at ~ 800 GHz [13].

C. Phase-Locked Loop (PLL)

Generation of free running high frequency signal by itself is not sufficient. The signal must be stabilized using a phased

TABLE I
SUMMARY OF 410-GHz VCO PERFORMANCE

Measured Power	-47 dBm
2nd Order Harmonic Power	-49 dBm
Antenna loss	7 dB
Mismatch loss	2 dB
Back calculated Push-push P_{out}	-40 dBm
Simulated push-push P_{out} with inductor Q of 6 @200GHz, bypass cap Q of 1 @400GHz and R_{sub} of 200Ω.	-39 dBm
Simulated push-push P_{out} with inductor Q of 6 @200 GHz, bypass cap Q of 5 and R_{sub} of 1000 Ω.	-18 dBm
Power Consumption (V_{DD}=1.5V)	17 mW

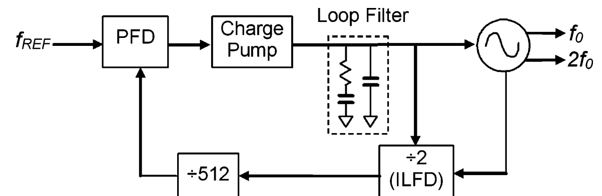

Fig. 13. 50-GHz phase-locked loop block diagram.

locked loop. To address this, a fully integrated PLL tunable from 45.9 to 50.5 GHz, which also outputs the second order harmonic at frequencies between 91.8 and 101 GHz, has been demonstrated in a 130-nm logic CMOS process [26]. Fig. 13 is a block diagram of 50-GHz PLL. The circuit utilizes an injection-locked frequency divider (/2) (ILFD), and a 1/512 static frequency divider. The phase frequency detector (PFD) uses a three-state phase detection scheme. The loop filter is second order and the PLL is third order. The loop filter consists of two MOS capacitors and one polysilicon resistor. The loop bandwidth target is ~ 500 kHz and the phase margin is ~70 degrees. The reference frequency for the PLL is ~ 50 MHz. The injection locked divider is an LC-tank type [27], which is essentially an oscillator running near the frequency a half of that for the VCO. Fig. 14 shows the schematic of VCO and injection locked divider combination.

The output power level is about −10 dBm at 1.5-V V_{DD} and 12-mA VCO bias current, and the phase noise while free running is about −90 and −109 dBc/Hz at 1-MHz and 10-MHz offset from the carrier, respectively. The output power of second harmonic near 100 GHz is −22 dBm. The second harmonic output is the first signal above 100 GHz ever locked by a silicon circuit. The chip size is 1.16 × 0.75 mm^2 including bond pads. Usually, the first frequency divider limits the maximum PLL operating frequency. Since the injection locked divider (Fig. 14, right) is an oscillator whose operating frequency is lower than that of the VCO, the PLL maximum frequency is limited by the maximum VCO frequency instead of that for the divider. This means it should be possible to lock the 410-GHz signals in 45-nm CMOS. If the output frequency can be quadrupled using four quadratures, it should be possible to lock ~ 800 GHz signal [13].

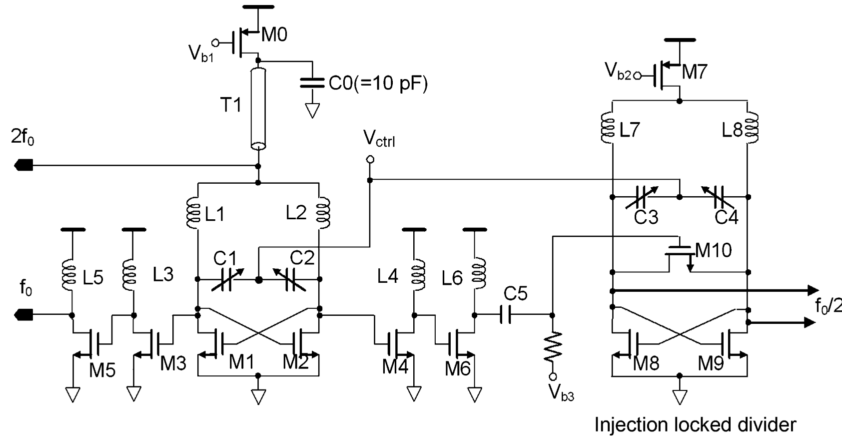

Fig. 14. VCO and injection locked divider.

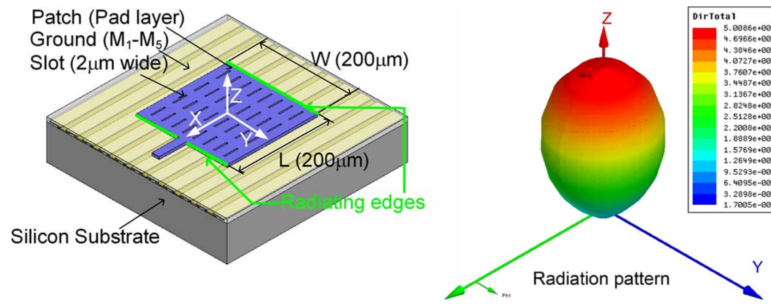

Fig. 15. Patch antenna and its radiation pattern. The peak directivity is 5.

D. Frequency Multiplication Using Schottky Diodes

As commonly done in sub-millimeter wave systems using discrete components [2], the Schottky barrier diodes in CMOS can also be used to increase signal frequency by using frequency multiplication. Like the push technique, use of a diode frequency multiplier can increase output frequency range and lower phase noise. As mentioned, Schottky diodes fabricated in CMOS have significant cathode (n-well) to substrate capacitance (40 fF for a diode with a 1.64-μm^2 anode area and 5.8-fF Schottky junction capacitance) as well as non-negligible substrate resistance. These make use of a series topology for frequency multiplication in [11], [28] difficult in CMOS. To overcome this, a balanced topology with two shunt diodes with grounded cathodes [29]–[31] which also increases the output power is utilized for the CMOS implementation [12], [13]. The doubler fabricated in 130-nm CMOS uses two shunt SBDs (0.64 $\times$ 0.64 μm^2 unit cell area with f_T of 680 GHz and m_j of 0.5) achieves the minimum conversion loss (CL) of about 10 dB at input power of 8.5 dBm, corresponding to $\sim$10% efficiency. The circuit utilizes diodes with larger unit cells with higher $\mathrm{m_j}$ than that using the minimum sized unit cells to reduce CL [32]. The maximum output power is ~ -1.5 dBm at 125 GHz. There is no saturation of CL up to input power of 8.5 dBm suggesting that the doubler should be able to provide even higher output power if an input signal source with higher calibrated power is used. With the 2-THz diodes, it should be possible to generate outputs at 500-700 GHz with reasonable efficiency.

V. On-Chip Patch Antenna

The 410-GHz oscillator utilizes a patch antenna for optical spectrum analyses. Fig. 15 shows the patch antenna. The size of patch is 200 $\times$ 200 μm^2. The patch is formed using the bond pad metal layer while the ground plane is formed with metal layers 1–5 shunted together in the 45-nm CMOS process. The patch and ground plane are separated by a $\sim$4 μm thick SiO_2 layer. Fig. 15 also shows the radiation pattern. The peak directivity in the direction perpendicular to the patch is 5. As also shown in Fig. 15, patch antennas rely on fringing fields for radiation and its efficiency is strongly dependent on the patch size to the dielectric layer thickness ratio. Increasing the dielectric layer thickness from 4 to 7 μm in simulations improves the efficiency to 50% (Fig. 16). This in combination with better matching the antenna and oscillator operation frequencies will reduce the overall losses of antenna from 9 to $\sim$ 3 dB.

VI. Detector Circuits

To implement the sub-millimeter wave system in Fig. 1, a detector is also required. This section describes approaches for using Schottky diodes and MOS transistors in passive detectors. To evaluate use of Schottky diodes in a detector, a 182-GHz detector was fabricated once again using 130-nm foundry CMOS [33]. The detector test signal was generated on-chip by modulating the bias current of a push-push VCO. As shown in Fig. 17 (middle), the detector consists of a $\sim$ 180-GHz RF matching circuit, a Schottky diode, a low-pass filter with $\sim$ 10-GHz corner frequency, and an amplifier for driving a 50-Ω load. The diode

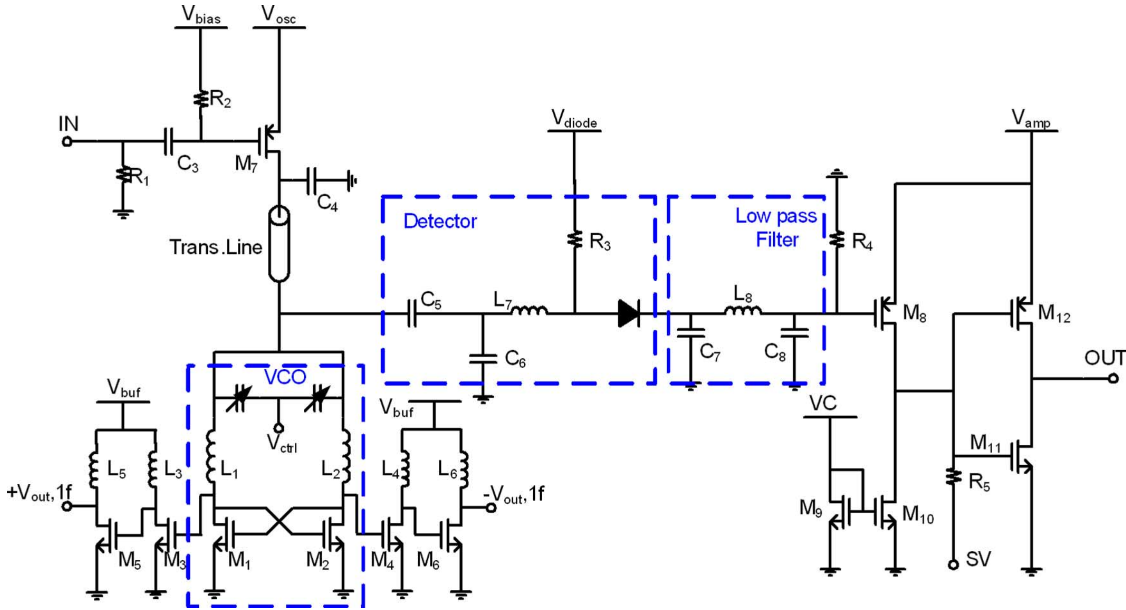

Fig. 17. Detector schematic.

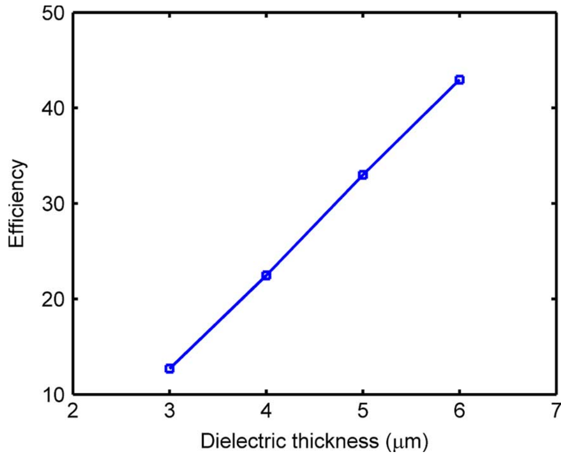

Fig. 16. Antenna efficiency versus the thickness of dielectric layer between the patch and ground plane.

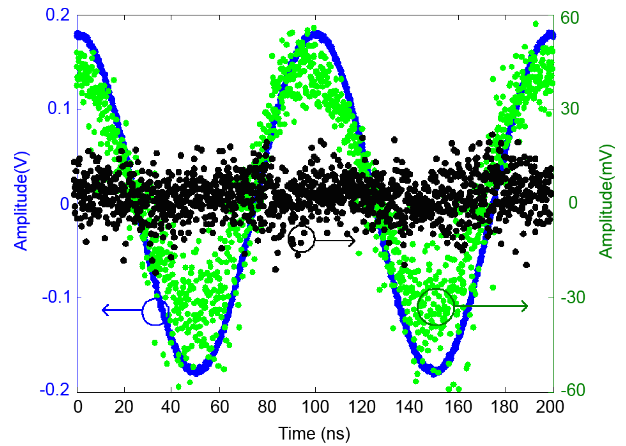

Fig. 18. Modulation signal and demodulated signals when V_{DD} of modulator is 1.75 and 0.3 V.

has been forward biased (0.3 mA) through a 1-kΩ resistor (R_3) to maximize the conversion gain [34], [35]. The detector input is conjugately matched to the signal source output at ~ 180 GHz.

The left portion of Fig. 17 shows a schematic of the circuit for generating the modulated 182-GHz signal. This design utilizes the 192-GHz VCO in [22]. Buffers were added to monitor the fundamental VCO output. This lowered the frequency at push-push port to ~ 182 GHz. The amplitude of this VCO was modulated by changing the gate voltage of M_7, or the bias current (I_{bias}) of oscillator. The DC bias voltage at gate of M_7 (V_{bias}) is 0 V. The bypass capacitor C4 is an AC-short for the signal near 180 GHz, but it presents high impedance to the modulating signal. Since changing I_{bias} also modifies the drain voltage of VCO core transistors and thus the capacitances of L-C tanks [22], the input signal also modulates the output frequency by ~50–100 MHz. Fig. 18 shows the voltage waveforms of modulation and detected signals across a 50-Ω load, when the VCO is modulated with 10-MHz 0.1-V amplitude input signal at 1.75-V V_{DD} and 0.3-V V_{DD} for the modulator. Reducing the supply voltage can quench oscillation and make the detector output to flatten out suggesting the detector is indeed detecting the modulated signal.

There is also a concern whether the detector is picking up the modulated fundamental signal instead of the modulated frequency doubled signal. Fig. 19 shows the fundamental and frequency doubled signal power at the push-push output of a test structure. It shows that the unwanted fundamental output is at least 10 dB lower than the frequency doubled output. Fig. 20 shows the effects of diode bias on the modulated output at 0.3-V V_{DD} for the modulator. When the diode bias is zero, the output of modulator completely flattens out suggesting that the modulation signal is not somehow fed through power lines or the substrate. These all together indicate that the detector has successfully detected 182-GHz modulated signal in 130-nm CMOS. Fig. 21 show photographs of chip including the modulator and

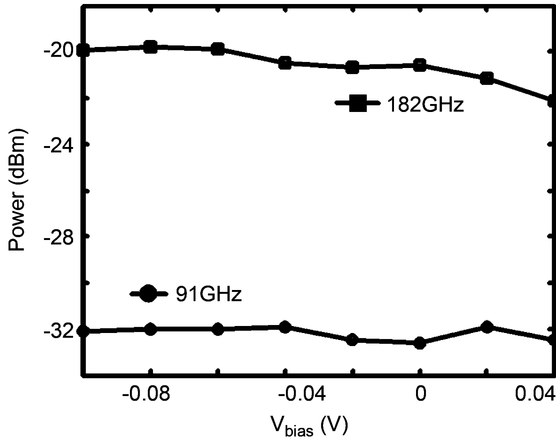

Fig. 19. Fundamental and frequency doubled signal power at the push-push output of a test structure. It shows that the fundamental output is at least 10 dB lower than the frequency doubled output.

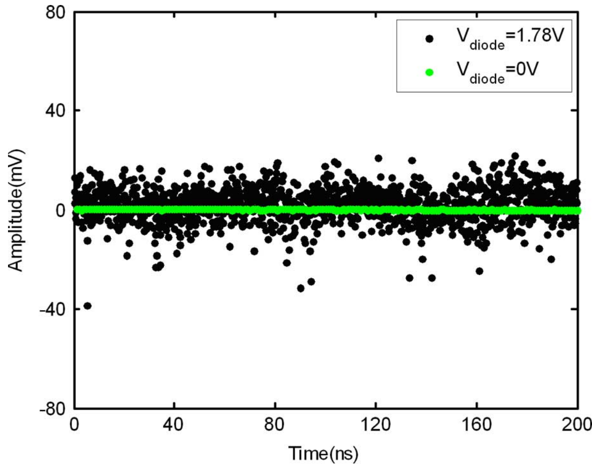

Fig. 20. Effects of diode bias on the modulated output at 0.3-V V_{DD} for the modulator. When the diode bias is zero, the output of modulator completely flattens out suggesting that the modulation signal is not somehow fed through power lines or the substrate. See Fig. 17 for V_{diode} definition.

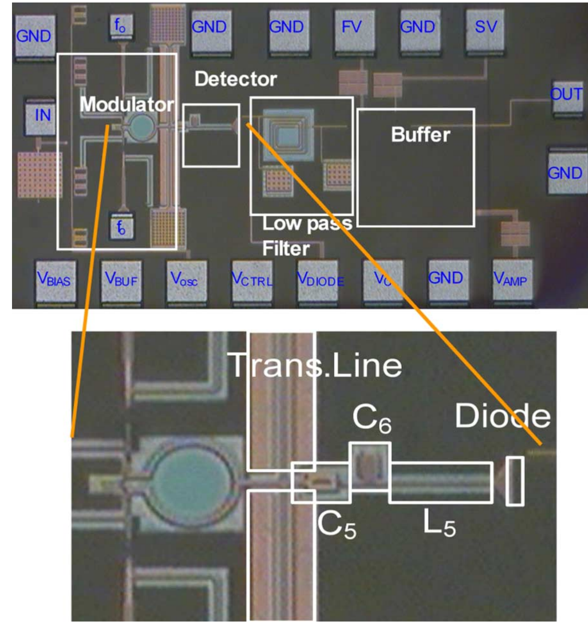

Fig. 21. Die photographs of detector.

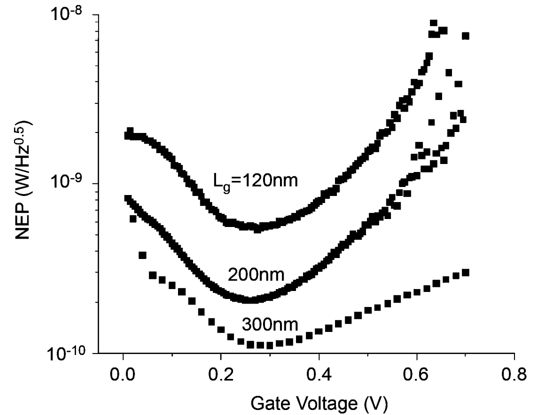

Fig. 22. Noise equivalent power as a function of the gate voltage V_g for MOSFETs with varying gate lengths, $T = 300$ K.

detector. It also contains an enlarged photograph of the detector portion. The chip size is 1120×600 μm^2 including bond pads.

Sub-millimeter wave signals can also be detected by exciting plasma waves of electron density in field effect transistors [36]. Recently, detection for sub-THz and THz radiation by rectification of plasma related nonlinearities has been demonstrated in the channels of nMOS transistors in 130-nm CMOS [37]. A 700-GHz plasma wave detector using an nMOS transistor with width and length of 10 and 0.3 μm has been reported [38]. The responsivity is greater than 200 V/W. Fig. 22 shows the minimum power of signal with 1-Hz bandwidth that can be detected (noise equivalent power, NEP) is around 100 pW. For gate voltages between 0.3 and 0.8 V, NEP decreases with decreasing gate voltage because the responsivity increases more rapidly than the increase of noise. Below 0.3 V, the rapid increases of channel resistance and noise cause NEP to increase. NEP also decreases with increasing channel length because of an increase of responsivity that saturates around gate length of 300 nm. These results qualify the Si-CMOS detectors as one of the most sensitive room temperature THz detectors. This type of detectors has been used to demonstrate a focal plane array for terahertz detection and imaging [39], and can also be used in other sub-millimeter wave systems.

VII. Challenges in the Paths to THz CMOS Circuits and Systems

Using a mainstream foundry logic CMOS process to fabricate signal generators and detectors that operate at high millimeter wave and sub-millimeter wave frequencies appears to be possible. This however, is just a start. Whether CMOS circuits are capable of supporting practical sub-millimeter wave/terahertz systems must be investigated. As a matter of fact, with the support from Semiconductor Research Corporation, Texas Analog Center of Excellence at University of Texas, Dallas is investigating the feasibility of implementing CMOS circuits for a 180–300 GHz spectrometer for home use that can detect many of the harmful molecules on the Environmental Protection Agency list. The spectrometer could also be used

in breath analyses for diagnostics of diseases [40], [41]. Such applications have the potential for requiring a moderate volume.

For these applications, presently the output power of CMOS circuits is too low. This is fundamentally limited by the low transistor breakdown voltage and insufficient $f_{\max}$ especially due to the loss associated in the parasitic capacitors, low Q of varactors, and loss of metal lines resulting from their thicknesses being low, as well as the low inter-level dielectric layer thicknesses that limit the usable metal widths. The thin dielectric layer also limits the antenna efficiency. Tuning range is low, which is due to the operating frequency of circuits being too close to $f_{\max}$ or the insufficient $f_{\max}$, and the parasitics of interconnect capacitances.

The substrate losses associated with the transistors, varactors and metal lines are complicated by the fact that the plasma frequencies of doped silicon are near the operating frequency. For instance, the plasma frequency of a p-type silicon substrate with 9-Ω-cm resistivity is 480 GHz, while that for a p-type silicon substrate with 1-Ω-cm resistivity is 1.75 THz [42]. These will increase losses and the substrate model must be augmented.

The noise performance of transistors and diodes are not well understood and characterized. At room temperature, the thermal noise starts to deviate from its white nature at operating frequency of ~ 1 THz or higher [43]. The thermal noise power spectral density $[\mathrm{V}^2/\mathrm{Hz}]$ is

$$\begin{aligned} P_v(f) &= 2R\left[\frac{h|f|}{2} + \frac{h|f|}{e^{h|f|/(kT)}-1}\right], \\ R &= \text{value of the physical resistor (ohms)} \\ h &= 6.2\times 10^{-34}\,\mathrm{J-sec} \text{ is Planck's constant} \\ k &= 1.38\times 10^{-23}\,\frac{\mathrm{J}}{\mathrm{K}} \text{ is Boltzmann's constant} \\ T &= \text{the absolute temperature of the resistor (Kelvin).} \end{aligned} \tag{1}$$

The flicker noise of Schottky diodes has not been properly quantified. Preliminary measurements suggest that the corner frequency is ~ 4 MHz.

The technology scaling should alleviate some of theses. According to the 2008 *ITRS*, by 2016, the required f_{T} and $f_{\max}$ of nMOS transistors in production are 520 and 670 GHz [5]. The same for SiGe HBT transistors are 430 and 460 GHz. SiGe HBT circuits deliver higher output power due to higher supply voltage. However, it is unlikely that the problems with dielectric and metal layers having inadequate thicknesses will be mitigated with the digital technology scaling. Most likely, either the back-end process should be modified or post foundry fabrication steps should be used to address these problems. Approaches to reduce 1/f noise in Schottky diodes including using a guard ring, dynamic diode biasing, as well as process optimization should be investigated. Lastly, a moderate volume application that can drive the CMOS terahertz circuit development must be identified and nurtured.

VIII. Conclusion

Feasibility of using a mainstream foundry logic CMOS process to fabricate signal generators and detectors that operate at high millimeter wave and sub-millimeter wave frequencies has been demonstrated. This however is just the beginning and numerous technical challenges need to be overcome before a practical CMOS sub-millimeter/terahertz system is realized. Given the potentially important safety, security and healthcare applications and technical challenges, the terahertz CMOS is a new exciting research opportunity for the silicon integrated circuits community.

Acknowledgment

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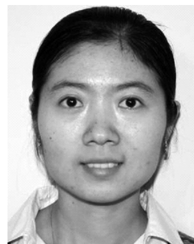

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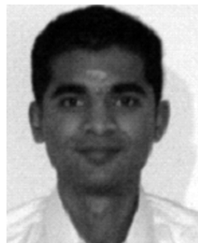

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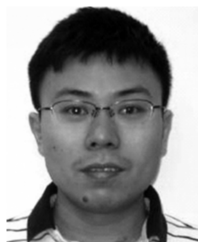

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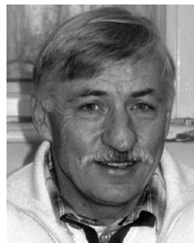

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