A 280-GHz Schottky Diode Detector in 130-nm Digital CMOS

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***Abstract*—A 2 × 2 array of 280-GHz Schottky-barrier diode detectors with an on-chip patch antenna (255× 250 μm^2) is fabricated in a 130-nm logic CMOS process. The series resistance of diode is minimized using poly-gate separation (PGS), and exhibits a cut-off frequency of 2 THz. Each detector unit can detect an incident carrier with 100-Hz ∼ 2-MHz amplitude modulation. At 1-MHz modulation frequency, the estimated voltage responsivity and noise equivalent power (NEP) of the detector unit are 250 V/W and 33 pW/Hz$^{1/2}$, respectively. An integrated low-noise amplifier further boosts the responsivity to 80 kV/W. At supply voltage of 1.2 V, the entire chip consumes 1.6 mW. The array occupies 1.5× 0.8 mm^2. A set of millimeter-wave images with a signal-noise ratio of 48 dB is formed using the detector. These suggest potential utility of Schottky diode detectors fabricated in CMOS for millimeter wave and sub-millimeter wave imaging.**

***Index Terms*—CMOS, detector, imaging, NEP, on-chip patch antenna, responsivity, Schottky barrier diode, terahertz.**

I. Introduction

RESEARCH at the terahertz frequency range (100 GHz–10 THz) of electromagnetic spectrum has been active for potential applications in imaging including that for concealed weapon detection, aviation assistance and cancer detection, spectroscopy, short range radar, secured high-speed data communication, and others [1]–[3]. For all these applications, a detector is a fundamental building block. THz detectors fabricated in CMOS for imaging in particular have received a great deal of attention for their potential for low cost, high yield and excellent capability of integration with other signal processing circuits. Based on the Dyakonov-Shur plasma wave detection theory [4], the first sub-THz silicon FET detector was demonstrated in 2004 by Knap *et al.* [5], [6]. The first focal plane FET detector array (3 × 5 pixels) in 0.25 μm CMOS was reported for imaging at 650 GHz by Lisauskas and Öjefors *et al.* in 2009 [7], [8]. More recently, a FET detector fabricated in a 65-nm SOI CMOS technology using high resistivity substrates was reported to achieve an NEP (Noise Equivalent Power) of 50 pW/Hz$^{1/2}$ at 650 GHz [9].

For their high speed and fabrication simplicity, Schottky barrier diodes (SBDs) have been used to implement an RF detector for the past century and continue to play an important role. Excellent NEP performance for III-V semiconductor SBD has been reported (20 pW/Hz$^{1/2}$ at 800 GHz [10] and 1.4 pW/Hz$^{1/2}$ at 100 GHz [11]). By using interband tunneling, a heterojunction backward diode presented in [12] demonstrated 49.7 kV/W responsivity and 0.18 pW/Hz$^{1/2}$ NEP at 94 GHz. It was reported in 2005 that a Shallow Trench Separated (STS) Schottky barrier diode with 1.5-THz cut-off frequency could be fabricated in foundry 130-nm digital CMOS without any process modifications [13]. Using this device structure, a millimeter-wave detector [14] and a frequency doubler [15] were demonstrated, but the noise performance and responsivity of the detector were not characterized. The cut-off frequency is increased to above 2-THz employing Polysilicon-Gate Separated (PGS) Schottky diodes [16], [17] in the same 130-nm CMOS. Using these diodes, a 280-GHz detector has been demonstrated [18], however the measured responsivity fluctuates significantly with frequencies, and the peak value is over three times smaller than that in the simulation. To better understand these, the detector was characterized with a higher power source (29 mW compared with 82 μW in [18]) that allowed measurements at larger source-to-detector separation with reduced standing wave effects. The measured total responsivity increases to 80 kV/W (or 250 V/W without on-chip amplification) which matches the simulation well. In combination with this and using higher modulation frequency (1 MHz compared with 25 kHz in [18]), this paper reports single cell NEP of 33 pW/Hz$^{1/2}$.

In Section II, Schottky diode and detection using the diode are presented. Section III discusses the diode detector design. The measurements including responsivity and noise performance as well as images formed with the detector are presented in Section IV. Finally, conclusions including comparisons to previously reported detectors are discussed in Section V.

II. Schottky Diode and Square-Law Detection

A PGS SBD in digital foundry CMOS was first reported in 2009 [16]. Its unit-cell cross section and top view are shown in Fig. 1. A polysilicon gate is used to separate the anode and cathode. Compared to STS SBD, the current path between the Schottky junction and n^+ cathode region in a PGS Schottky diode is shorter. Therefore for a 16-unit-cell test structure, the

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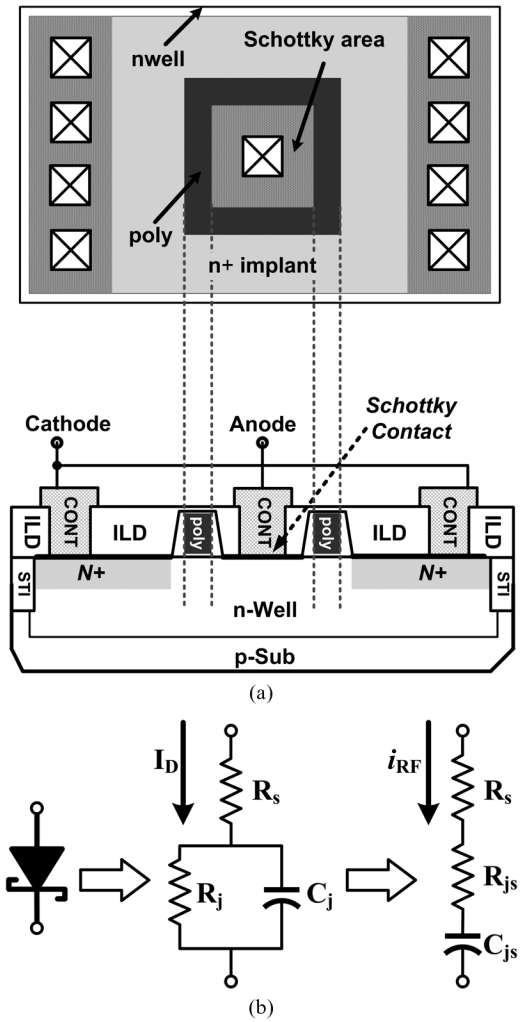


Fig. 1. Poly-Gate-Separated Schottky-barrier diode in 130-nm CMOS process: (a) cross section and top view (b) simplified model of a biased diode. The figures in (a) are not drawn to scale. R_s and C_j are the series resistance and junction capacitance of the diode, R_j represents the dynamic resistance $(1/g_m)$ of diode, and R_{js} and C_{js} are the equivalent series components of the diode.

series resistance, R_s (see the equivalent model in Fig. 1(b)) drops from 13 to 8 Ω. Due to the polysilicon gate to contact spacing design rule, the unit-cell Schottky area increases from 0.32×0.32 μm^2 (STS SBD) to 0.4×0.4 μm^2 (PGS SBD), which increases the junction capacitance, C_j from 8 to 10 fF. But the overall cut-off frequency, $f_{\mathrm{T}} = 1/(R_s \cdot C_j)$ increases from 1.5 to 2 THz.

When a small AC signal is applied, a Schottky diode generates DC voltage proportional to the signal power due to its second and other even order terms associated with nonlinearity. For a device with nonlinear $I-V$ relationship, $i = f(v)$, the ideal current responsivity $\Re_{i,0}$ which is the ratio between the rectified DC current Δi and the input power P_{in}, is [19]

$$\Re_{i,0} = \frac{\Delta i}{P_{in}} = \frac{f^{(2)}(v)}{2f^{(1)}(v)} \tag{1}$$

where $f^{(1)}(v)$ and $f^{(2)}(v)$ are the first and second derivatives of f(v). For Schottky diodes, $i_D = f_D(v_D) = I_s \cdot (e^{qv_D/nk_BT} - 1)$, where I_s is the diode reverse saturation current, k_B is Boltzmann's constant and n is the diode ideality factor. The measured

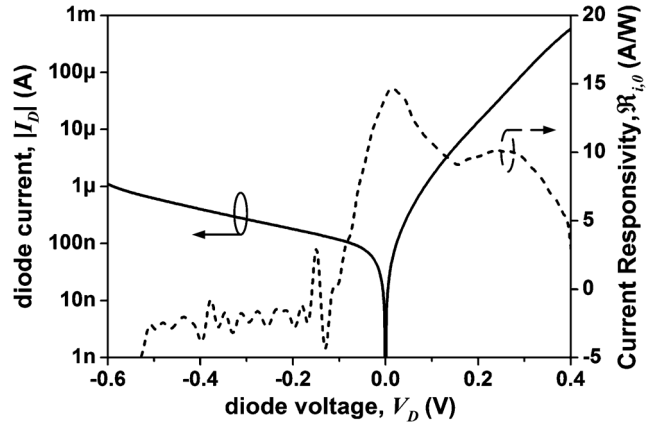


Fig. 2. Measured $I-V$ characteristic of a 16-unit-cell PGS Schottky diode (solid line), and the calculated ideal current responsivity (dashed line).

$I-V$ characteristics of the PGS SBD are shown in Fig. 2. The extracted saturation current, I_s and ideality factor, n are 50 nA and 1.35 respectively. Current responsivity extracted using (1) is also plotted in Fig. 2. For $I_D = 1$ to 100 μA, the current responsivity is on the order of 10 A/W, which is significantly larger than that of ∼2.6 mA/W for a FET-based detector [8].

The detector in this paper operates in a voltage mode, and the current responsivity can be converted into the voltage responsivity $\Re_{v,0}$, which is the product of the current responsivity $\Re_{i,0}$ and the dynamic diode junction resistance R_j ($R_j = 1/g_m = 1/f_D^{(1)}(v_D)$).

$$\begin{aligned}\Re_{v,0} &= \frac{\Delta v}{P_{in}} = \frac{\Delta i}{P_{in}} \cdot R_j = \frac{f_D^{(2)}(v_D)}{2\left[f_D^{(1)}(v_D)\right]^2} \\ &= \frac{1}{2I_s \cdot e^{\frac{qv_D}{nk_BT}}} = \frac{1}{2(I_D + I_s)}.\end{aligned} \tag{2}$$

From (2), the peak voltage responsivity occurs when diode bias current approaches zero. However, this bias condition is not used for two reasons:

(i) Due to the low reverse saturation current of the diode ($I_s = 50$ nA), junction resistance R_j at low bias level is too high (~ 700 kΩ) for efficient power matching.

(ii) High R_j forms a low-frequency pole with the load capacitance, C_L, of the detector ($f_{out,p} = 1/(2\pi R_j C_L)$), which limits the bandwidth of detector.

Because of these, the diode in this detector design is forward biased. Besides the bias current, the number of diode unit cells in shunt, namely the total diode size must be specified. Note that the previous analysis assumed that all the input RF power is absorbed by R_j, which is not true in reality due to the finite series resistance R_s and junction capacitance C_j. Based on the diode model in Fig. 1(b), the RF power transfer degradation factor ξ can be expressed as [19]

$$\begin{aligned}\xi &= \frac{P_{total} - P_j}{P_{total}} = 1 - \frac{R_{js}}{R_{js} + R_s} \\ &= 1 - \frac{R_s}{R_j + R_s + R_s^2 R_j^2 C_j^2 \omega^2 / R_s} \\ &= 1 - \frac{1}{1 + \frac{R_s}{R_j} + \frac{R_j}{R_s} \cdot \left(\frac{\omega}{\omega_T}\right)^2}\end{aligned} \tag{3}$$

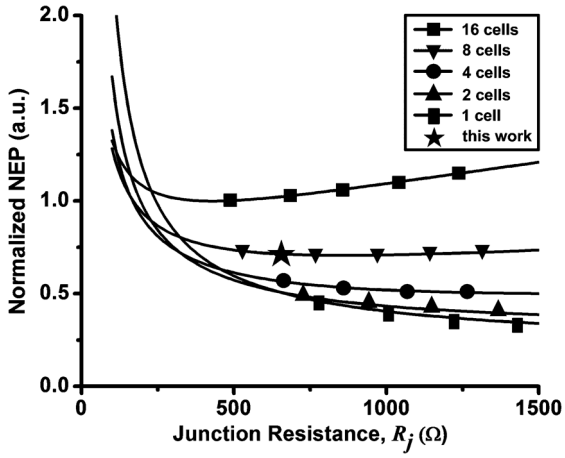


Fig. 3. Calculated NEP of detectors with different diode junction resistance R_j and the number of unit cells.

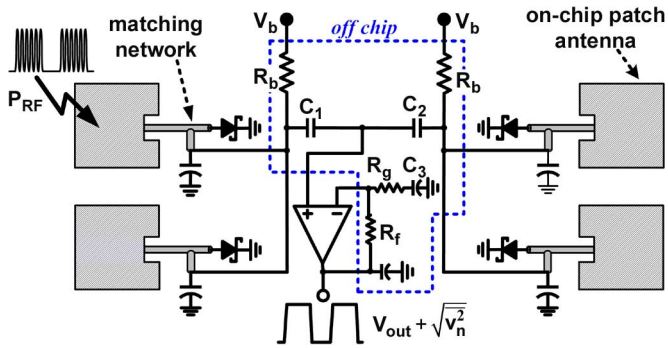


Fig. 4. Schematic of the 280-GHz Schottky diode detector.

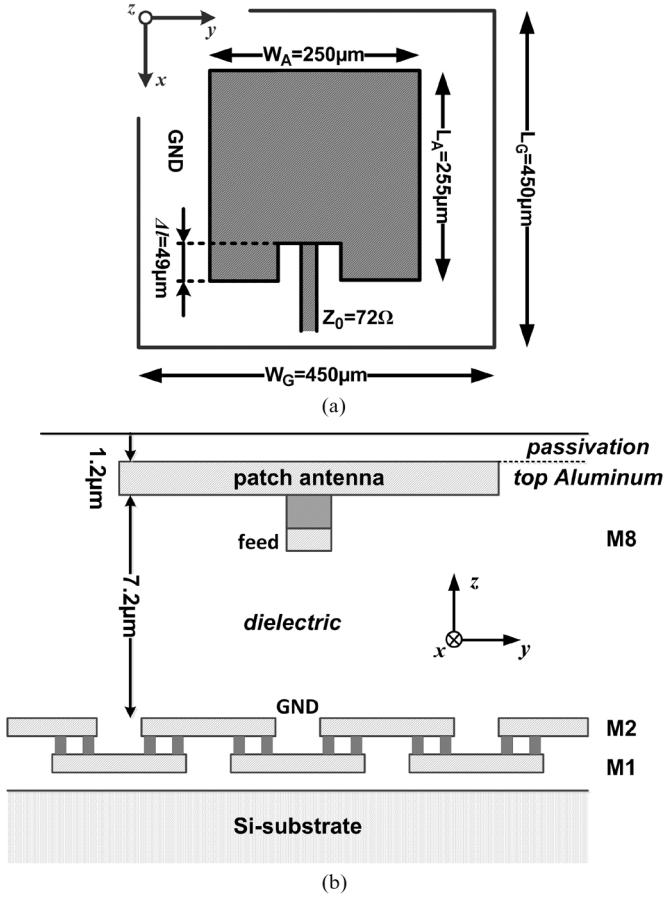


Fig. 5. (a) Top and (b) cross section views of the patch antenna. The slots in M1 and M2 layers are required by the design rules.

where P_{total} and P_j are the total input power and the power dissipated in R_j, respectively. At 280 GHz for the PGS, (3) gives a minimum responsivity drop of 22%.

Another key performance metric for the detector, Noise Equivalent Power (NEP), is defined as the input RF power level at which the detector output signal to noise ratio (SNR) is unity for 1-Hz bandwidth. Mathematically, it is the ratio between the output noise voltage spectral density $(\mathrm{V/Hz^{1/2}})$ and detector voltage responsivity. To achieve optimum NEP, the shot and flicker noise generated in diode need to be considered. The power spectrum density (PSD) [19] is

$$\overline{i_n^2}/\Delta f = \frac{4k_BTt_w}{R_j}\left(1+\frac{f_N}{f}\right) \tag{4}$$

where f_N is the flicker noise corner frequency, which is normally proportional to the bias current; and t_w is the white noise temperature ratio (the ratio between the white noise generated from the diode and that from a resistor equal to R_j), which is $n/2$ when forward bias current I_D is much larger than I_s [20]. Combining (1)–(3) and the shot noise part of (4), NEP of the diode detector with modulation frequency higher than the $1/f$ noise corner frequency is

$$NEP = \frac{R_j\cdot\sqrt{i_n^2/\Delta f}}{R_j\cdot\Re_{i,0}\cdot(1-\xi)} \approx \frac{4nt_w^{1/2}\cdot(k_BT)^{3/2}}{q}\cdot\frac{1+\frac{R_s}{R_j}+\frac{R_j}{R_s}\left(\frac{\omega}{\omega_T}\right)^2}{R_j^{1/2}}. \tag{5}$$

R_s and C_j scale inversely and linearly with the number of unit cells. A set of NEP plots based on (5) are plotted in Fig. 3.

The scalability of PGS SBD model, which is based on measurements of a 16 unit-cell test structure, is questionable. As a smaller number of unit cells is chosen, the diode impedance becomes more susceptible to any possible interconnect parasitics. For instance, if a single cell diode with scaled C_j of 0.63 fF is chosen, simulations indicate that a 1 fF interconnect parasitic shunt capacitance could result in a reflection loss of -5 dB. As a compromise, the unit cell number of 8 that results around the median NEP is chosen for the design, though Fig. 3 indicates that fewer diode cells lead to lower NEP. Additionally, Fig. 3 also shows that NEP does not change significantly once the junction resistance increases above 500 Ω, so the dynamic diode junction resistance is chosen to be 600–700 Ω, which requires a bias current of $\sim$ 50 μA.

III. 280-GHz Diode Detector Design

A schematic of the diode detector is shown in Fig. 4. Four detector cells are fabricated on the same die. It will be shown in Section III-C of this section that for uniformly-distributed radiation power density, combining the outputs of four cells could increase the signal to noise ratio (SNR) of image by 6 dB. In general, each detector cell collects the radiation signal at 280 GHz through one on-chip patch antenna, and then rectifies the signal using the diode square-law detection discussed earlier to generate the baseband signal. Similar to other radiation detectors,

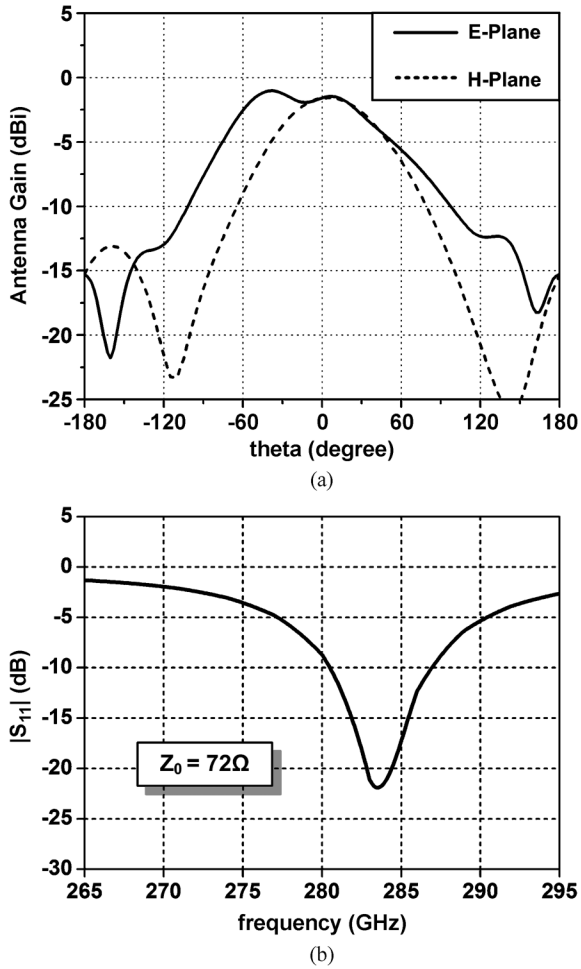


Fig. 6. Simulated (a) antenna gain in different directions and (b) reflection coefficient of the patch antenna versus frequency ($Z_o = 72\ \Omega$).

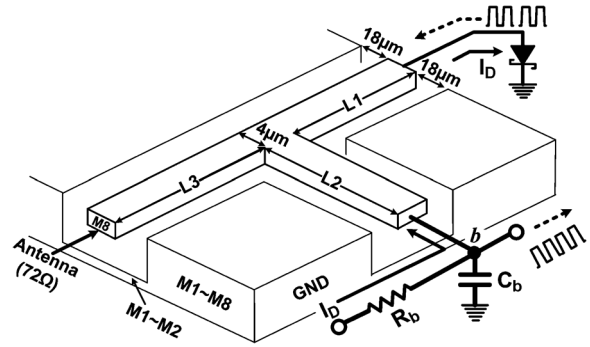


Fig. 7. Matching network between the on-chip antenna and Schottky diode that uses GCPW transmission lines. The length of three sections in the figure are $L_1 = 38\ \mu$m, $L_2 = 44\ \mu$m and $L_3 = 38\ \mu$m.

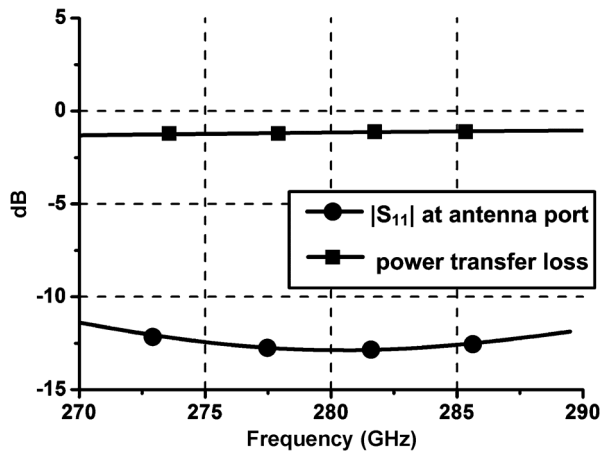


Fig. 8. HFSS-simulated reflection coefficient and power transfer loss of the matching network.

this diode detector requires the radiation source to be amplitude modulated at frequency f_m. This way, the output of detector would also be located at f_m, instead of at DC, where the circuit is susceptible to flicker noise and drift. In addition, a low-noise preamplifier is also included on-chip to amplify the detected signal without significantly degrading the noise performance. The outputs of two detector cells on each side are made to share one bond pad to reduce the chip area. The diodes are biased through on-board resistor R_b (10 kΩ), and the AC coupling capacitors $C_1 \sim C_3$ are not integrated for their large value ($\sim 1\ \mu$F). Since the Schottky diode has already been described in detail, only the design of other major components of the detector is discussed in the following sections.

A. On-Chip Antenna

The radiated signal is picked up by an on-chip patch antenna with a size of $255 \times 250\ \mu$m^2. The antenna is made of the top Aluminum layer (shown in Fig. 5). Metal 1 and Metal 2 layers are shunted together to form the ground plane ($450 \times 450\ \mu$m^2), so that the EM wave is reflected back to free space instead of propagating through the lossy silicon substrate. The dielectric layer that separates the patch and ground plane is SiO_2 with 7.2-μm thickness. The slots in Metal 1 are covered over using Metal 2 (Fig. 5(b)). The antenna performance is simulated in the full-wave 3-D simulator, HFSS. The other three antennas with proper port termination are also included in the simulation to account the aperture overlap effect [8]. The size of the ground plane in the simulation is also the same as the real chip area. Fig. 6 shows the simulation results. The simulated peak directivity and gain of each antenna are 5.1 dBi and -1.6 dBi, respectively for antenna efficiency of 21%. The low efficiency is due to the thin dielectric layer between the patch and ground limited by the metallization of the CMOS process as well as the conductor loss. The aperture size calculated from the directivity is 0.29 mm^2. The simulated resonant impedance on the edge of patch is 108 Ω. This high resistance narrows the feed line width and increases loss. An inset in Fig. 5(a) is used to lower the antenna impedance to 72 Ω [21]. The simulated antenna -10 dB impedance bandwidth is 7 GHz.

B. Matching Network

A forward-biased Schottky diode has complex impedance. To improve power transfer efficiency, a short-stub matching network is inserted between the antenna and the diode using Grounded CPW (GCPW) transmission lines (Fig. 7) [15], [22]. To match to the antenna port, the characteristic impedance of the line is also chosen to be 72 Ω. A multi-finger metal capacitor C_b connected to node "b" presents high impedance to DC bias and baseband signal, while shorting the 280-GHz signal to

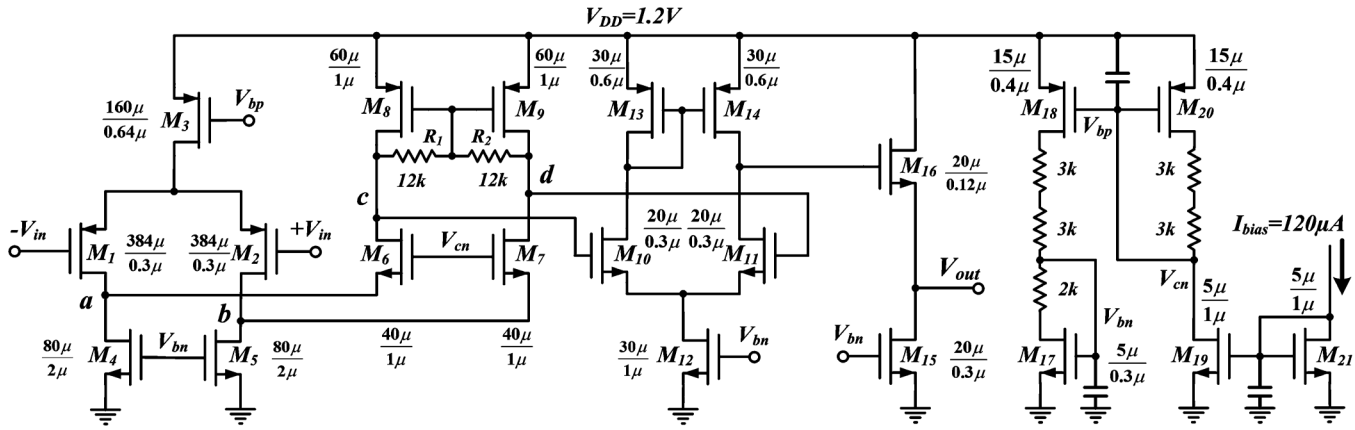


Fig. 9. Schematic of the low-noise preamplifier.

ground. Since the detector performance is not sensitive to the parasitic capacitance on node "b", the diode bias current is injected and the down-converted output signal Δv is extracted from this node. The HFSS simulation indicates that the bandwidth of matching network is over 20 GHz and the loss is about 1.2 dB (Fig. 8).

C. Output Combining

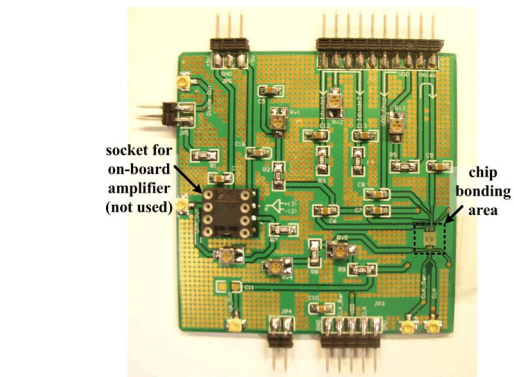
As mentioned earlier, the outputs of detector cells could be combined in shunt. The benefit of such configuration is the reduced output noise voltage. The expression of noise current from each detector was given in (4). If m diode detectors are connected in parallel, the total noise current power, $(\overline{i_n^2})_{total}$, will be increased by a factor of m.

$$\left(\overline{i_n^2}\right)_{total} = \sum_{k=1}^{m} \left(\overline{i_n^2}\right)_k = m \cdot \frac{4k_B T t_w}{R_j}\left(1 + \frac{f_N}{f}\right)\Delta f. \quad (6)$$

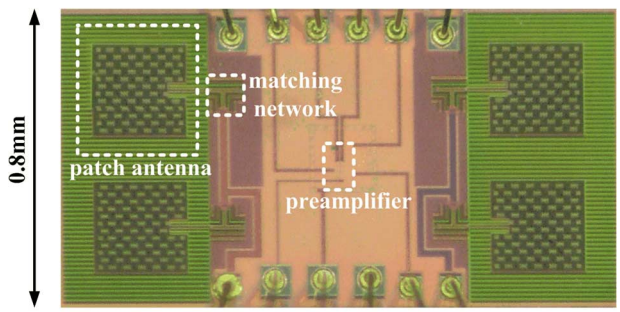
In contrast, the total noise voltage power at the output is decreased by a factor of m.

$$\left(\overline{v_n^2}\right)_{total} = \left(\overline{i_n^2}\right)_{total} \cdot R_{total}^2 = \left[m\frac{4k_B T t_w}{R_j}\left(1 + \frac{f_N}{f}\right)\Delta f\right]\left(\frac{R_j}{m}\right)^2 = \frac{\overline{v_n^2}}{m}. \quad (7)$$

For many applications, the radiation power density over the detector (rather than the total power) is fixed. Even in imaging applications in which a beam is focused on a detector, the spot size is still normally several times larger than a single antenna size [23] due to the Gaussian distribution property of the beam [24]. The output signal level does not change in a parallel configuration, so the SNR increases by a factor of m (or 6 dB for four cells). This however decreases the voltage responsivity by a factor of m. Since the output noise voltage amplitude in (7) decreases by $m^{1/2}$ times, the overall NEP, which is the noise voltage divided by the voltage responsivity increases by a factor of $m^{1/2}$. But such output combining is still desirable in many situations because of higher SNR. For example, such configuration could be used to reduce the exposure time of each pixel with given SNR by four times, hence reducing the time required to form an image.



(a)



(b)

Fig. 10. Die photo of the 280-GHz CMOS SBD detector after mounting on a printed circuit board.

D. Preamplifier

A preamplifier is included on chip and is shared among the four detector cells. The amplifier consists of three stages (Fig. 9). The first stage uses folded configuration, and has a common-centroid PMOS input pair (M_1 and M_2) to reduce the input referred flicker noise and offset. Also, M_4 and M_5 have a large channel length (2 μm) to reduce their flicker noise contribution. Their large parasitic drain capacitance does not result in an unacceptably large time constant due to the low impedance at nodes "a" and "b". A pure resistive load may achieve better noise performance [25], but the large DC voltage drop across the resistors is not practical in this low-V_{DD} circuit.

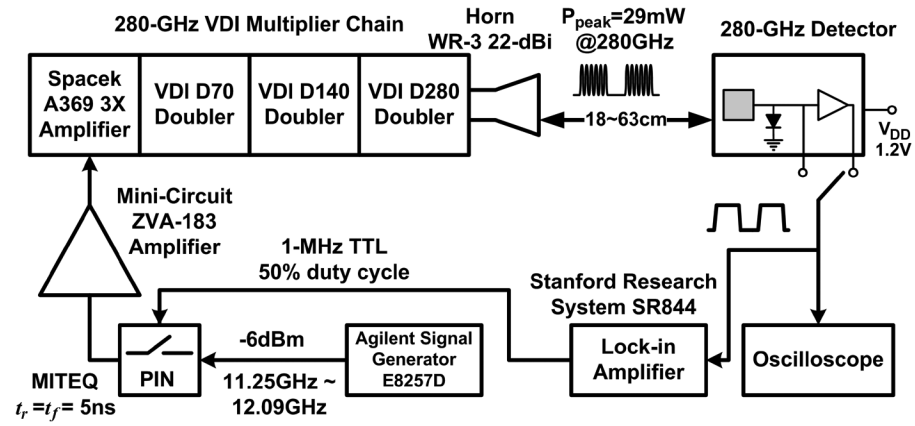


Fig. 11. 280-GHz detector responsivity measurement set-up.

The simulated flicker noise corner frequency and white noise level of the amplifier are 100 kHz and 3 nV/Hz$^{1/2}$ respectively. Resistors R_1 and R_2 not only provide the common-mode feedback, but also lower the time constant on nodes "c" and "d". M_{10}~M_{14} turn differential signals into single-ended and further boost the gain. Finally, a source follower formed with M_{16} provides sufficient driving capability for the capacitive load of instrument input. Transistors M_{17}~M_{21} form a bias network. The amplifier provides 50-dB voltage gain with 2-MHz 3-dB bandwidth with an external resistive feedback, which also establishes the DC operating point for the amplifier. The power consumption of amplifier is 1.3 mW at 1.2-V supply voltage.

IV. Measurement Results

The detector is fabricated in the UMC 130-nm logic CMOS process. The chip area is 1.5×0.8 mm^2. Its die photo and the printed circuit board (PCB) for testing are shown in Fig. 10. The responsivity of detector is measured using the set-up shown in Fig. 11. An input signal of 11.25 GHz ~ 12.09 GHz is fed into a VDI Amplifier/Multiplier Chain (AMC) to generate 270 GHz ~290 GHz radiation signal. Linearly-polarized RF signal is radiated through a WR-3 horn antenna. A lock-in amplifier, SR844 generates TTL signal up to 1 MHz that can turn on and off the PIN switch to AM-modulate the signal and at the same time measures the rms value of output voltage for the detector. The detector output is also measured by an oscilloscope and Fig. 12 shows the output waveform (detector at a distance of 38 cm from the source).

If the detector is placed too close to the radiation source (e.g. ~2 cm), significant fluctuation of the amplitude in the detector output was observed in the frequency response [18]. Such standing-wave effect may be caused by the multi-reflection between the non-absorbent detector board and the source horn. The incident wave to the detector is constructively and destructively interfered. Larger separation results in smoother detector frequency response due to increased propagation loss for multi-reflected signals. Fortunately, with the higher available radiation power (~29 mW at 280 GHz) than the one in [18], the distance between the source and PCB in the set-up in Fig. 11 could be increased sufficiently (d = 57 cm) to significantly

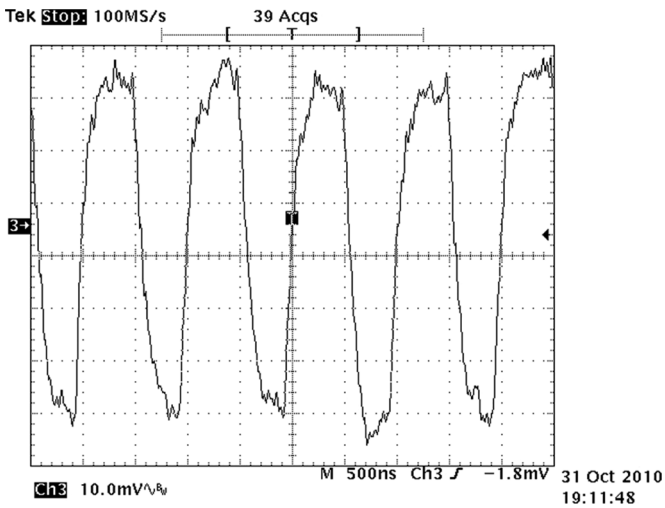


Fig. 12. Waveform at the output of the preamplifier (fRF = 280.6 GHz, fchop = 1 MHz, distance = 38 cm).

reduce the standing wave effect. The detector output at varying radiation frequencies is measured with the lock-in amplifier.

The estimation expression of the single detector unit voltage responsivity is

$$\Re_v = \frac{v_{out}}{P_{in}} = \frac{\frac{\pi}{\sqrt{2}} V_{rms}}{A_R \cdot \frac{P_{cw} \cdot G_T}{4\pi d^2}}. \tag{8}$$

The denominator of (8) is the RF power received by each detector cell, which is the product of the aperture size, A_R, of the patch antenna from the simulations discussed in Section III and the radiation power density at a distance d from the source. The power (P_{cw} in (8)) of the transmitted continuous-wave signal (without modulation) from the source at different frequencies is measured using an Erickson PM4 power meter and plotted in Fig. 13. When the carrier amplitude is modulated by a square wave with a 50% duty cycle, Fourier analysis indicates that the rms value of fundamental frequency component of the detected signal, V_{rms} measured by the lock-in amplifier should be $\pi/\sqrt{2} \approx 2.2$ times smaller than the peak-to-peak value of the

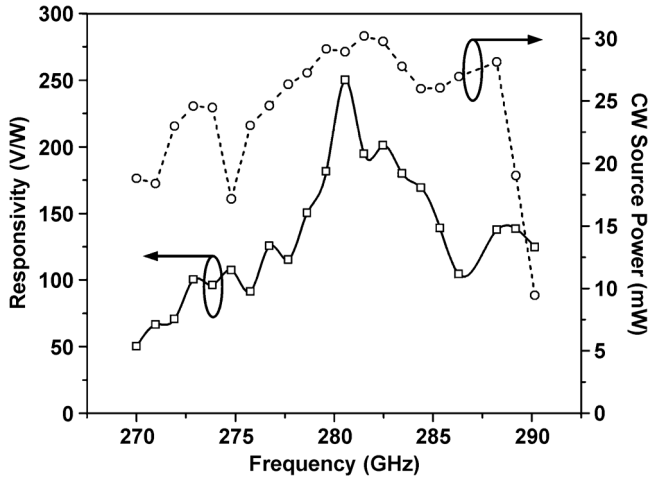


Fig. 13. (a) Single detector unit responsivity (with amplifier gain de-embedded) at varying source frequencies and (b) continuous-wave radiation power measured with a power meter.

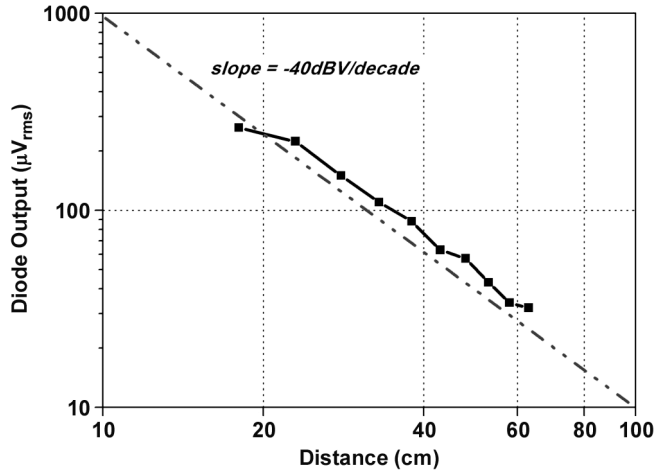


Fig. 14. The diode output voltage versus distance between the source and detector. The measurement frequency is 280.6 GHz. The slope of -40 dB/decade for the data (or -20 dB/decade for the input power) verifies the $1/d^2$ dependency expected from the Friis transmission equation [27].

square wave captured by the oscilloscope [26]. The gain of the source horn antenna, G_T, is 22 dBi.

Using (8), the voltage responsivity versus frequency is calculated and plotted also in Fig. 13 (with the 50-dB gain of the on-chip amplifier de-embedded for convenient comparison with other works). The peak responsivity 250 V/W (or 80 kV/W with on-chip amplification) is measured at 280.6 GHz, which is the resonant frequency of the patch antenna. The associated amplified detector output V_{rms} read from the lock-in amplifier is 11.9 mV, and the peak power received by the patch antenna is 0.33 μW.

The above estimation assumes that the transmission of radiation power follows the Friis Equation [27]. To verify this assumption, the detector response (without preamplifier) at varying distances (18 to 63 cm) is also characterized. The results are shown in Fig. 14. The -40 dB/decade slope within the measurement distance range indicates that (8) is valid. The data are also consistent with prior measurements (Fig. 12 with $d = 38$ cm and Fig. 13 with $d = 57$ cm).

In addition, Fig. 15 plots both the measurement and simulation results of responsivity at varying diode DC current. Two curves fit well and give the same optimum bias point ($\sim 50\,\mu$A) for the peak responsivity. Power matching is most efficient at this peak point and (2) explains the rapid drop of the curve beyond the peak.

To determine the noise equivalent power (NEP) of the detector, the output noise of the detectors with and without the amplification of the on-chip amplifier is amplified by an external low-noise amplifier (EG&G Model 5184, 0.8 nV/Hz$^{1/2}$ input referred noise, 60-dB gain), and measured by an Agilent 89410 A vector signal analyzer. The noise power spectral density (PSD) of the detector is plotted in Fig. 16. The average noise voltage difference between two diodes in shunt and four in shunt is about 3 dB, which is consistent to (7). The $1/f$ noise corner frequency is around 4 MHz, which is unfortunately still larger than the maximum modulation frequency

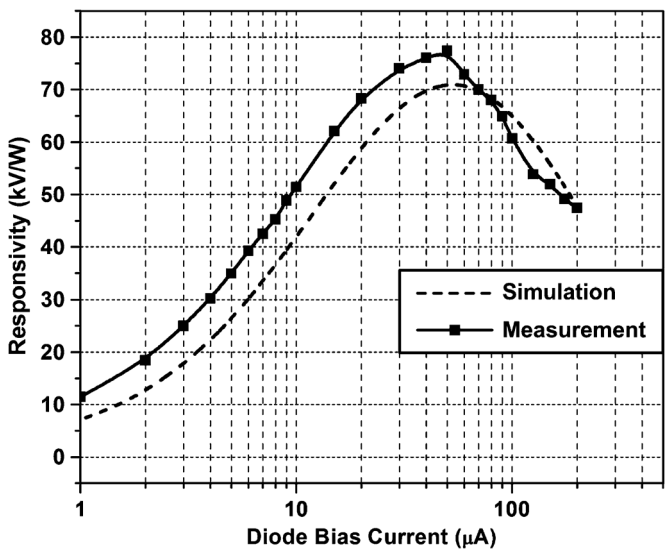


Fig. 15. Simulation and measurement results of the single detector unit responsivity (with amplifier) versus diode bias current at 280.6 GHz input frequency.

(1 MHz) capability of the setup in Fig. 11. At 1 MHz, the output noise voltage of four detector cells is 4.1 nV/Hz$^{1/2}$. So each detector cell generates $\sim$8.2 nV/Hz$^{1/2}$ noise. Based on the measured responsivity and noise data, the NEP of four and two detector combinations at 1-MHz modulation frequency are 66 pW/Hz$^{1/2}$ and 42 pW/Hz$^{1/2}$, and the estimated NEP for a single cell is 33 pW/Hz$^{1/2}$. When the on-chip amplifier is included, the NEP increases by approximately 10% to 73 pW/Hz$^{1/2}$ and 47 pW/Hz$^{1/2}$ for four and two detector combinations. Given that the simulated input referred noise of the amplifier at 1 MHz is 3 nV/Hz$^{1/2}$, the NEP of one detector cascaded by the amplifier is estimated to be 36 pW/Hz$^{1/2}$. Fig. 16 also indicates that the NEP of the detector (without amplifier) is expected to further drop to 20 pW/Hz$^{1/2}$, if the modulation frequency is increased beyond the flicker noise

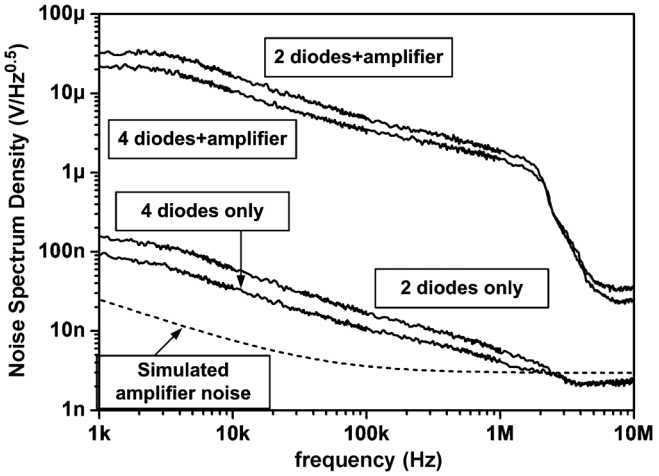


Fig. 16. Measured output noise voltage power spectrum density of the detector, with and without the on-chip amplifier. The bandwidth of the amplifier is 2 MHz. Simulated input referred noise of the amplifier is also plotted.

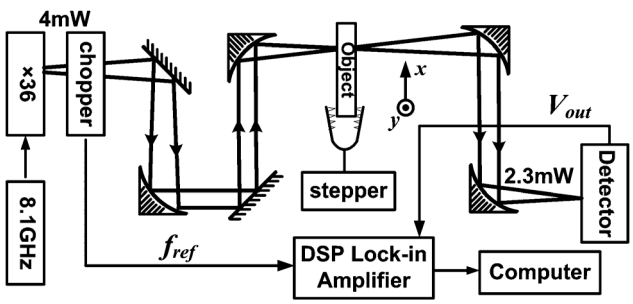


Fig. 17. Block diagram of the THz imaging system.

corner frequency of 4 MHz; and the performance starts to be limited by the noise and bandwidth of the preamplifier.

Lastly, the 280-GHz Schottky diode detector was integrated into a 2-D focal-plane image scanner at the Université Montpellier 2, France (shown in Fig. 17). The power radiated from the source (different from the one in Fig. 11) is 4 mW, and the power delivered to the detector is 2.3 mW. The lowest frequency provided by the source is 292 GHz, at which the responsivity of the detector degrades significantly (Fig. 13). Moreover, the mechanical chopper frequency of the set-up is only 340 Hz, at which the detector suffers from a high level of flicker noise (Fig. 16). Despite these, the detector is still able to form images with an SNR of 48 dB. The SNR here is defined as the ratio of quantized lock-in amplifier outputs when the detector is illuminated by the source without an object in the beam line and when the beam is blocked by a thick metal layer. Fig. 18 shows some of these images. The scanned area over the objects is 70×70 mm^2 divided into 175×175 pixels. It takes around 20 minutes to scan each image. Each pixel takes 40 ms of measurement time of which mechanical motion consumes 30 ms. Since the actual electronic sampling time for noise averaging is only 10 ms, an array of detectors may also be used to construct a video-rate millimeter-wave camera. Lastly, the sampling time could be greatly reduced by optimizing the radiation and modulation frequencies.

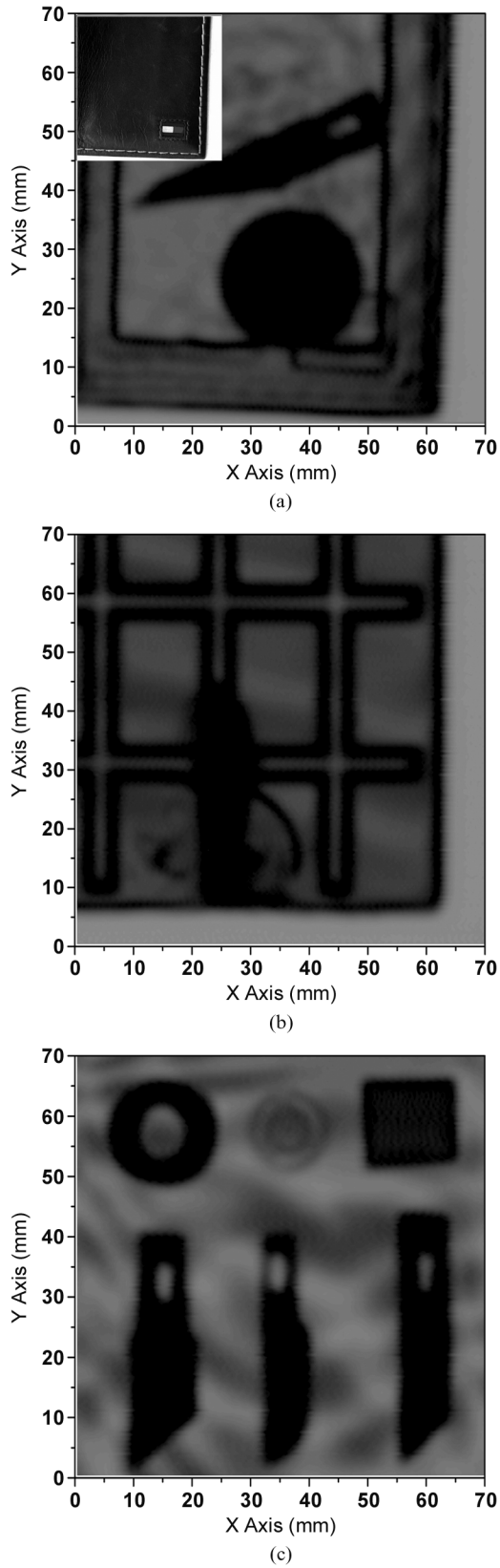


Fig. 18. Three THz images formed using the diode detector at 292 GHz: (a) a coin and a blade hidden inside a leather wallet; (b) a blade hidden inside a chocolate bar; (c) metal and plastic rings, rubber and three blades in a shipping envelope. The bright and dark interference fringes are due to the etalon effect resulting from the reflection between two surfaces of structure that encloses the imaged objects [23].

TABLE I
SUMMARY OF DETECTOR PERFORMANCE AND COMPARISON WITH PRIOR WORKS

Technology			NEP [pW/Hz$^{1/2}$]	[kV/W]	Freq. [THz]	Monolithic Integration	Reference
SBD	130-nm logic CMOS[1]	4 detectors in shunt	66† 73††	0.063† 20††	0.28	yes	This Work
		2 detectors in shunt	42† 47††	0.125† 40††			
		single detector[2]	33† 36††	0.25† 80††			
	GaAs		20 1.5	0.4† 3.8†	0.8 0.15	no	[10]
	ErAs/InAlGaAs		1.4	6.8†	0.1	no	[11]
Heterojunction Backward Diode	InAs/AlSb/$Al_{0.12}Ga_{0.88}Sb$		0.18	49.7	0.094	no	[12]
MOSFET[3]	Silicon		100†	0.033†	0.7	yes	[6]
	250-nm CMOS		300††	80††	0.65	yes	[8]
	65-nm SOI CMOS		50†	1.1† 72††	0.65	yes	[9]
Golay Cell	--		200-400	0.1-45	0.2-30	no	[28]
Pyroelectric	--		400	150††	0.1-30	no	[29]

†without amplifier ††with amplifier

Note:

1. Simulated antenna pattern and aperture size (larger than the detector physical size) are used in (8) to estimate NEP and $\Re_v$.
2. The single detector NEP data is based on measured noise floor of two and four detectors in shunt, and calculation using Equation (7).
3. The peak responsivity and minimum NEP in [6], [8] and [9] don't occur at the same bias point.

V. CONCLUSIONS

This paper has shown that bulk CMOS-compatible Schottky barrier diodes can be used to detect millimeter-wave and potentially THz radiation. The performance of detector is summarized in Table I and compared to those of other room temperature THz detectors. Because of the differences in the tuned frequency, it is difficult to make a clean comparison. However, the NEP of Schottky diode detector is better than that of Golay cells and Pyroelectric detectors around 300 GHz. After de-embedding the on-chip antenna and matching network loss ($\sim$8 dB), the estimated intrinsic NEP of the 8-cell PGS SBD in 130-nm CMOS at 280-GHz RF frequency and 4 MHz modulation frequency is 3.2 pW/Hz$^{1/2}$, which is only 2$\times$ larger than that of the waveguide-fed GaAs SBD in [10] at 150 GHz. There are also several potential reasons to expect the NEP of Schottky diode detector to be lower than that of NMOS detectors including the higher current responsivity due to stronger nonlinearity of the SBD. The current power spectral density of shot noise for NMOS transistors biased in sub-threshold region of operation with $V_{DS} = 0$ is $4k_BTg_{ds}$ [30] compared to $2nk_BTg_m$ of the SBD. Lastly, the capacitance of NMOS detector structures is mostly related to gate oxide capacitance while that for the SBD detectors is related to junction capacitance. These capacitances are highly bias dependent and more work is needed to understand how they contribute to the difference of responsivity and NEP for the NMOS and SBD detectors. Simulations suggest that at 600 GHz the degradation factor, ξ of this high-f_{T} diode only increases to 38% from 22% at 280 GHz, the loss of the matching network increases to 1.7 dB, while simulated efficiency of the patch antenna at 600 GHz (size: 126×124 μm^2) improves from 21% to 50%. Because of these, the performance of diode detector should remain almost the same at 600 GHz and could be better than that of the NMOS detectors [6], [8] including that fabricated using 65-nm CMOS on a high resistivity substrate [9]. Given that the cut-off frequency of PGS SBDs is 2 THz, detectors operating at frequencies higher than 1 THz should be possible in the 130-nm CMOS process. Lastly, the transmission imaging configuration described in this paper can be used to image hidden defects, to monitor moisture contents during paper production, to inspect envelops for dangerous contents, as well as others.

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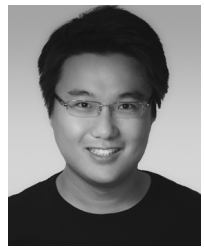

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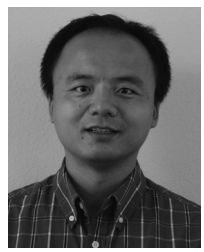

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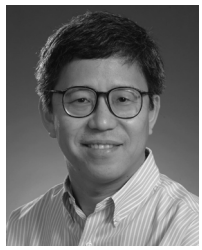

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