15.2 280GHz and 860GHz Image Sensors Using Schottky-Barrier Diodes in 0.13μm Digital CMOS

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Millimeter and sub-millimeter-wave imaging using solid-state circuits is gaining attention for security and medical applications. To lower cost and increase integration, MOSFETs in CMOS are being investigated for implementing broadband detectors [1-3]. However, neither measured noise-equivalent power (NEP) nor noise floor of the imager was given in [1]. Although NEP of 17pW/Hz$^{1/2}$ was achieved at 650GHz in [2], an external lens was attached to the 65nm SOI CMOS chip. In [3], an NEP of 66pW/Hz$^{1/2}$ was measured at 1.05THz using 65nm CMOS without a lens attached to the chip. Additionally, although the efforts reported in [1-3] realized an array, none demonstrated the image-array function. As an alternative, polysilicon-gate-separation (PGS) Schottky-barrier diodes (SBD) with cut-off frequency of ~2THz were fabricated in CMOS without process modifications [4] and were used to demonstrate a 280GHz detector with NEP of 30pW/Hz$^{1/2}$ [5,6]. To significantly enhance the scanning speed, a 16-pixel 280GHz SBD imager is fabricated and its array function is reported in this paper. The imager including baseband amplifiers achieves responsivity of 5.1kV/W and NEP of 29pW/Hz$^{1/2}$. More importantly, its operation was demonstrated in a setup that requires no mirror or lens that is bulky and costly. Next, an 860GHz SBD detector is demonstrated with a measured non-amplified responsivity of 355V/W and NEP of 32pW/Hz$^{1/2}$. This NEP is ~2X lower than the best reported work in CMOS [3]. Both chips are fabricated in a 0.13μm logic CMOS. The results suggest a path for high performance, compact and affordable sub-millimeter-wave and terahertz CMOS imagers using SBDs.

Figure 15.2.1 shows the proposed imager architecture, which includes a 4×4 SBD pixel array, bias-distribution circuitry, a reconfigurable readout amplifier array, as well as address/control multiplexers. Unlike the active-pixel array with an in-pixel amplifier in [1], a passive pixel array is chosen for the following reasons. First, the SBD in this work is forward-biased (I_D=50μA) and exhibits lower dynamic resistance (R_d=1/g_m=~600Ω), so in the presence of potentially large bus interconnect capacitances, the bandwidth is higher than that of MOSFET detectors biased at 0V [1] or in the subthreshold region [2]. Secondly, the 1/f noise corner frequency of forward-biased SBDs in CMOS is high (2 to 4MHz), while the absolute noise level is low (8.2nV/Hz$^{1/2}$ at 1MHz) [6]. Accordingly, large power consumption and area for the amplifier are needed to mitigate the degradation of NEP by the amplifier noise. Thirdly, the passive-pixel architecture requires only one interconnect for each row (bias and signal) and column (address control), which provides a good fill factor and scalability.

A schematic of a 280GHz SBD pixel and the PGS SBD unit structure are shown in Fig. 15.2.2. A $CoSi_2$ contact on an n-type silicon diffusion forms a Schottky junction. The series resistance is reduced (8Ω for 16 cells) by the 0.12μm polygate ring separation. Each diode consists of eight 0.4×0.4μm^2 shunted cells. Signals are picked up by a 250×255μm^2 patch antenna formed using the ~1.5μm thick aluminum bond pad layer. The antenna ground is placed under (Metal1-Metal2) and also around the patch antenna (Metal1-Metal8) and isolates the bus lines. The HFSS simulated directivity of the patch antenna is 6.7dBi and radiation efficiency is 29%. A short-stub GCPW transmission-line matching network is inserted for effective power transfer from the antenna to the diode. The short termination of the matching network is implemented by a metal capacitor, C_{ij}, which also presents open to low-frequency rectified signals. The bias/signal connection of each pixel is controlled by an NMOS switch (30μm/0.12μm), which has only 15Ω on-resistance compared to 600Ω diode dynamic resistance to ensure a small switch noise contribution. The switch parasitics have little effect on RF detection because C_{ij} is an AC short at RF.

Imager pixel performance uniformity is critical to lower fixed-pattern noise. Because the diode intrinsic responsivity, noise level and impedance are determined by the current, current-mode bias distribution is adopted (Fig. 15.2.1). A reference current is duplicated at each row, and is then locally mirrored to bias a selected diode. To attenuate the transistor noise injection into the diodes, 12kΩ polysilicon resistors, R_x are inserted between the current mirrors and buses. The resistors also increase the output impedance of the bias circuitry to reduce the load on the row bus that carries the rectified signal.

The imager output can operate in either a serial low-noise mode or a parallel high-speed mode (Fig. 15.2.1). In serial mode, Analog Multiplexer (AM)-I combines and connects all the inputs of the readout amplifiers to a pixel selected by address ($\overrightarrow{C}$ $\overrightarrow{R}$), while AM-II combines the outputs of amplifiers (Out_S). This mode decreases the amplifier noise by 6dB. In parallel mode, AM-I feeds pixel signals in each row to a corresponding amplifier, thus providing multichannel outputs for a four-time higher scan rate. To avoid imager output saturation at the 30mW radiation power of a 280GHz source, the amplifier gain is set to 24dB. The amplifier consumes 1.3mW and exhibits 3dB bandwidth of 2MHz. Total power of the 280GHz SBD imager is 6mW. The pixel pitch is 500μm (λ_0/2) and the die area is 2.3×2.4mm^2.

The 860GHz pixel unit has a similar schematic to that shown in Fig. 15.2.2, but uses only four diode cells in shunt and an 82μm-wide patch antenna. Simulated antenna efficiency increases to 71%, which compensates the larger diode loss at higher operating frequency. The bias current of the diode is 20μA. The responsivity measurement setup is shown in Fig. 15.2.3. To reduce the impact of diode 1/f noise, the source is modulated at 1MHz. The voltage responsivity is estimated using the expression in Fig. 15.2.3. The continuous-wave source power, P_{cw} is measured using a VDI Erickson power meter. Measured responsivity R_v, and the output noise power-spectral density (PSD) for the 280GHz imager and 860GHz detector are plotted in Fig. 15.2.4. Peak responsivity of 5.1kV/W and 355V/W (without amplifier) are achieved at 282.5 and 860GHz, respectively. The output noise PSD of the 280GHz imager in serial mode is 150nV/Hz$^{1/2}$ at 1MHz with a corresponding NEP of 29.4pW/Hz$^{1/2}$. Given that the diode noise is 8.2nV/Hz$^{1/2}$ [6], (or 24.4pW/Hz$^{1/2}$ NEP), the rest of the imager increases NEP by only 20%. The output noise of the 860GHz detector at 1MHz is 11.1nV/Hz$^{1/2}$ with a corresponding NEP of 32pW/Hz$^{1/2}$. This is ~2X lower than that of the 1.05THz detector fabricated in 65nm CMOS [3].

The 280GHz imager is integrated in a lens-less short-range imaging setup with an MSP430 launchpad for multiplex-sampling synchronization (Fig. 15.2.5). Compared to a bulky and costly lens-based system [1-3], this approach is more promising for compact and affordable systems. Fixed-pattern noise of the imager is measured and used to correct variations among pixels. The 4×4 array increases the imaging speed by 4 to 8 times, due to fewer mechanical scan steps. Following several years of anticipation, this work at last demonstrates a fully functional CMOS imager operating near or in the sub-millimeter-wave frequency range. An image obtained using the 860GHz detector with finer spatial resolution is also shown in Fig. 15.2.5.

This work suggests that Schottky diodes fabricated in CMOS without any process modifications can support THz imaging. The chip die micrographs and a performance comparison are given in Fig. 15.2.6.

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 978-1-4673-0377-4/12/$31.00

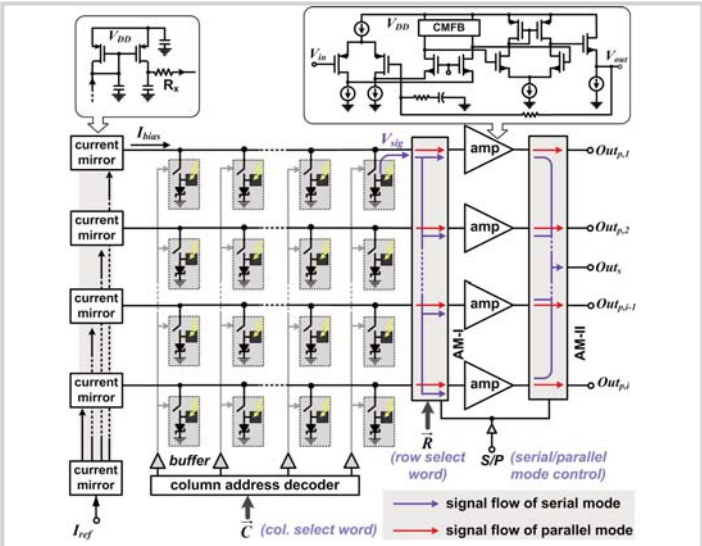


Figure 15.2.1: Proposed architecture for SBD millimeter and sub-millimeter-Wave imager in CMOS.

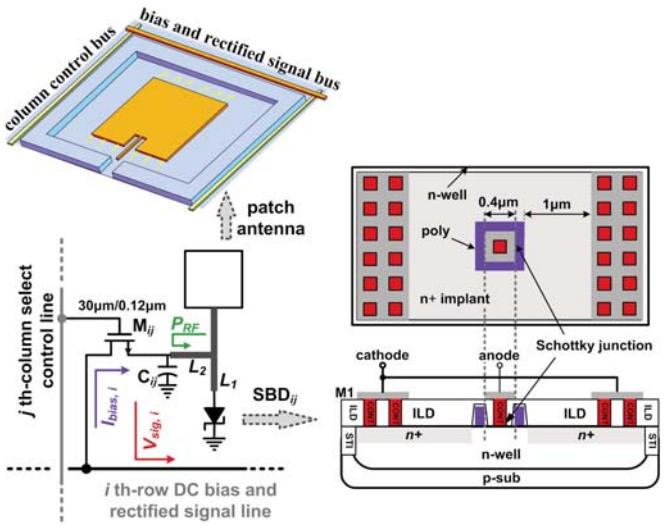
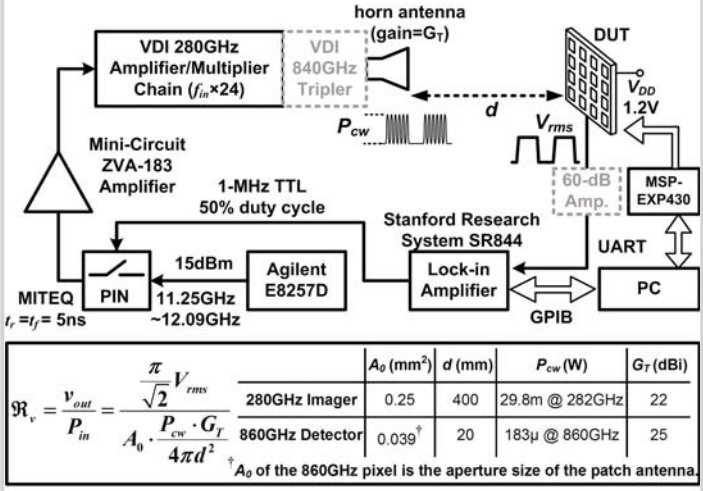


Figure 15.2.2: Schematic of a pixel, including (right) cross section and top view of the PGS SBD in CMOS, and (upper left) patch antenna.



$$\Re_v = \frac{v_{out}}{P_{in}} = \frac{\frac{\pi}{\sqrt{2}} V_{rms}}{A_0 \cdot \frac{P_{cw} \cdot G_T}{4\pi d^2}}$$

	A_0 (mm²)	d (mm)	P_{cw} (W)	G_T (dBi)
280GHz Imager	0.25	400	29.8m @ 282GHz	22
860GHz Detector	0.039†	20	183μ @ 860GHz	25

†A_0 of the 860GHz pixel is the aperture size of the patch antenna.

Figure 15.2.3: Block diagram of the responsivity measurement setup. Components in dashed lines are only for measurements of the 860GHz detector.

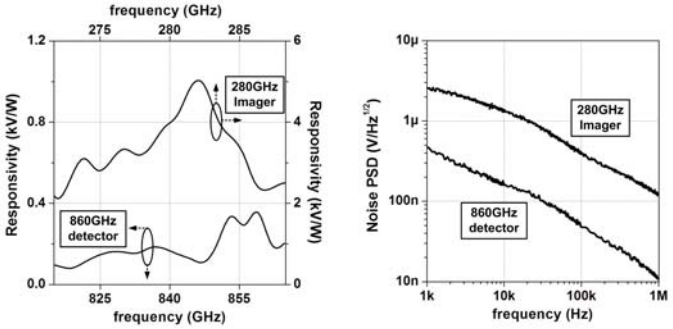


Figure 15.2.4: (Left) measured voltage responsivity and (right) output noise power-spectral density, of the 280GHz imager in serial mode and the 860GHz detector.

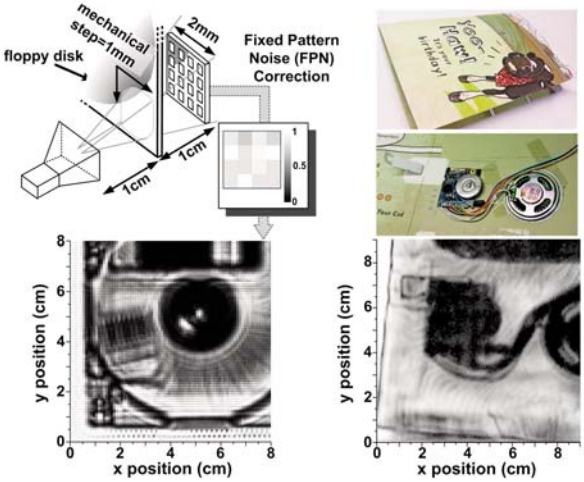
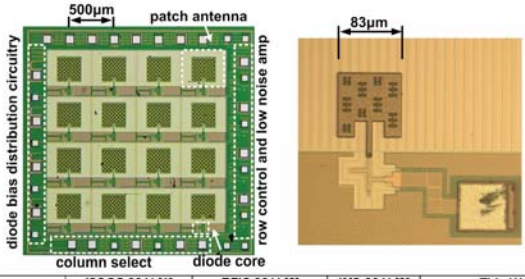


Figure 15.2.5: Lens-less THz multi-pixel imaging concept and the image of a floppy disk and a musical greeting card obtained using the 280GHz imager (left) and the 860GHz detector (right). Fixed-pattern noise of the imager is measured and used to correct variations among pixels.



	ISSCC 2011 [1]	RFIC 2011 [2]	IMS 2011 [3]	This Work	
Technology	130nm CMOS	65nm SOI CMOS	65nm CMOS	SBD in 130nm CMOS (logic)	
Array Size	3×4	15 (standalone)	15 (standalone)	4×4	single pixel
Responsivity†	2.5kV/W @ 300GHz 51V/W @ 1THz	1.1kV/W @ 650GHz 1.9kV/W @ 650GHz ††	800V/W @ 1THz	323V/W @ 283GHz	355V/W @ 860GHz
Measured NEP	Not reported	40 pW/Hz^1/2 17pW/Hz^1/2 ††	66pW/Hz^1/2	29pW/Hz^1/2	32pW/Hz^1/2
Pixel Multiplexing	Not demonstrated	No	No	Yes (dual mode)	No

†: amplifier gain is not included ††: with lens attached to the chip

Note: Listed responsivity and NEP of the detectors in [2] and [3] don't occur at the same bias point.

Figure 15.2.6: Die micrographs of the CMOS SBD 280GHz imager and 860GHz detector, and a comparison table for the state-of-the-art in CMOS THz detectors.

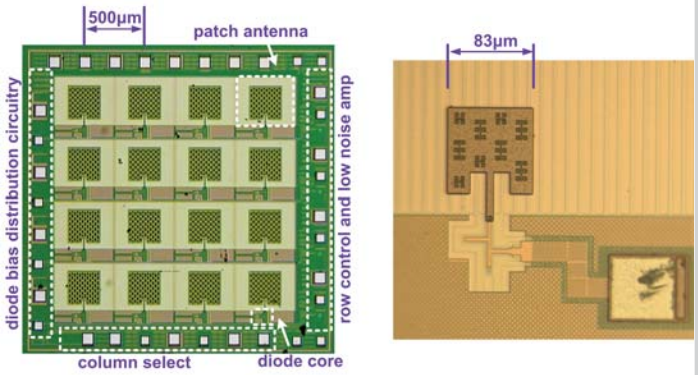


Figure 15.2.7: Die photos of the CMOS SBD 280-GHz imager and 860-GHz detector.

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