Active Terahertz Imaging Using Schottky Diodes in CMOS: Array and 860-GHz Pixel

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***Abstract*—Schottky-barrier diodes (SBD's) fabricated in CMOS without process modification are shown to be suitable for active THz imaging applications. Using a compact passive-pixel array architecture, a fully-integrated 280-GHz 4×4 imager is demonstrated. At 1-MHz input modulation frequency, the measured peak responsivity is 5.1 kV/W with $\pm 20\%$ variation among the pixels. The measured minimum NEP is 29 $\mathrm{pW/Hz^{1/2}}$. Additionally, an 860-GHz SBD detector is implemented by reducing the number of unit cells in the diode, and by exploiting the efficiency improvement of patch antenna with frequency. The measured NEP is 42 $\mathrm{pW/Hz^{1/2}}$ at 1-MHz modulation frequency. This is competitive to the best reported performance of MOSFET-based pixel measured without attaching an external silicon lens (66 $\mathrm{pW/Hz^{1/2}}$ at 1 THz and 40 $\mathrm{pW/Hz^{1/2}}$ at 650 GHz). Given that incorporating the 280-GHz detector into an array increased the NEP by $\sim 20\%$, the 860-GHz imager array should also have the similar NEP as that for an individual detector. The circuits were utilized in a setup that requires neither mirrors nor lenses to form THz images. These suggest that an affordable and portable fully-integrated CMOS THz imager is possible.**

***Index Terms*—CMOS, detector, image sensor, imaging, lens-less, NEP, on-chip patch antenna, responsivity, Schottky barrier diode, terahertz.**

I. Introduction

THE interests for utilizing silicon integrated circuits in terahertz (THz) applications are increasing [1]. Terahertz typically refers to the spectrum range between 300 GHz and 3 THz spanning the portion between the millimeter wave and infrared [2], [3]. It is also called the THz gap. Terahertz is particularly of interest in medical and security imaging applications due to its non-ionizing nature unlike that for X-rays, and smaller wavelengths that result a finer spatial resolution compared to millimeter wave imaging [2]–[4]. The rapid progress in the research of THz circuits using CMOS and other silicon technologies is starting to make it possible to integrate THz sensors and post-processing circuits in a silicon chip. This will help enable future THz imaging systems affordable and maybe even portable [5]. Due to the moderate sensitivity resulting from the lack of ability to pre-amplify the input THz signals before detection, these sensors are better suited for active imaging that requires an external THz source to illuminate objects.

The recent room-temperature active imaging research using silicon technologies builds on the THz detection with silicon MOSFET's in 2004 [6] and the demonstration of Shallow-Trench separated Schottky barrier diode (SBD) with measured cutoff frequency of 1.5 THz in foundry CMOS in 2005 [7]. The CMOS-based non-coherent detectors operating at high millimeter wave and THz frequencies are first reported using an SBD operating near 200 GHz in 2006 [8] and using a MOSFET at 650 GHz in 2008 [9], [10]. A critical figure of merit of THz imagers is Noise Equivalent Power (NEP), which is the input power level at which the signal-to-noise ratio (SNR) over 1-Hz bandwidth is unity [11]. To decrease NEP, several techniques have been proposed, but inevitably at increased cost. In [12], an NEP of 17 $\mathrm{pW/Hz^{1/2}}$ at 650 GHz was reported. This excellent NEP is achieved by attaching a high-resistivity silicon lens to a 65-nm CMOS SOI chip that enhances radiation coupling into an on-chip antenna. Without the lens, the NEP increased to 66 $\mathrm{pW/Hz^{1/2}}$ at 1.05 THz [13]. The most recent report of MOSFET imager is a fully-integrated, thousand-pixel CMOS terahertz camera chip with a measured NEP of 100 $\mathrm{pW/Hz^{1/2}}$ [14]. The imager uses a nano-scale CMOS technology (65 nm), substrate thinning, and a hyper-hemispheric silicon lens.

The first Schottky detector in CMOS for active imaging was reported in [15] and [16]. The 280-GHz detector exhibited NEP of 33-$\mathrm{pW/Hz^{1/2}}$ at 1-MHz modulation frequency. The detector utilized Poly-Gate Separated (PGS) SBD's, which have a measured cutoff frequency of ~ 2 THz and are fabricated in 130-nm CMOS without any process modifications [17]. These initial works provide a promising alternative to MOSFET detection, towards realizing a fully-integrated CMOS imager operating near 1 THz. To achieve this goal using Schottky diode detectors, it is necessary to have (i) an array architecture with low noise and a high fill factor, and (ii) a pixel operating near 1 THz with high sensitivity. This paper, which is an extended version of the work previously presented in [18], describes in greater detail the designs and prototypes from an effort to satisfy these requirements. In Section II, an imaging array architecture suitable for Schottky diode detectors is discussed and utilized to implement a 4×4 280-GHz imaging pixel array with a minimum NEP of 29 $\mathrm{pW/Hz^{1/2}}$. Unlike the arrays with in-pixel

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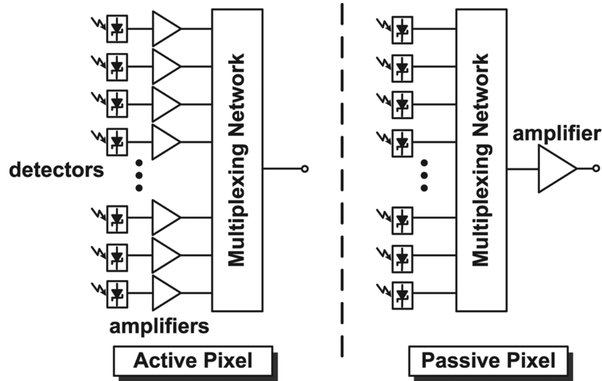


Fig. 1. Comparison between the active-pixel and passive-pixel schemes in image sensors.

amplifiers [14], [19], the proposed architecture increases noise by only 20%. Then, in Section III, an 860-GHz single-pixel prototype with an NEP of 42 $\mathrm{pW/Hz^{1/2}}$ is described. Analyses indicate that the NEP of SBD pixel can stay useful even above 1 THz. The experimental results of these two circuits are presented in Section IV. Finally, in Section V, utility of these sensors is demonstrated in a compact lens-less THz imaging setup. It is noteworthy that, similar to [15] and [16], the sensors reported in this paper are fabricated in 130-nm foundry CMOS once again without process modifications.

II. SBD Imager Architecture: 280-GHz Array

Most of previously reported THz imagers focus only on the design and characterization of a single detector. In some works ([9], [10], [12], [13], [15] and [16]), multiple pixels are implemented; however, they were not organized in an array in which each element can be separately addressed. The multiplexing function required for a fully functional imager was incorporated in [19], but not experimentally demonstrated. To date, only two fully functional THz imaging arrays ([14], [18]) are experimentally demonstrated. It is important to understand that the array architecture is highly dependent on the characteristics and DC bias of the imager transduction device. In this section, a scalable, low-noise architecture [18] specifically for imagers based on DC biased Schottky-barrier diodes in CMOS is presented.

Image sensors in general can be categorized into two types: active pixel array and passive pixel array [20]. The difference in their configurations is illustrated in Fig. 1. In CMOS visual light sensors, the in-pixel photodiodes are reversely biased, resulting in large output resistance. To avoid a large time constant due to this resistance as well as the bus capacitance, and to improve noise immunity, in-pixel buffers are typically included [20]. The situation is similar for most of MOSFET THz imagers reported to date, in which transistors, biased around subthreshold region without a DC current flow, have a large output channel resistance [10], [14], [19], thus needing in-pixel buffers. On the contrary, in SBD-based THz sensors with diodes forward biased to achieve optimum NEP, the dynamic resistance is $\sim 650\ \Omega$ [16], which is small enough to directly drive the bus. Therefore, a passive pixel scheme is adopted for our SBD imager.

In addition, the choice of passive pixel scheme is also influenced by the noise characteristics of the SBD's for two reasons. First, the initial research [16] showed that the output noise floor of the SBD pixel is dominated by flicker noise up to modulation frequency of 4 MHz. So for lower NEP, the chopping/modulation frequency of the input THz wave (thus the detector output frequency) should be close to this corner or higher. Accordingly, the amplifier following a pixel should have a sufficient bandwidth to amplify the rectified signal. Second, the absolute level of the diode noise near the flicker corner frequency is low ($< 10\ \mathrm{nV/Hz^{1/2}}$), so the input-referred noise of amplifier should be well below this to reduce its noise contribution. For an amplifier to simultaneously achieve these two requirements, significant power consumption and area are inevitable. In fact, the higher NEP of MOS detector array [14] is largely due to the noise of in-pixel amplifier. As a result, it is preferred to have passive pixels with shared amplifiers that have significantly better noise performance than that of the detector.

A block diagram of the proposed architecture prototyped in a fully-integrated 280-GHz array is shown in Fig. 2. The circuit consists of a 4×4 SBD passive-pixel array. Four pixels in each row share a single bias current circuitry located on the left. The four horizontal analog buses carry the bias current, I_{bias}, to the pixels, and transfer the rectified baseband signals, V_{sig}, to an amplifier bank on the right for signal readout. Two analog multiplexers can configure the input/output terminals of the amplifiers so as to offer two operation modes: parallel mode and serial mode. In the parallel mode, signals from four pixels within the same selected column are connected to the corresponding amplifier in each row, so that parallel amplified outputs are provided for higher throughput. In the serial mode, the two multiplexers shunt all the amplifiers together, and the input is connected to one selected row bus, so that the baseband signal from one pixel in the selected row is simultaneously amplified by all amplifiers. It will be shown later that the amplifier combining in this mode reduces the noise contribution from the amplifiers to further decrease the overall NEP. In serial mode, sixteen pixels are electronically scanned one at a time, under the control of column/row address codes. The address is assigned using the Gray code to prevent glitches during sequential scanning [21]. Next, different parts of the array are discussed.

A. Pixel Design

The schematic of each SBD pixel is shown in Fig. 3. It is based on the pixel design in [16], with modifications for multiplexing. The incident 280-GHz wave is received by an on-chip patch antenna, and is then transferred into an 8-cell Schottky diode through a short-stub GCPW transmission line matching network. The short termination of the network is provided by a metal bypass capacitor C_1 ($\sim$ 300 fF). To a rectified signal at 1 MHz, C_1 presents open. For efficient power matching and optimum NEP, the diode in an activated pixel is forward biased with 50-μA current [16]. In Fig. 3, only one horizontal bus line is needed to simultaneously multiplex the detected signal, V_{signal}, and the diode DC bias, I_{bias}. Also only one vertical line is needed to control the bus access through the MOSFET M_1. Such a compact array-interconnect scheme is another advantage of the proposed passive pixel array architecture. The *on*-resistance of M_1 (30 μm/0.12 μm) is only 15 Ω, much smaller than the 650-Ω diode dynamic resistance, to ensure a small switch

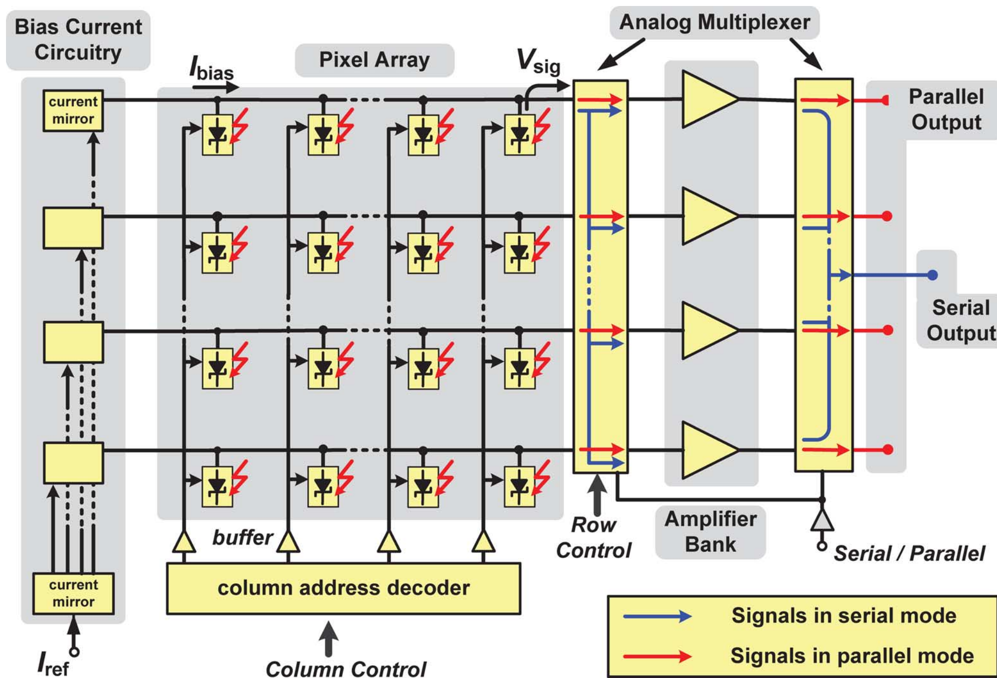


Fig. 2. The proposed SBD imaging array architecture used in the 280-GHz 4 × 4 CMOS sensor.

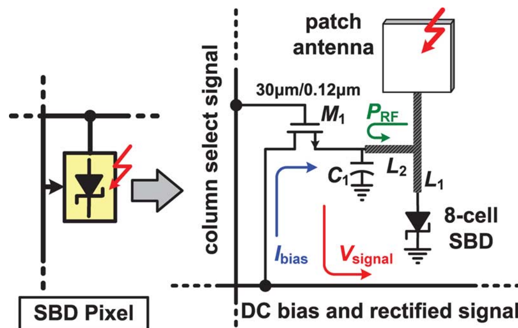


Fig. 3. The schematic of a 280-GHz passive SBD pixel inside the array shown in Fig. 2.

noise contribution. The parasitics of switch and buses are connected in parallel to the bypass capacitor C_1, which isolates the pixel core from the parasitics.

A three-dimensional structure of the diode with interconnects is shown in Fig. 4(a). The 8-cell PGS SBD is configured in a 2×4 pattern. The anodes of cells are connected to Metal 6, and then four diode-cell pairs are combined to a GCPW transmission line at Metal 8. The diode cathodes are connected to the ground plane through $n+$ diffusion regions, as well as the shunted Metal 1 and Metal 2. Fig. 4(b) shows the cross-section of one SBD unit with a Schottky junction area of $0.4 \times 0.4\ \mu\text{m}^2$. A separation of 1 μm from the grounded cathode to the central anode provides the optimum tradeoff between the metal-metal capacitance (5 fF) and the series resistance (16 Ω) for the 8-cell SBD [22]. Extracted from the measured diode I-V curve, the saturated current I_s, ideality factor n, and the knee current I_{kf} of the 8-cell SBD are 25 nA, 1.35 and 80 μA, respectively. Patch antennas are used in the pixels so that the incident radiation is shielded from the lossy Si-substrate by the ground plane (Fig. 5). The top aluminum bond-pad layer used to fabricate the patch has

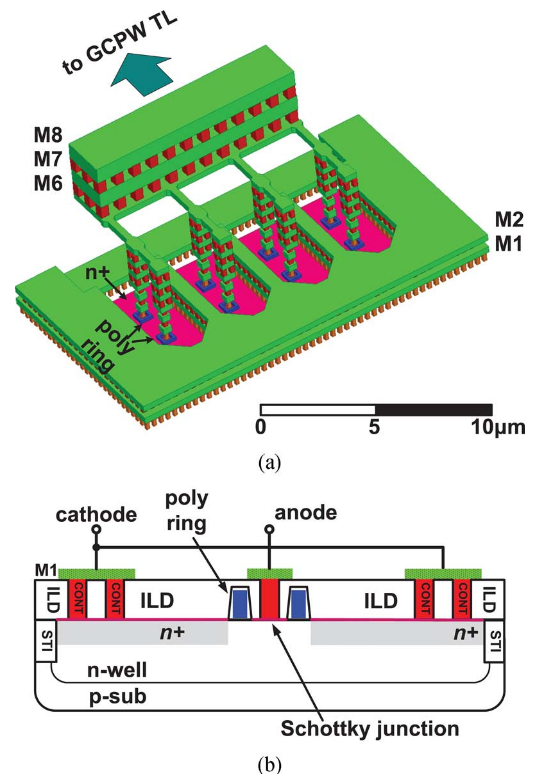


Fig. 4. (a) The 3D structure of the 8-cell SBD in the 280-GHz imager. (b) The cross-section of one SBD unit [16].

a thickness of $\sim 1.2\ \mu$m, and is 7.2-μm away from the ground plane. Between the radiator and ground plane, the metal dummy fills are blocked, and the effective relative dielectric constant of the dielectric layer in between is ~ 3.7. The HFSS-simulated [23] directivity and radiation efficiency are 6.7 dBi and 29%,

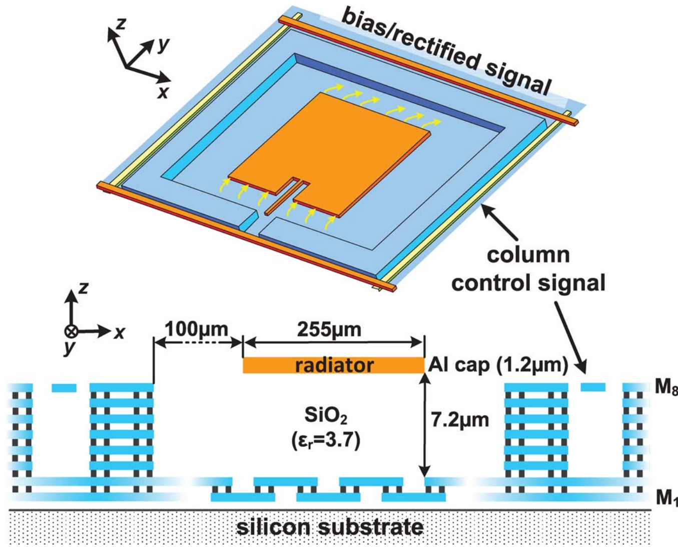


Fig. 5. Top and cross-sectional views of the on-chip patch antenna and bus lines.

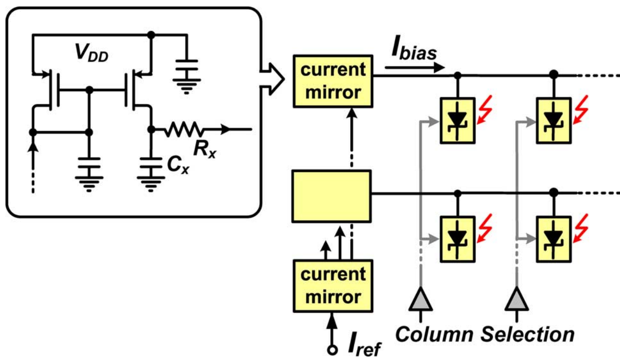


Fig. 6. Bias-current distribution network in the 280-GHz imager.

respectively. At a distance of 100 μm from the patch, stacked grounded metal walls are used to isolate patches as well as the bus interconnects.

B. Bias-Current Distribution Network

For image sensors, performance uniformity among pixels is critical to lower fixed-pattern noise (FPN). For an SBD pixel in particular, the responsivity and sensitivity are strongly dependent on the diode forward-bias current. Therefore, a *current*-mode bias distribution network is adopted. In the schematic (Fig. 6), reference current, I_{ref}, is duplicated into each row using current mirrors. In each row, a 5-kΩ polysilicon resistor, R_x, is added to decrease the loading of the bus by the bias circuitry.

C. Output Amplifier Bank

As previously mentioned, the amplifier can be configured by two analog multiplexers (Fig. 7). When in the serial mode (control pin $S/P = 0$), the bus B_1 shorts the inputs of all amplifiers together, and connects to one pixel row selected by Analog Multiplexer I. The outputs of amplifiers are shorted to serial output Out_s through Analog Multiplexer II. The total transconductance of the combined amplifiers, G_{total}, is (Fig. 8(a))

$$G_{total} = 4G_0 \tag{1}$$

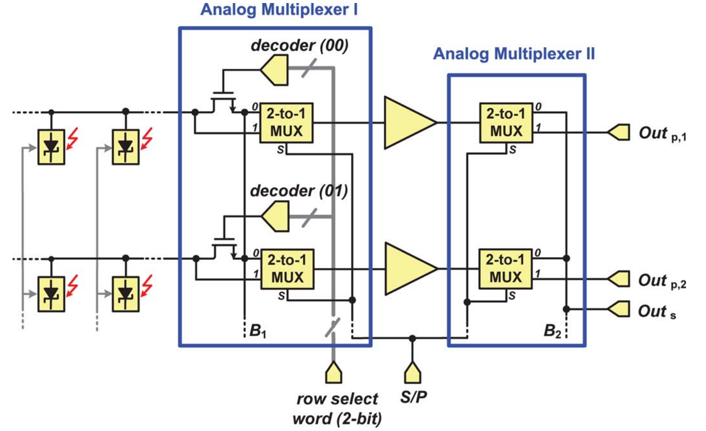


Fig. 7. Schematics of Analog Multiplexer I and Analog Multiplexer II (only two rows are shown).

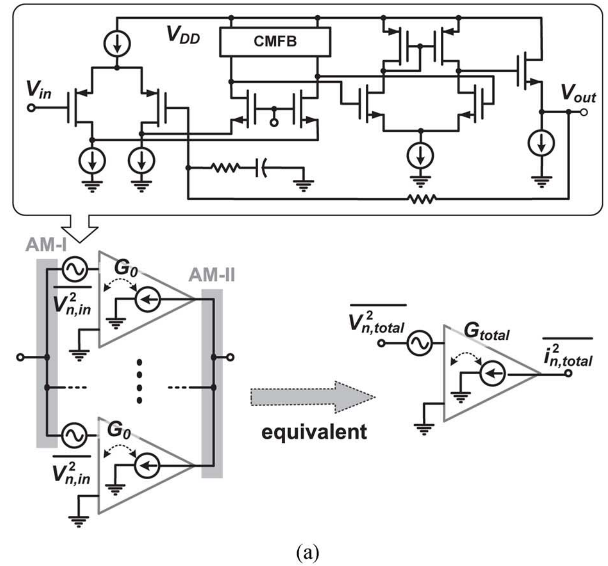


Fig. 8. (a) Schematic of the low-noise amplifier and the concept of amplifier combining. (b) Simulated pixel noise and input referred noise of the amplifier with and without the combining.

where G_0 is the transconductance of each amplifier. The total output noise current, $i_{n,total}$, is

$$i_{n,total}^2 = 4i_{n,out}^2 = 4v_{n,in}^2 G_0^2 \tag{2}$$

where $i_{n,out}$ and $v_{n,in}$ are the output noise current and input referred noise voltage of each amplifier, respectively. The contribution of the input referred current noise is negligible because the input impedance is much larger than the detector resistance. Therefore, the total equivalent input referred noise, $v_{n,total}$, is

$$v_{n,total} = \sqrt{v_{n,total}^2} = \sqrt{\frac{i_{n,total}^2}{G_{total}^2}} = \sqrt{\frac{4v_{n,in}^2 {G_0}^2}{16G_0^2}} = \frac{v_{n,in}}{2} \tag{3}$$

or 6-dB lower than the input referred noise of each amplifier. An intuitive way to understand this is that the signals are added coherently, while the noise from four uncorrelated sources are added incoherently, thus SNR increases. The schematic of the amplifier is shown in Fig. 8(a), and the design details have been presented in [16]. The simulated noise of pixel and amplifier are shown in Fig. 8(b). Due to the large-size of the PMOS input pair in each amplifier, the input referred noise is well below the diode noise. In addition, the amplifier exhibits a 3-dB bandwidth of 2 MHz. These, however, comes with the relative high DC power (1.3 mW per amplifier), which necessitates the amplifier sharing scheme as discussed before. To avoid output saturation while accommodating the large 280-GHz radiation power and small distance (Sections IV and V), the gain is set to 24 dB by on-chip resistive division feedback (Fig. 8(a)).

The SBD array architecture described above is significantly different from the ones in [14] and [19]. Besides, due to the absence of an in-pixel amplifier, for each row and column, only one metal trace is required for biasing, signal transmission and multiplexing functions. Especially at high frequencies where the size of low noise in-pixel amplifier can approach that of a pixel, the array architecture in this paper should provide a higher pixel fill factor (percentage of pixel area that is sensitive to the incident radiation [24]). A die microphotograph is shown in Fig. 9. The chip size is 2.4 $\times$ 2.4 mm^2, most of which is occupied by the on-chip patch antennas. The pixel pitch is set to about a half of the wavelength in free space ($\sim$ 500 μm) for lower Rayleigh diffraction [25]. For testing, the chip is mounted and wire bonded onto an FR-4 printed circuit board (PCB). The total DC power consumption of the imager is 6 mW.

III. SBD Detection at Terahertz: 860-GHz Low-Noise Pixel

It is desirable to increase the operation frequency of the SBD pixels to the mid-terahertz range ($\sim$ 1 THz) for several reasons. First, due to diffraction, higher-frequency operation provides better spatial resolution in an imaging system. Secondly, the areas of antenna and matching network inside each pixel are proportional to the wavelength square (λ^2), so more pixels can be integrated in a given chip area. Thirdly, the cutoff frequency (2 THz) of the PGS SBD was extrapolated from the measured data around 20 GHz [17], [22]. The terahertz detection capability of such a high cutoff-frequency device can be better verified by the measurements of THz detectors. Finally, due to the fact that many of MOSFET detectors were characterized between 650 GHz to 1 THz [9]–[14], Schottky diode detectors operating at the same frequency range will make it possible to have a cleaner performance comparison.

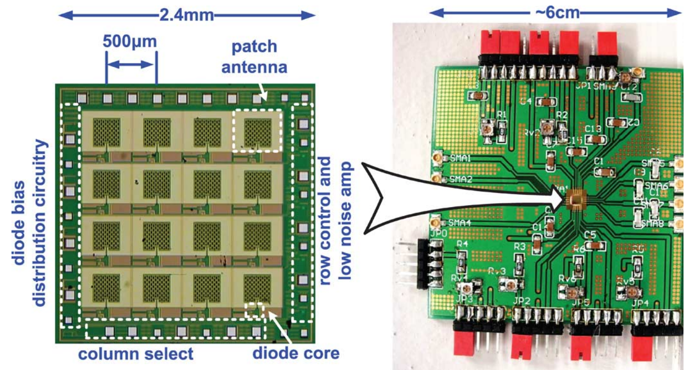


Fig. 9. Microphotograph of the 280-GHz image sensor and photograph of an imager PCB.

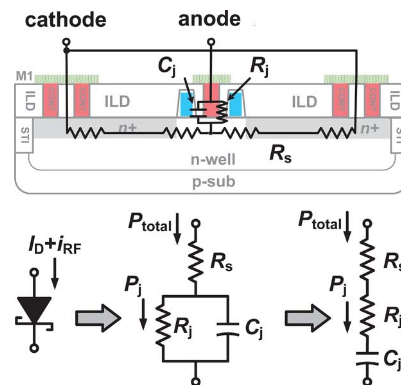


Fig. 10. Parasitics of the Poly-Gate Separated (PGS) Schottky diode.

For terahertz detection using SBD's, first it is necessary to examine the mechanisms of the high-frequency performance degradation. The parasitics of Schottky barrier diodes are illustrated in the diode cross-section in Fig. 10. The shunt capacitance, C_j, comes from the Schottky junction and the metal-to-metal capacitance. The series resistance, R_s, is due to the cathode salicided $n+$ diffusion, n-well under the polysilicon gate, and metal interconnects including contacts. Although the cutoff frequency of this device, $f_T = 1/(2\pi R_s C_j)$, is as high as 2 THz, these parasitics still degrade the detection responsivity in THz range because only a part of the total input RF power, P_{total}, is delivered to the Schottky diode core represented by the diode dynamic resistance, R_j. The RF power-transfer efficiency, η_{diode}, is [16]

$$\eta_{diode} = \frac{P_j}{P_{total}} = \frac{1}{1 + \frac{R_s}{R_j} + \frac{R_j}{R_s} \cdot \left(\frac{f_{in}}{f_T}\right)^2}. \tag{4}$$

Using (4), η_{diode} of the 8-cell diode in the 280-GHz imager in Section II as a function of input frequencies is plotted in Fig. 11 (solid line). It can be seen that the efficiency drops by 5 $\times$ from

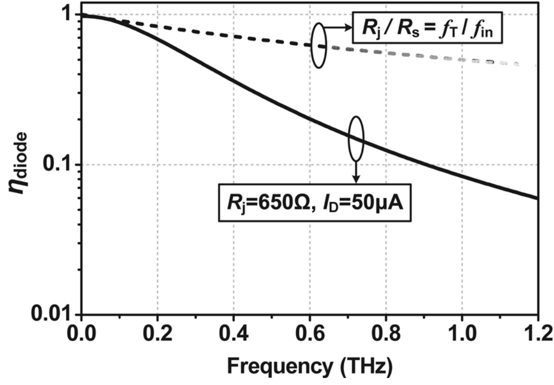


Fig. 11. Calculated RF power transfer efficiency of the 8-cell SBD as a function of input frequency.

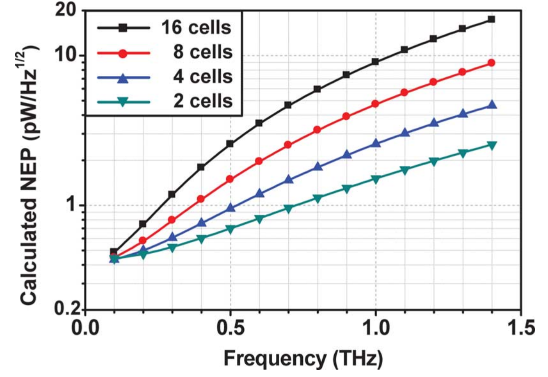


Fig. 12. Calculated NEP versus frequency for varying numbers of SBD unit cells connected in parallel. The bias current of the diodes is 50 μA.

280 GHz to 860 GHz. When R_s, f_{in} and f_T are fixed, the loss can be minimized by adjusting the diode bias current or R_j:

$$\frac{R_j}{R_s} = \frac{f_T}{f_{in}} \tag{5}$$

and the result optimum η_{diode} is also plotted (dotted line) in Fig. 11. Unfortunately, when the frequency exceeds 600 GHz, the points on the dotted line are no longer usable. This is because the bias current needed is too high and the I-V curve of Schottky diode deviates from the ideal exponential due to high-level carrier injection ($I_{kf} = 80\ \mu$A) that decreases intrinsic current responsivity [16]. Higher bias current also leads to higher $1/f$ and shot noise current. These two factors therefore degrade the NEP, which can also be expressed as the ratio between the output noise current and current responsivity. To overcome this performance degradation, the impact of diode sizing and patch antenna frequency scaling are examined next to improve the performance of SBD pixel prototype operating near 1 THz.

A. Diode Sizing

The expression for NEP when limited by shot noise at temperature T is [16]

$$NEP = \frac{4nt_w^{1/2} \cdot (k_B T)^{3/2}}{q} \cdot \frac{1 + \frac{R_s}{R_j} + \frac{R_j}{R_s}\left(\frac{f_{in}}{f_T}\right)^2}{R_j^{1/2}} \tag{6}$$

where n once again is the diode ideality factor, k_B is Boltzmann's constant, and t_w is the white noise temperature ratio (the ratio between the white noise generated from the diode and that from a resistor equal to R_j), which is $\sim n/2$ [26].

As discussed, a diode is composed of multiple unit cells connected in parallel. If m is the number of shunted diode unit cells, the NEP of an m-cell diode at input frequency f_{in} is

$$NEP = \frac{4nt_w^{1/2} \cdot (k_B T)^{3/2}}{q} \cdot \frac{1 + \frac{R_{s0}}{m \cdot R_j} + \frac{m \cdot R_j}{R_{s0}}\left(\frac{f_{in}}{f_T}\right)^2}{R_j^{1/2}} \tag{7}$$

where R_{s0} is the series resistance of each unit cell. The optimum value of m for the lowest NEP should be

$$m_{opt} = \frac{R_{s0}}{R_j} \cdot \frac{f_T}{f_{in}}. \tag{8}$$

For the values of R_{s0}, R_j, f_T and f_{in} of our interest, m_{opt} is around 1 or lower. NEP decreases with decreasing m. Using (7), NEP's of diodes with varying m are plotted versus frequency in Fig. 12. The junction resistance of the diodes R_j is 650 Ω. An equivalent ideality factor n of 1.7 is used to account for the non-negligible responsivity degradation effect due to the high-current injection at this bias point. Fig. 12 shows that NEP degrades with frequency as expected and that by choosing a smaller number of unit cells, the NEP degradation is partially compensated. For example, at 860 GHz by using a 4-cell, instead of an 8-cell SBD, the NEP degradation compared to an 8-cell SBD at 280 GHz reduces from 4.5 × to 2.5 × . If the 4-cell SBD is biased at 25 μA to keep the same current density and ideality factor, the NEP degradation is 3.1 × .

B. Antenna Efficiency

Another factor that determines the overall NEP of sensor is antenna efficiency that is inversely proportional to NEP. The 28% antenna efficiency at 280 GHz leaves a significant room for improvement. To investigate this, patch antennas for operation at varying resonant frequencies are simulated with HFSS for the CMOS process backend described in Section II (Fig. 5) and plotted in Fig. 13. The efficiency increases from 30% at 300 GHz to 73% at 850 GHz. Intuitively, this is due to an increase of the ratio between the antenna to ground gap, d, and antenna width, w, with frequency, which increases radiated power compared to the loss associated with the stored energy inside the metal cavity.

The patch antenna, being a parallel-resonance type [27], can be modeled as a shunt R-L-C circuit in Fig. 14 near the resonance frequency . The resistance is further split into one radiation resistance, R_{rad}, and three loss resistances: metal conductivity loss, $R_{loss,m}$, substrate-wave loss, $R_{loss,s}$, and dielectric loss, $R_{loss,d}$. Only the power absorbed by R_{rad} is radiated.

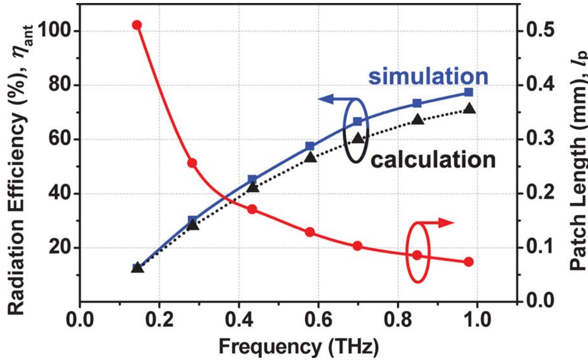


Fig. 13. HFSS-simulated radiation efficiency of patch antennas and their physical length versus operation frequency. Calculated radiation efficiencies using (9) and (13) are also included.

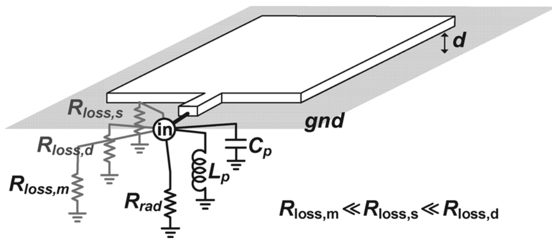


Fig. 14. Equivalent lumped circuit model of a patch antenna near the resonance frequency. The resonance frequency is set by L_p and C_p of the tank. $R_{loss,m}$, $R_{loss,d}$ and $R_{loss,s}$ represent the loss caused by the finite metal conductivity, dielectric and substrate-mode wave, respectively.

Among all loss mechanisms, the metal loss is the dominant. So the antenna efficiency, η_{ant}, can be estimated as

$$\eta_{ant} = \frac{R_{loss,m}}{R_{loss,m} + R_{rad}} = \frac{1}{1 + \frac{R_{rad}}{R_{loss,m}}}. \quad (9)$$

The antenna radiation resistance, calculated using 2-dimensional Fourier transform is [28]

$$R_{rad} = \frac{\varepsilon_{eff} Z_0^2 c_0^2}{63.6 \times (2\pi f_{in} d)^2} \quad (10)$$

where ε_{eff} is the microstrip effective dielectric constant, Z_0 is the characteristic impedance of the patch microstrip, and c_0 is the speed of light in free space.

A patch antenna is often modeled as a half-wavelength microstrip with an open termination. The finite input resonance resistance due to conduction loss of a such transmission line, $R_{loss,m}$ in (9) is [29]

$$R_{loss,m} = \frac{2Z_0^2}{R_m l_P} \quad (11)$$

where R_m is the microstrip series resistance per unit length, and l_P is the patch length (about half wavelength). Combining (9)–(11), the ratio of radiation resistance and metal loss resistance as a function of frequency is

$$\frac{R_{rad}}{R_{loss,m}} = \frac{\varepsilon_{eff} c_0^2 R_m l_P}{127 \times (2\pi f_{in} d)^2}. \quad (12)$$

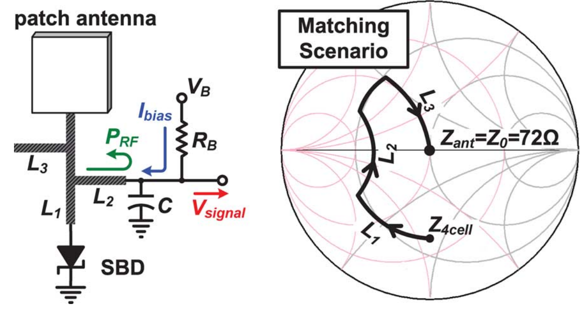


Fig. 15. Schematic of the 860-GHz SBD detector, and the matching network design in a Smith Chart. The bias resistor R_B is off-chip.

The microstrip series resistance, R_m, is inversely proportional to the conduction cross-section area, $p \cdot \delta$, where p is the perimeter of the radiator cross-section (proportional to $1/f_{in}$), and δ is the skin depth (proportional to $1/f_{in}^{0.5}$). l_P is also proportional to $1/f_{in}$. Therefore, $R_{rad}/R_{loss,m}$ in the expression of η_{ant} (9) has the following dependence on the operation frequency f_{in}:

$$\left.\frac{R_{rad}}{R_{loss,m}}\right|_{f_{in}} \propto \frac{1}{p \cdot \delta} \cdot l_P \cdot \left(\frac{1}{f_{in}}\right)^2 \propto f_{in} \cdot \sqrt{f_{in}} \cdot \frac{1}{f_{in}} \cdot \left(\frac{1}{f_{in}}\right)^2 \propto f_{in}^{-1.5}. \quad (13)$$

Based on the simulated efficiency of the 145-GHz antenna in Fig. 13, the values of $R_{rad}/R_{loss,m}$ and η_{ant} are 7.1 and 12.3% at 145 GHz. Then using (9) and (13), calculated efficiencies normalized to η_{ant} at 145 GHz are plotted in Fig. 13. They show good agreement with the HFSS simulated results.

C. 860-GHz Schottky Diode Detector Design

Due to the decreasing NEP by using a diode with fewer unit cells (Section III-A) in combination with the improved antenna efficiency at higher frequency (Section III-B), it should be possible to keep NEP of SBD detectors low up to 1 THz. To experimentally demonstrate this, a single image pixel prototype with input radiation frequency of 860 GHz is fabricated. Radiation at such frequency for testing can be obtained by cascading a frequency tripler at the output of the existing 280-GHz source. The schematic of the 860-GHz detector is shown in Fig. 15. It is similar to the topology in Fig. 3, except that an open stub L_3 is added into the matching network. Without it, the length of L_1 and L_2 will become short and too sensitive to variations. The matching network design with L_3 in a Smith Chart is also illustrated in Fig. 15. The diode has a reduced number of 4 unit cells to partially compensate the NEP degradation without taking too much risk regarding the scalability of diode model constructed from the measurement of a 16-unit diode test structure.

At terahertz, the effect of the parasitic inductance of the diode interconnects is unclear, and is unfortunately, not measurable. Using HFSS [23], the simulated inductance of the simplified interconnect structure of the 4-cell diode (Fig. 16) is 1.8 pH, which changes the reactance of the forward-biased diode from $-74j\ \Omega$ to $-64j\ \Omega$. The radiation directivity of an integrated 860-GHz patch antenna in E-plane is simulated and shown in Fig. 17. The

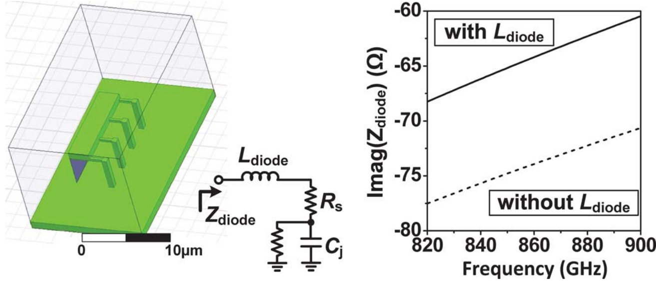


Fig. 16. Simplified structure for the full-wave EM simulation of the 4-cell diode interconnect series inductance, L_{diode}, and the simulated diode impedance with and without L_{diode}.

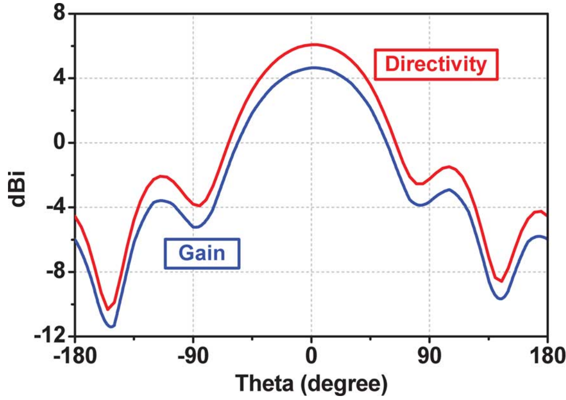


Fig. 17. HFSS-simulated radiation pattern (E-plane) of the 860-GHz on-chip patch antenna.

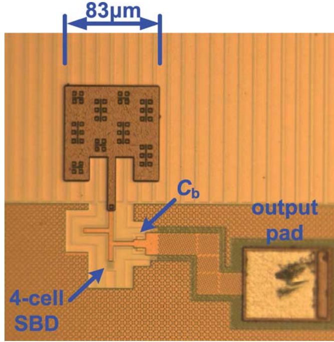


Fig. 18. Microphotograph of the 860-GHz SBD image pixel.

peak directivity is 6.7 dBi and the efficiency (including the feed line) is 71%. The patch length is only 83 μm. This design is also fabricated in the same 130-nm digital CMOS process, and its die photo is shown in Fig. 18.

IV. Measurement Results

The test setup for the measurement of imager responsivity is shown in Fig. 19. For the 280-GHz imager, the signal is radiated from a VDI 280-GHz amplifier/multiplier chain (AMC) using a horn antenna. The radiated power is calibrated using an Erickson calorimeter (Fig. 20). To mitigate the impact of flicker noise in the imager, the signal is chopped at 1 MHz with a 50% duty cycle. The chip on a PCB is aligned to the horn antenna at a large distance of 400 mm to reduce the standing wave effect [15]. A lock-in amplifier is used to generate the modulation signal, and to simultaneously measure the detected signal from the imager. The array multiplexing function is used to characterize a pixel at a time.

Based on the Friis Transmission Equation [30], the voltage responsivity of imager is [16]

$$\Re_v = \frac{v_{out}}{P_{in}} = \frac{\frac{\pi}{\sqrt{2}} V_{rms}}{A_R \cdot \frac{P_{cw} \cdot G_T}{4\pi r^2}} \tag{14}$$

where V_{rms} is the 1-MHz imager output measured by the lock-in amplifier, P_{cw} is the continuous-wave radiation power, G_T is the conical horn antenna gain (22 dBi) and r is the distance between source and imager. In (14), A_R is the pixel antenna aperture size, which is calculated from the simulated antenna directivity. In the case of this multi-pixel imager, apertures of nearby pixels overlap; so A_R is the physical size of each pixel (0.25 mm^2) [10]. Using (14), the responsivity of all pixels is extracted from measurements. The highest responsivity along with the simulation is plotted in Fig. 20. The measured peak of 5.1 kV/W occurs at 282 GHz. The distribution of the responsivity is shown in Fig. 21. The responsivity variation is less than $\pm 20\%$. After de-embedding the on-chip amplifier gain of 24 dB, the peak responsivity of the stand-alone pixel is 336 V/W.

The output noise of a 280-GHz imager is amplified by an external low-noise amplifier EG&G Model 5184, and is then analyzed with an Agilent 89410A signal analyzer (Fig. 22(a)). The $-10\ \mathrm{dB/dec}$ slope indicates that the output noise is dominated by flicker noise. At 1-MHz modulation frequency, the output noise level is 150 $\mathrm{nV/Hz}^{1/2}$. So the minimum NEP of the imager is

$$NEP_{280\ \mathrm{GHz}\ Imager} = \frac{\sqrt{\bar{v_n^2}}}{\Re_v} = \frac{150\ \frac{\mathrm{nV}}{\mathrm{Hz}^{1/2}}}{5.1\ \frac{\mathrm{kV}}{\mathrm{W}}}$$
$$= 29\ \frac{\mathrm{pW}}{\mathrm{Hz}^{1/2}}. \tag{15}$$

The simulated and measured NEP of the 280-GHz imager at varying input frequencies are plotted in Fig. 22(b). Given that the diode noise is 8.2 $\mathrm{nV/Hz}^{1/2}$ at bias current of 50 μA [16], if the rest of the imager array structure is noiseless, the total NEP (transducer device limitation) is $(8.2\ \mathrm{nV/Hz}^{1/2})/(336\ \mathrm{V/W}) = 24\ \mathrm{pW/Hz}^{1/2}$. Comparing this to that in (15), the extra elements for implementing the array including biasing, multiplexing, and amplifying circuitries, increase the NEP by only 20%.

To characterize the 860-GHz sensor pixel, a VDI WR-1.2 frequency tripler is cascaded at the output of the 280-GHz set up (Fig. 19). Signals at 815 to 865 GHz are radiated through a 25-dBi diagonal horn antenna. The radiation power is below 1 mW, so the distance between the source and chip is decreased to 20 mm to increase the output level while keeping the standing wave effect small. The measured source power and responsivity are plotted in Fig. 23. The responsivity peak of 273 V/W occurs at 860 GHz. Compared to the results reported in [18], the measured source power is 30% higher due to more accurate de-embedding of the system loss. This decreased responsivity at 860 GHz by 30%, which in turn increased NEP by 30%. The simulation in Fig. 23 shows that the center frequency of the pixel

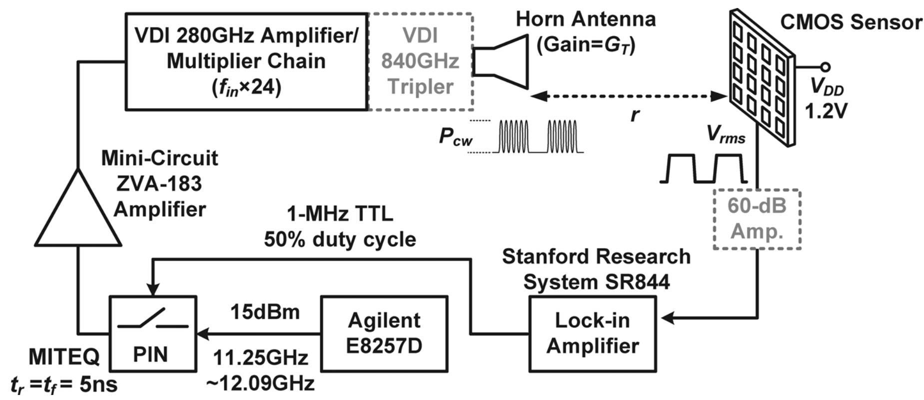


Fig. 19. Setup for responsivity measurement. Components in dashed lines are only for measurements of the 860-GHz detector.

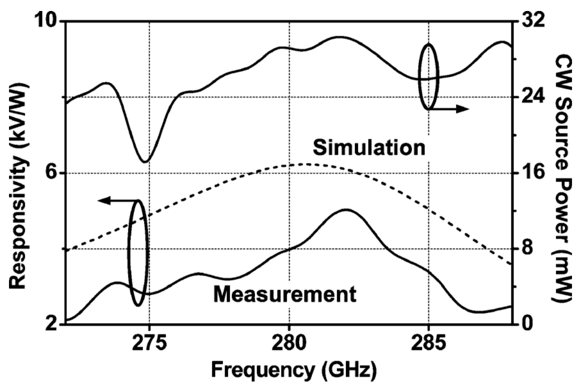


Fig. 20. Measured and simulated responsivity of the 280-GHz image sensor, as well as the measured continuous-wave radiation power of the signal source.

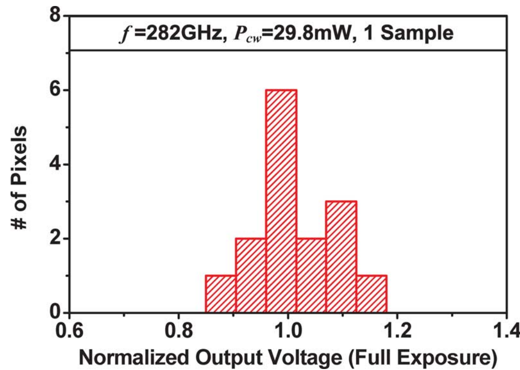
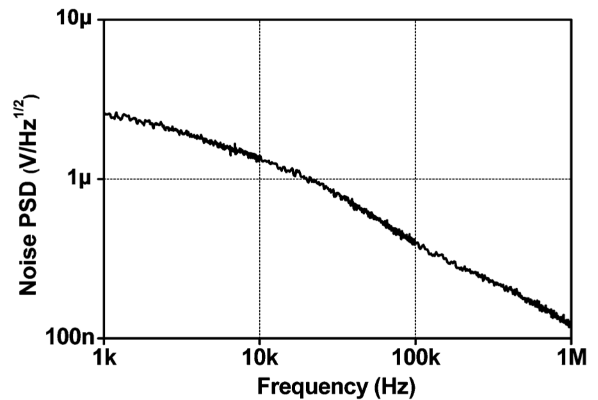
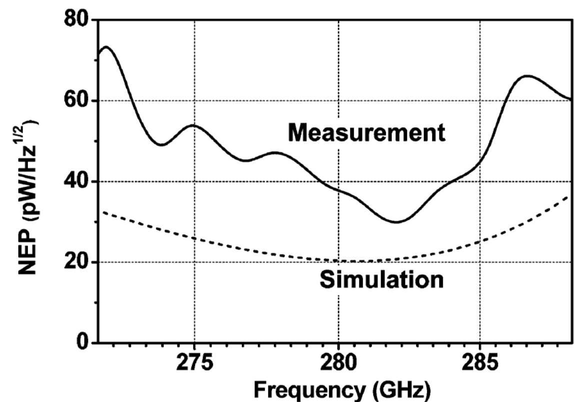


Fig. 21. Measured responsivity variation among 16 pixels of a 280-GHz image sensor.



(a)



(b)

Fig. 22. (a) The measured output noise floor of the entire 280-GHz image sensor in serial mode. (b) The simulated and measured total NEP of the 280-GHz sensor at varying input frequencies. Due to the lack of the diode noise model, the simulated NEP is based on the simulated responsivity and the measured diode noise. The diode bias current is 50 μA.

is off by 20 GHz from the design. Fig. 24 shows the measured and simulated responsivity at different diode bias currents. For bias current below 10 μA, the large diode junction resistance R_j (> 4 kΩ) increases the impedance mismatch between the antenna and the diode for input signal. Meanwhile, the larger R_j does not significantly increase the rectified signal voltage, because the detector bias resistor (~ 5 kΩ) in shunt (Fig. 15) is comparable or smaller than R_j. These factors cause the drop of the voltage responsivity in the low bias current region in Fig. 24. In the high bias current region, the voltage responsivity falls due to a decrease of R_j and high-current injection effect. The significant deviation between simulation and measurement in this high-bias region is because that the diode model used in the design cannot use a single knee current (I_{kf}) parameter to fully capture the high-current injection behavior.

Lastly, the measured noise of 860-GHz detector with 20-μA bias current is shown in Fig. 25(a). At 1 MHz, the noise is 11.1 $\mathrm{nV/Hz^{1/2}}$, so that the NEP of this detector is 42 $\mathrm{pW/Hz^{1/2}}$. Fig. 25(b) shows the simulated and measured NEP of the 860-GHz detector versus input frequency. Compared to the 280-GHz detector with an 8-cell diode, the higher $1/f$ noise

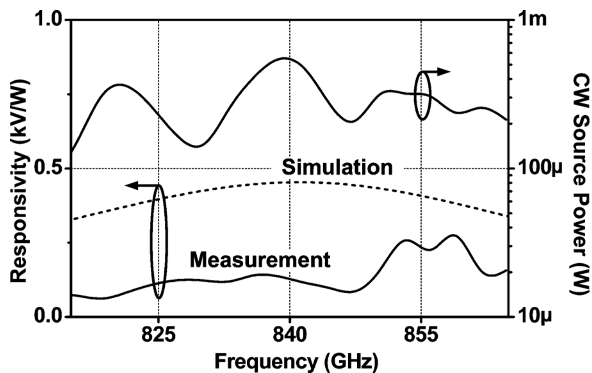


Fig. 23. Measured and simulated responsivity of the 860-GHz image pixel, as well as the continuous-wave radiation power of the signal source.

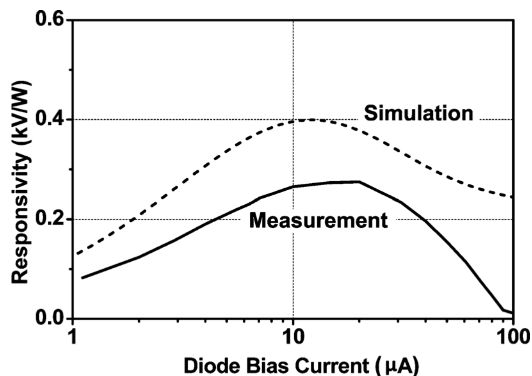
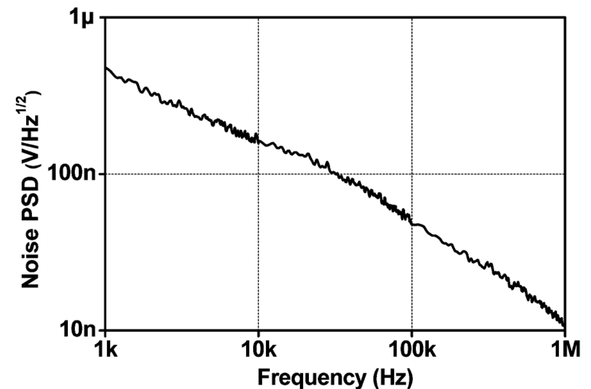
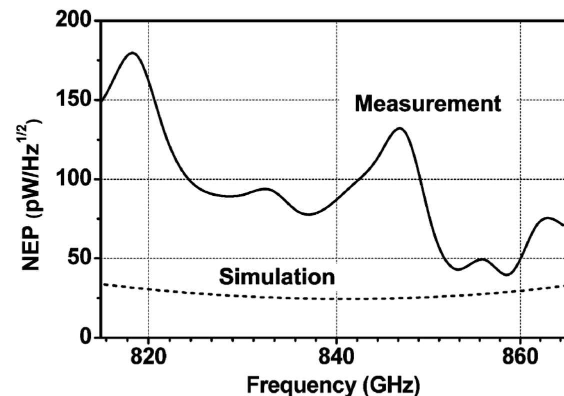


Fig. 24. Measured and simulated responsivity of the 860-GHz imager versus pixel diode bias current.



(a)



(b)

Fig. 25. (a) The measured output noise floor of the 860-GHz image pixel. (b) The simulated and measured NEP of the 860-GHz pixel at different input frequencies. Due to the lack of the diode noise model, the simulated NEP is based on the simulated responsivity and the measured diode noise. The diode bias current is 20 μA.

voltage of the 4-cell diode in the 860-GHz pixel is higher due to the smaller diode area [31]. The measured NEP of the 860-GHz detector is only $\sim 1.7\times$ higher than 24 $\mathrm{pW/Hz^{1/2}}$ of the 280-GHz detector (without an on-chip baseband amplifier). The predicted intrinsic NEP of the diode for the 860-GHz detector is $3.1\times$ higher than that of the 280-GHz detector according to the analyses in Section III-A, which include the reduction of diode area and current. Then with the $2.5\times$ improvement of antenna efficiency simulated in Section III-B, the predicted total NEP degradation is $1.2\times$. Finally, the NEP calculation in Section III-A assumes the output noise is limited by shot noise. If we replace the noise part in (7) with the measured flicker noise (Figs. 22(a) and 25(a)), the predicted total NEP degradation for the 860-GHz detector should be $1.1\times$, which is lower than the measured degradation factor of $\sim 1.7\times$.

V. Imaging in a Lens-Less Setup

In the previously reported CMOS THz imager works, including our previous SBD detectors [9]–[16], multiple lenses or mirrors are used. These bulky components, however, increase the cost, system complexity and size. In addition, focal-plane multi-pixel imaging requires precise alignment and focus which is more difficult compared to its counterpart using visible light [32]. For these reasons, it is preferable to find an alternative that can provide a path toward affordable and portable THz scanners.

In multiple THz imaging applications, objects to be imaged are thin (~ 1 to 3 cm), and can be placed in a way that simplifies the imaging process and hardware. Security check of postal envelopes, analysis of contents in an enclosure, and identification of anti-counterfeit labels are examples of such applications. For these, a proximity imaging technique is proposed in this paper and is illustrated in Fig. 26. A system is composed of a THz solid-state radiation source array, and an array of the THz imaging pixels discussed earlier. They are located in a close proximity on both sides of an object to be scanned such that the THz beam is not significantly diverged and an image can be formed without using lenses or mirrors. A diverging THz beam from each source projects the spatial information of the illuminated object region directly onto a corresponding detector pixel, so that in each scan step, the image for a strip A_i of object is constructed. By repeated stepping and scanning, a complete image of object is constructed. Since electronic scanning is faster than mechanical scanning, a larger sensor unit with more pixels on a larger die will reduce the number of mechanical steps and scan time. However, without lenses or mirrors, the image quality of lens-less approach is expected to be inferior.

In our setup in Fig. 27(a), the source-to-imager distance is 20 mm. The object is placed at the mid-point between the source and imager, and the corresponding mechanical scan step is 1 mm. An MSP-430 board [33] is used to control the multiplexing of the 280-GHz imager, which generates a 16-pixel sub-image

TABLE I
PERFORMANCE COMPARISON OF ACTIVE THz IMAGERS IN CMOS

References	Technology	Array Size	Responsivity†	Measured NEP	Chopping Frequency	Pixel Multiplexing
[12]	65-nm SOI	15 (standalone)	1.1 kV/W@0.65 THz 1.9 kV/W@0.65 THz††	40 pW/Hz$^{1/2}$ 17 pW/Hz$^{1/2}$††	1 kHz	No
[13]	65-nm bulk	15 (standalone)	800 V/W@1 THz	66 pW/Hz$^{1/2}$	1 kHz	No
[19]	130-nm Bulk	3×4	2.5 kV/W@0.3 THz 51 kV/W@1 THz	Not reported	30 kHz	Not demonstrated
[14]	65-nm bulk	32×32	140 kV/W@0.86THz†,††	100 pW/Hz$^{1/2}$††	5 kHz	Yes
[16]	Schottky diode in 130-nm bulk (logic)	2×2 (standalone)	250 V/W@0.28 THz	33 pW/Hz$^{1/2}$	1 MHz	No
This work		4×4	336 V/W@0.28 THz	29 pW/Hz$^{1/2}$		Yes (dual mode)
		single pixel	273 V/W@0.86 THz	42 pW/Hz$^{1/2}$		No

†The responsivity refers to that of the device only (with the on-chip amplifier gain de-embedded), except that in [14], which includes the gain of both the on-chip readout circuitry and a 5-dB off-chip VGA.

††The data are measured with wafer thinning and a silicon lens attached to the chip.

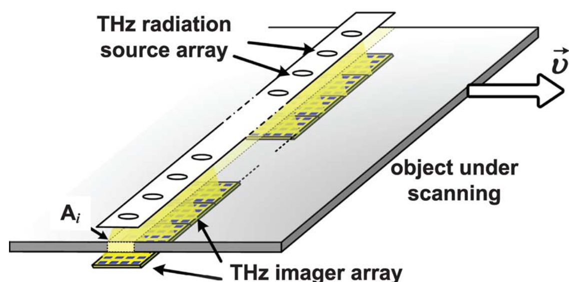


Fig. 26. Illustration of a lens-less portable THz scanner using CMOS imager integrated circuits.

for each mechanical scan step. The full-exposure (no object inserted) variation of sub-image is pre-sampled for correction of FPN. The FPN discussed here also includes the effects of non-uniformity of incident power to the detector caused by source antenna non-ideality as well as structures adjacent to the imager chip on the PCB. Once again, the source is chopped at 1 MHz. Fig. 27(b) shows the clocking sequences for the multiplexed-pixel imaging. The sampling and integration in the lock-in amplifier start after the selection of a pixel. An integration time t_2 of $\sim$ 10 mS corresponds to $\sim$ 10,000 modulation signal periods, which is long enough to average out the pixel-switching noise.

Since each 16-pixel sub-image is electronically scanned, for the same number of pixels for a given image, use of the 280-GHz array reduces imaging time from 1.5 hours down to 25 minutes. Currently, the scanning time is limited by the mechanical stepping time and delays associated with communication from and to LabVIEW software [34] that controls the setup and data collections. As Fig. 27(b) shows, the decrease approaches 16 $\times$ if the electronic sampling time t_2 is reduced (hence lower SNR). A 280-GHz image of a floppy disk formed with 80 $\times$ 80 sub-images (320 $\times$ 320 pixels) is shown in Fig. 28. The SNR of the image, which is the ratio between the data of the brightest and darkest regions, is 55 dB (with 10-mS sampling time). The internal magnetic disk and features of plastic housing are clearly

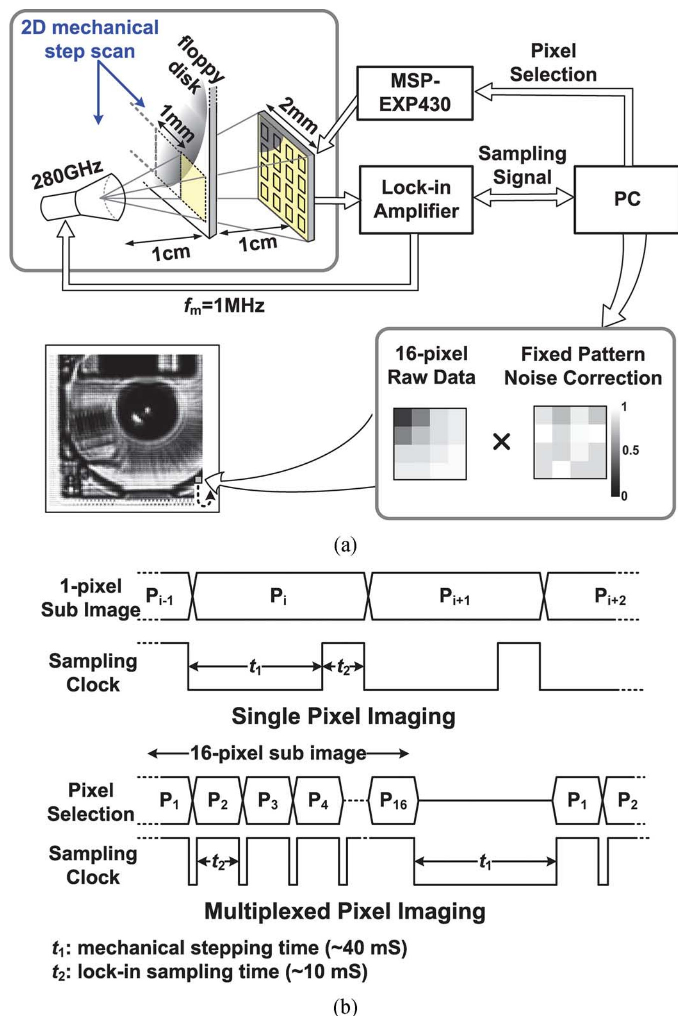


Fig. 27. (a) Lens-less THz imaging system, and 280-GHz image of a floppy disk after the fixed pattern noise correction. (b) The signal time sequences of single-pixel imaging and multiplexed-pixel imaging.

revealed. Finally, the 860-GHz detector is also utilized in the same setup. With the same 10-mS sampling time, the 860-GHz

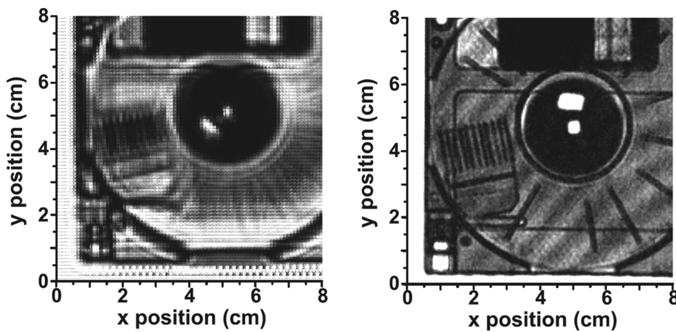


Fig. 28. Images of a floppy disk obtained using the 16-pixel 280-GHz image sensor (Left) and single 860-GHz image pixel (Right).

image has an SNR of 43 dB, and is compared in Fig. 28 to that from the scan using the 280-GHz array. It can be clearly seen that due to a smaller wavelength, the 860-GHz scan provides a better spatial resolution.

VI. CONCLUSIONS

A fully-integrated 280-GHz 4×4 imager with a measured NEP of 29 $\mathrm{pW/Hz^{1/2}}$ and a responsivity of 5.1 kV/W is demonstrated. This imager utilizes passive pixels and low noise amplifiers placed outside the pixels. Incorporation of the pixels into this highly scalable array increases NEP by only 20%. This is the first demonstration of electronic-scanning multi-pixel THz imaging using CMOS. By reducing the number of unit cells in the diode and exploiting the efficiency improvement of patch antenna with frequency for a given backend process, an 860-GHz SBD detector with a measured NEP of 42 $\mathrm{pW/Hz^{1/2}}$ is demonstrated. The circuits are fabricated using a foundry 130-nm digital CMOS process. Given that incorporating the 280-GHz detector into an array increases NEP by only 20%, the 860-GHz imager array should also have the similar NEP as that for an individual detector. The performance of imagers fabricated in CMOS is compared in Table I. The 42-$\mathrm{pW/Hz^{1/2}}$ NEP is competitive to the best reported performance of MOSFET-based pixel (66 pW/Hz at 1 THz [13] and 40 $\mathrm{pW/Hz^{1/2}}$ at 650 GHz [12]) that has been implemented using a 65-nm CMOS process and measured without using an external silicon lens. These indicate that SBD's fabricated in CMOS without process modification are competitive (if not superior) for THz imaging applications. The imaging circuits were utilized in a setup that neither requires mirrors nor lenses to form images. This in combination with the measured imager performance suggests that an affordable THz imager with a form factor similar to a smart phone should be possible.

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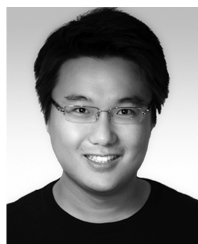

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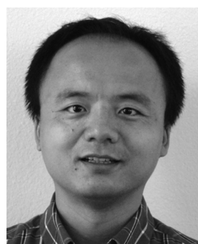

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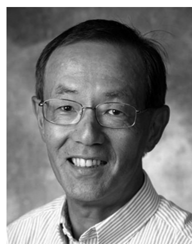

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