Design and Demonstration of 820-GHz Array Using Diode-Connected NMOS Transistors in 130-nm CMOS for Active Imaging

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***Abstract*—An 820-GHz 8 $\times$ 8 diode-connected NMOS transistor active imaging array with an on-chip pixel selection circuit was demonstrated in a 130-nm CMOS technology. The noise performance of this architecture is comparable to the state-of-the-art MOSFET and Schottky diode detector arrays. The imaging array consists of a row and column selector, an array of diode-connected NMOS transistor passive pixels, an analog multiplexer, and a low-noise amplifier bank. At 823 GHz, it achieves 2.56 kV/W of measured mean responsivity with a standard deviation of 18% and 36.2 pW/Hz$^{1/2}$ of measured mean noise equivalent power (NEP) at 1-MHz modulation frequency with a standard deviation of 67%. The mean responsivity is greater than $\sim$ 2 kV/W between 815 to 835 GHz. The minimum NEP of 12.6 pW/Hz$^{1/2}$ is the lowest for CMOS based detectors at $\sim$ 1 THz. The 8 $\times$ 8 imaging array occupies 2.0 $\times$ 1.7 mm^2 and consumes 9.6 mW of power. Reducing device sizes to support the increase of operating frequency is expected to increase the variability and mitigation approaches will be required. The measured access time for the pixel is $\sim$ 40 nS. The number of elements that can be connected in a row is determined by the modulation frequency and can be more than 1000 elements while supporting a frame rate greater than 1000 per second. Lastly, the expressions of responsivity and NEP including $1/f$ noise that can be used for the detector optimization are derived and presented.**

***Index Terms*—CMOS, diode-connected transistor detector, imaging, lens-less, NEP, on-chip antenna, responsivity, submillimeter-wave detector, terahertz.**

I. Introduction

SUB-MILLIMETER wave (300 GHz $\sim$ 3 THz) detection using complementary metal–oxide–semiconductor (CMOS) and SiGe BiCMOS technologies has recently gained interests for its higher resolution compared to millimeter-wave (mm-wave) imaging and the non-ionizing nature that should make its use safer compared with X-ray imaging [1], [2]. Submillimeter waves can potentially be used for imaging concealed objects, imaging through packages, authentication, material inspection, and others [3]–[6]. The progress resulting from these efforts using silicon as well as other semiconductor technologies has extended the upper frequency limit of electronics, and made portable and fully integrated submm-wave systems no longer an impossibility. As a matter of fact, a fully integrated 280-GHz 4 $\times$ 4 Schottky barrier diode imaging array with noise equivalent power (NEP) of 29 pW/Hz$^{1/2}$ in 130-nm CMOS [7], [8] and a 1-k pixel MOS transistor based imaging array with NEP of 100 pW/Hz$^{1/2}$ in 65-nm CMOS [9] have been demonstrated. NEP, a critical figure of merit is defined as the minimum signal power that results a unity signal-to-noise ratio (SNR) within a 1-Hz bandwidth [10]. Additionally, a 860-GHz SBD detector with NEP of 42 pW/Hz$^{1/2}$ [7], [8] has been demonstrated and noting the small difference between the NEP performance for a stand-alone detector and those in the 280-GHz array [7], an NEP of $\sim$ 50 pW/Hz$^{1/2}$ has been suggested for 860-GHz SBD imaging arrays [8].

Almost all of the previous detector research, except the four fully functional imaging arrays operating at 280 GHz[8], 700–1100 GHz [9], 200–1000 GHz [11], [12] focused on pixel characterization. Because of this, many of the presented arrays lacked the ability to address an individual pixel [14]–[18]. Most MOSFET detectors and imaging arrays reported [11], [12], [14]–[17], [19] have high impedance at the baseband frequency and have utilized an active pixel scheme, as opposed to a passive pixel scheme [7], [8],[20]. To drive a line with a large number of pixels attached, an amplifier is integrated into a pixel. Without such amplifiers, an imager is more susceptible to noise pick up, and requires a longer delay for image formation. However, if the pixel amplifier is not properly designed, then the imager NEP can be dominated by the amplifier noise[14]–[17].

The sub-millimeter wave MOSFET detectors traditionally have zero drain-to-source dc bias voltage and current which makes $1/f$ noise in the absence of RF input signal zero. In [11], [12], the source node is physically grounded. This requires AC coupling between the detector and amplifier using a capacitor with value of $\sim$ 3 pF which has an impedance of $\sim$ 50 kΩ at 1 MHz. In [15], the detector formed with a width to length ratio of 3 is biased in the deep subthreshold region with $V_{DS} = 0$ V, and the resistance is high. In [9], the total resistance of detector can be lower than 10 kΩ and it should be possible to realize an imaging array without an in-pixel amplifier, though the authors chose to include an in-pixel amplifier.

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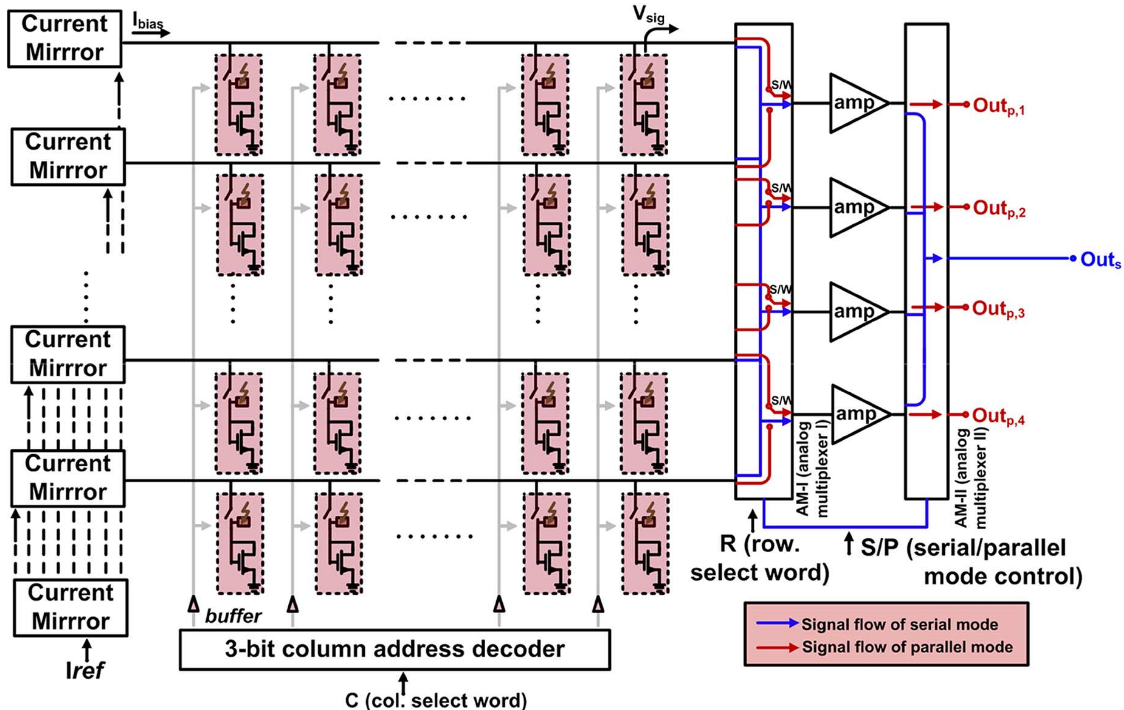


Fig. 1. Shown is the 8 × 8 array for active terahertz imaging in 130-nm CMOS technology.

A forward biased SBD detector has a relatively low dynamic resistance ($\sim$ 1.0 kΩ) and it can drive a large number of pixels without an in-pixel amplifier [7], [8]. It was shown that the output noise of SBD detectors is dominated by $1/f$ noise with a corner frequency of $\sim$ 4 MHz [18]. This issue however can be bypassed using an amplitude modulation frequency of THz signals close to or above the $1/f$ noise corner frequency and including low noise amplifiers with a sufficiently large bandwidth. As a result, a larger area and higher power consumption are necessary for the amplifiers [7], [8]. Low impedance detectors similar to SBD detectors can also be realized using diode-connected NMOS transistors. These detectors then can be arrayed like the SBD detectors using a passive pixel with highly optimized amplifiers outside a pixel. This paper reports an 8 × 8 diode-connected room-temperature NMOS transistor imaging array operating at 820 GHz [13] that achieves comparable NEP as that expected for the Schottky diode-based 840-GHz imaging arrays [8], which is more than 2 × lower than that of the best for NMOS-based imaging arrays [9]. In addition to more details of imaging array in [13], this paper presents the design considerations and additional measurement results including transient and noise characteristics. Section II describes the 8 × 8 imaging array. In Section III, detailed pixel design and responsivity and noise analyses are presented. Section IV describes the transient behavior and scalability to a larger array, while Section V presents the measurement results. A compact lensless submm-wave active imaging is demonstrated in Section VI. Finally, the paper is concluded in Section VII.

II. Imaging Array Architecture

The passive pixel array architecture used for this work is shown in Fig. 1. It is the same as that in [7], [8] except for the fact that the SBDs are replaced by diode-connected NMOS transistors. It consists of a column of current mirrors, an 8 × 8 pixel array, analog multiplexers, amplifier banks, and column/row decoders. The reference current (I_{ref}) provided from off-chip is duplicated and delivered to each of the rows (I_{bais}) via a current mirror. Each row of bus lines delivers both the bias current to pixels and the rectified signal (V_{sig}) to the amplifier bank. (The bank is the same as that for the 280-GHz SBD array [7], [8].) Two analog multiplexers (AM-I and AM-II) enable on-chip configurability for routing the detected signal(s) to the output through the amplifier(s). AM-I multiplexes the outputs of diodes to the inputs of amplifiers. AM-II can be configured so that the imaging array can be used in two operating modes: high-speed parallel mode and low-noise serial mode. In parallel mode, AM-I ties two pixel rows together such that Outp1~4 (Fig. 1) in parallel for a higher throughput. In serial mode, each of the pixels can be selected one by one. The rectified diode output signal is routed to all four amplifiers and the amplifier outputs are tied together. In serial mode, since the noise is increased by a square root of number of amplifiers while the signal is increased linearly with the number of amplifiers, the SNR at the output is increased [8].

III. Pixel Design

Fig. 2 illustrates the pixel design. Each pixel consists of an NMOS switch, a patch antenna, a diode-connected NMOS transistor, and a double stub matching network. The radiated signal is collected by an on-chip patch antenna and delivered to a diode-connected transistor via a double stub GCPW matching network. An on-chip metal capacitor C_{ij} ($\sim$ 200 fF) shorts the RF signal to ground but not the rectified signal (V_{sig}). The matching scheme is the same as that in [7], [8] and [13]. The

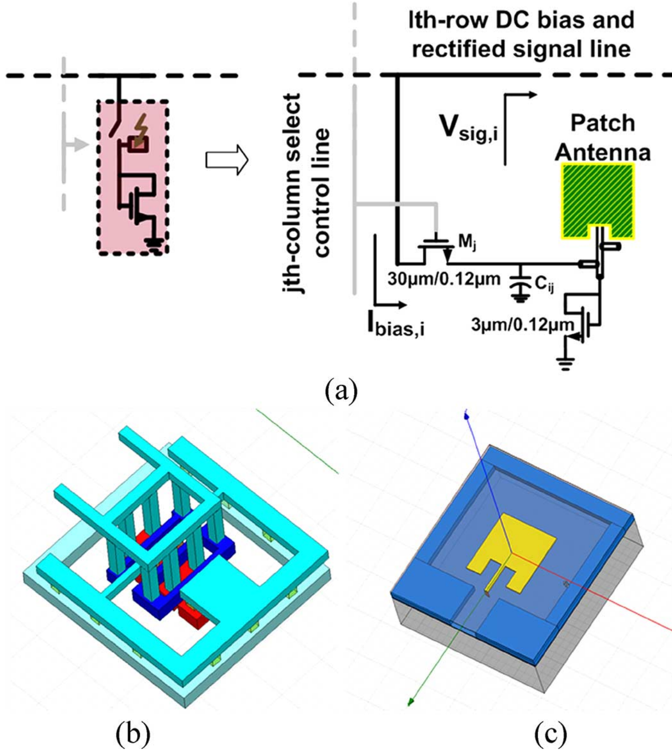


Fig. 2. Schematic of single detector pixel. Each of the pixel (a) has a column selector and (b) a diode-connected transistor and (c) an on-chip patch antenna.

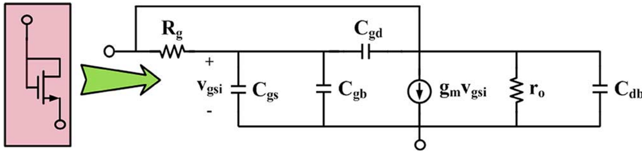


Fig. 3. Equivalent circuit model of diode-connected NMOS transistor.

NMOS column selector (M_j) controls the distribution of bias current (I_{bias}) and the rectified signal.

A. Diode-Connected MOS Transistor Design

For the simulation of this design, the digital transistor model with a gate resistor, R_g added in series is used because the transistor width required for the detector is smaller than the minimum allowed for RF transistors in the 130-nm CMOS process technology. R_g is estimated by scaling the gate resistance simulated using the RF transistor model that includes the non-quasi-static (nqs) effects. The process used for this work supports BSIM3 transistor models. An equivalent small signal model including the gate resistance is shown in Fig. 3.

The current responsivity is

$$\Re_i = \frac{\Delta i}{P_{\rm in}} = \frac{P_j}{P_{\rm total}} \cdot \frac{\Delta i}{P_j} = \eta_{\rm diode} \cdot \Re_{i0} = \eta_{\rm diode} \cdot \frac{f^{(2)}(v)}{2f^{(1)}(v)} \quad (1)$$

where $P_j/P_{\rm total}$ is the RF power-transfer efficiency or power degradation factor, $\eta_{\rm diode} f(v)$ is the I-V characteristic, and $f^2(v)$ and $f^1(v)$ are the second and first derivatives of $f(v)$ with respective to voltage [8], [10], [18]. P_j is the power delivered to the junction and $P_{\rm total}$ is the power incident to the detector. $\eta_{\rm diode}$ can be simulated using the small-signal model in Fig. 3 [21].

In the subthreshold region, drain current is exponentially dependent on gate voltage, and drain current is

$$I_{\rm DS} = \frac{W}{L} I_t \cdot \exp\left(\frac{v_{\rm GS} - V_{\rm TH}}{nV_T}\right) \cdot \left(1 - \exp\left(-\frac{v_{\rm DS}}{V_T}\right)\right) \quad (2)$$

where $I_t = q \cdot X \cdot D_n \cdot n_{po} \cdot \exp(k_2/V_T)$, $v_{\rm GS} = v_{\rm DS} = V_{\rm GS} + v_{\rm gs}$ [22]. D_n is the diffusion constant, n_{po} is the equilibrium electron concentration in the p-type body underneath the gate oxide, n is the gate coupling coefficient/ideality factor, V_T is the thermal voltage, X is the thickness of region in which the current flows, and k_2 is the ratio between the thermal voltage and gate coupling coefficient [22]. Since the dc gate to source voltage, V_{GS} is at least 3 times larger than the thermal voltage, V_T at the operating point, the second exponential term can be ignored. Therefore, from (2) the intrinsic current responsivity in the subthreshold is

$$\Re_{i0} = \frac{f^{(2)}(v)}{2f^{(1)}(v)} = \frac{1}{2nV_T}. \quad (3)$$

The voltage responsivity $\Re_v$ is defined as the ratio between the output voltage and input power

$$\begin{aligned}\Re_v &= \frac{\Delta v}{P_{\rm in}} = \frac{P_j}{P_{\rm total}} \cdot \frac{\Delta i}{P_j} \cdot R_j \\ &= \eta_{\rm diode} \cdot \Re_{v0} \\ &= \eta_{\rm diode} \cdot \frac{f^{(2)}(v)}{2\left[f^{(1)}(v)\right]^2} = \eta_{\rm diode} \cdot \frac{1}{2I_{\rm DS}}. \end{aligned} \quad (4)$$

Fig. 4(a) plots the simulated power degradation factor based on the small-signal model of diode-connected transistor in Fig. 3. The model parameters were extracted from the dc operating point simulation. The current responsivity simulated (harmonic balance) using the transistor model from the foundry is plotted in Fig. 4(b). The current responsivity computed by multiplying the simulated power degradation factor [$P_j/P_{\rm total}$, from Fig. 4(a)] multiplied and calculated $\Delta i/P_j = 1/(2nV_T)$ is also plotted in Fig. 4(b). The two plots are within 20%, suggesting that the simple expression for $\Delta i/P_j$, neglecting the nonlinear effects of capacitances is useful up to 1 THz. This is due to the fact that dc current cannot flow through capacitors and means that, if the power degradation factor can be computed, than an expression for the current responsivity with a similar accuracy as the simulation should be possible.

Unfortunately, the small-signal model in Fig. 3 is too complicated for hand analyses due to R_g, which is mostly due to the nonquasistatic effect. The circuit model is modified to that in Fig. 5 to make it more amenable for hand analyses. R_g is incorporated into R_i in series with C_{gs}. Fig. 6 compares the power degradation factors simulated using the two circuit models. Up to 1 THz, the differences are less than 20%, which suggests that the simplification is acceptable. For the circuit model in Fig. 5,

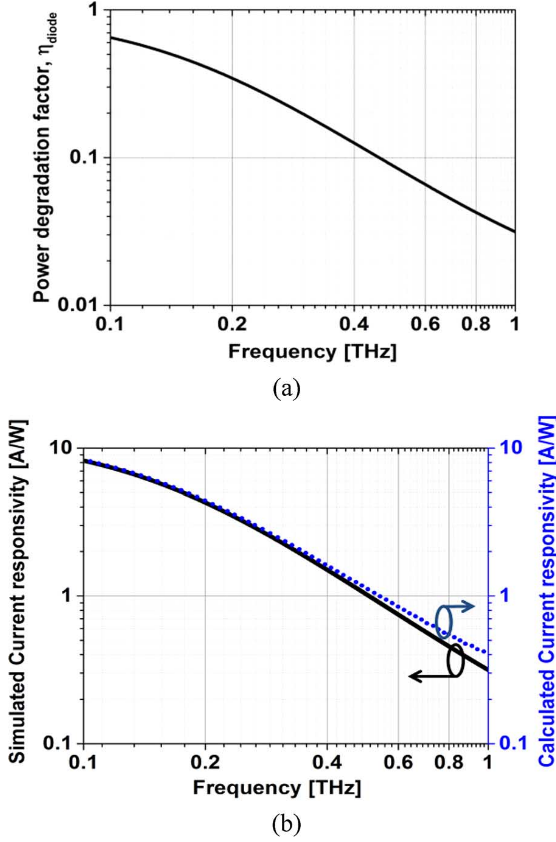


Fig. 4. (a) Simulated power degradation factor using the equivalent circuit model in Fig. 3. (b) Simulated current responsivity using an augmented transistor model from the foundry and calculated current responsivity multiplying the simulated power degradation factor in (a) with $1/(2nV_T)$.

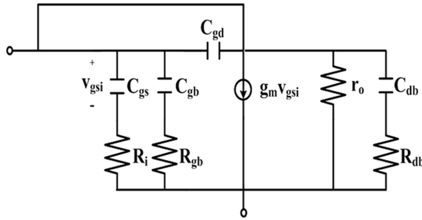


Fig. 5. Approximate small-signal model for hand analyses.

C_{gd} is shorted and v_{gsi} is computed using a simple voltage divider between the impedance of C_{gs} and R_i.

The power degradation factor η_{diode} is then

$$\begin{aligned}\eta_{\text{diode}} &= \frac{P_j}{P_{\text{total}}}\\ &= \frac{1}{\left(1+\left(\frac{f_{in}}{f_{B1}}\right)^2\right)\left[\frac{\frac{R_j}{R_i}\left(\frac{f_{in}}{f_{B1}}\right)^2}{1+\left(\frac{f_{in}}{f_{B1}}\right)^2}+\frac{\frac{R_j}{R_{db}}\left(\frac{f_{in}}{f_{B2}}\right)^2}{1+\left(\frac{f_{in}}{f_{B2}}\right)^2}+\frac{\frac{R_j}{R_{gb}}\left(\frac{f_{in}}{f_{B3}}\right)^2}{1+\left(\frac{f_{in}}{f_{B3}}\right)^2}+\frac{1}{1+\left(\frac{f_{in}}{f_{B1}}\right)^2}+\frac{R_j}{r_o}\right]}\\ &\cong \frac{1}{1+\frac{R_j}{R_i}\left(\frac{f_{in}}{f_{B1}}\right)^2}\end{aligned}$$

$$f_{B1}=\frac{1}{2\pi C_{gs}R_i},\ f_{B2}=\frac{1}{2\pi C_{db}R_{db}},\ f_{B3}=\frac{1}{2\pi C_{gb}R_{gb}}. \quad (5)$$

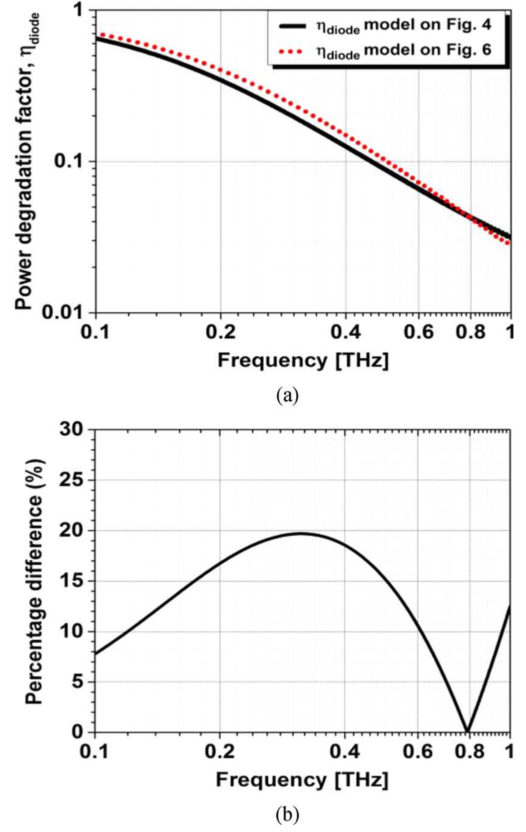


Fig. 6. (a) Comparison of power degradation factors based on the small-signal models in Figs. 3 and 5. The solid line is based on the small-signal model in Fig. 3 and the dotted line is based on the small-signal model in Fig. 5. (b) Percentage difference between the two plots in (a).

The drain–current noise power spectral density (PSD) of a transistor [10], [23] is

$$\begin{aligned}\frac{i_n^2}{\Delta f} &= \frac{2k_BT}{R_j}+\frac{K_f}{f_{\text{mod}}}\cdot\left[\frac{C_{\text{inv}}}{C_{\text{ox}}+C_d}\right]^2\cdot\frac{g_{\text{m}}^2}{W\cdot L\cdot C_{ox}^2}\\ &= \frac{2k_BT}{R_j}+\frac{C_{\text{inv}}^2}{(C_{\text{ox}}+C_d)^4}\frac{q^4}{(k_BT)^2}\cdot I_d^2\cdot\frac{N_{ot}}{W\cdot L\cdot f_{\text{mod}}}\end{aligned} \quad (6)$$

where K_f is a device specific flicker noise constant, C_{inv} is the inversion capacitance, C_{ox} is the oxide capacitance, C_d is the depletion capacitance, N_{ot} is the equivalent density of oxide traps per unit area, k_B is the Boltzmann's constant, T is temperature in °K, and f_{mod} is the amplitude modulation frequency of illuminating sub-millimeter wave signal. The inversion capacitance at subthreshold, C_{inv} is approximately equal to $Q_{\text{inv}}/(k_BT/q)$, therefore, C_{inv} is exponentially dependent on the gate to source voltage [23] and proportional to g_{m}.

NEP is the ratio between the output noise current and the current responsivity. When the shot noise is dominant, NEP is [8], [18]

$$\begin{aligned}\text{NEP} &= \frac{\sqrt{\frac{i_n^2}{\Delta f}}}{R_{i0}\cdot\eta_{\text{diode}}}=\frac{n(2k_BT)^{3/2}}{q\cdot R_j^{1/2}\cdot\eta_{\text{diode}}}\\ &\approx \frac{n(2k_BT)^{3/2}}{q\cdot R_j^{1/2}}\cdot\left(1+\frac{R_j}{R_i}\left(\frac{f_{\text{in}}}{f_{B1}}\right)^2\right).\end{aligned} \quad (7)$$

R_i is $\sim(1/5g_{\text{m}})$ [24].

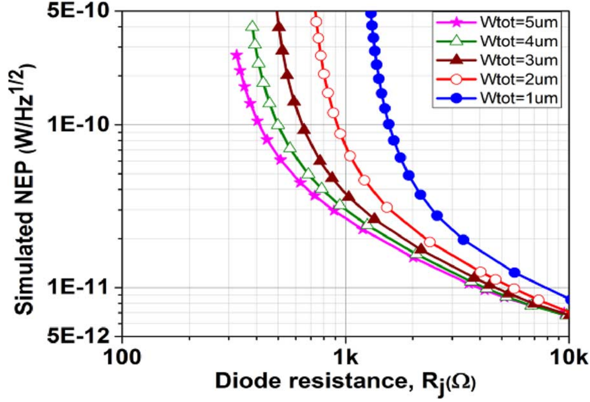


Fig. 7. Simulated NEP versus diode dynamic resistance and transistor width. The right-most plot is for the 1-μm width.

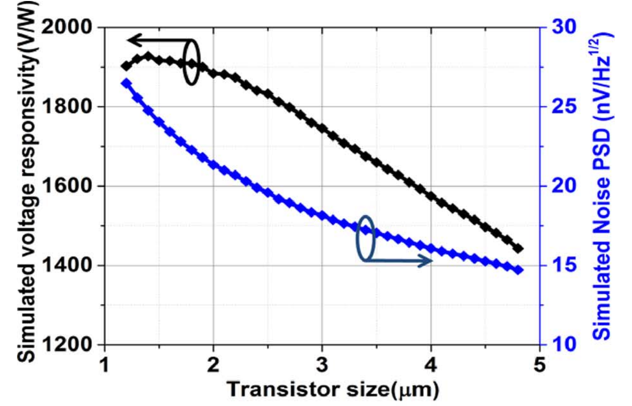
When the flicker noise is dominant, NEP is

$$\begin{aligned}\mathrm{NEP} &= \frac{\sqrt{\frac{i_n^2}{\Delta f}}}{R_{i0}\cdot\eta_{\mathrm{diode}}} = \frac{2nk_BT\cdot g_{\mathrm{m}}}{q\cdot C_{\mathrm{ox}}\cdot\eta_{\mathrm{diode}}} \\ &\quad\cdot\left[\frac{C_{\mathrm{inv}}}{C_{ox}+C_d}\right]\cdot\left(\frac{K_f}{f_{\mathrm{mod}}\cdot W\cdot L}\right)^{1/2} \\ &\approx \frac{2nk_BT\cdot g_{\mathrm{m}}}{q\cdot C_{\mathrm{ox}}}\cdot\left[\frac{C_{\mathrm{inv}}}{C_{\mathrm{ox}}+C_d}\right] \\ &\quad\cdot\left(\frac{K_f}{f_{\mathrm{mod}}\cdot W\cdot L}\right)^{1/2}\cdot\left(1+\frac{R_j}{R_i}\left(\frac{f_{\mathrm{in}}}{f_{B1}}\right)^2\right). \quad (8)\end{aligned}$$

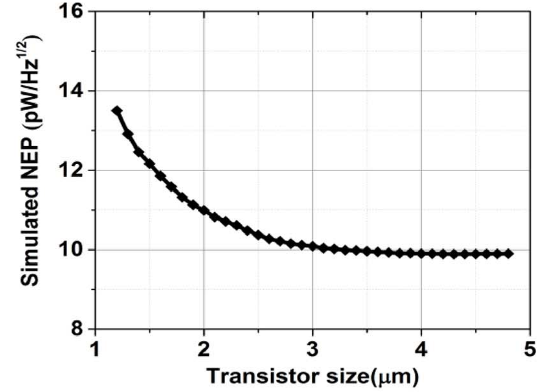
Simulated NEP using the digital transistor model from the foundry augmented to include R_g is plotted in Fig. 7. Amplitude modulation frequency is 1 MHz for an 840-GHz submm-wave signal. The finger width is chosen to be 1 μm, and the number of fingers is increased from one to five, resulting in a total transistor width range of 1 to 5 μm. It shows that a larger transistor and higher diode dynamic resistance, R_j are preferred because a smaller transistor requires larger diode voltage to lower R_j which causes deviation from the ideal exponential behavior, which reduces $\Re_{i0}$ and increases NEP. For BSIM3 models, R_i is bias independent and NEP is proportional to g_m due to the exponential dependence on V_{GS} for both C_{inv} on g_m. If R_i is proportional $1/g_m$ [24], then NEP in (8) should be proportional to g_m^2.

The diode dynamic resistance R_j forms a low-pass filter in combination with the input capacitance of on-chip amplifier and pixels connected to a row, which limits the detector bandwidth and increases the time required to form an image. For the $\sim$ 1 pF input capacitance of on-chip amplifier [8], the optimum R_j is $\sim$ 4 kΩ to keep the diode-connected transistors to operate in or close to the sub-threshold region while supporting settling time of 50 ns (3σ) corresponding to a 10-MHz bandwidth in serial mode. The on-chip amplifier with a simulated bandwidth of 10 MHz that can work with a modulation frequency up to the flicker noise corner frequency of diode connected transistor ($\sim$ 10 MHz) should be able to also support this imaging bandwidth.

Simulated voltage responsivity at 840 GHz and voltage noise PSD using the augmented foundry model are plotted versus transistor width in Fig. 8(a). The diode dynamic resistance, R_j



(a)



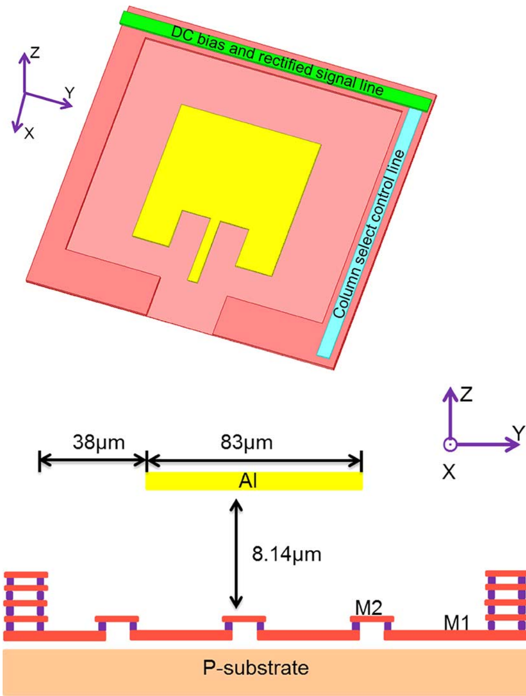
(b)

Fig. 8. (a) Simulated voltage responsivity (left axis) at 840 GHz and simulated $1/f$ noise PSD at 1 MHz (right axis) versus transistor width when R_j = 4 kΩ. (b) Simulated NEP at 840 GHz and 1-MHz modulation frequency.

is 4 kΩ. As the transistor width is increased, the voltage responsivity decreases due to a reduction of power degradation factor, η_{diode}. The factor decreases because C_{gs} increases with the width which in turn increases the $(R_j/R_i)\cdot(f_{\mathrm{in}}/f_{B1})^2$ term in the denominator of (5). On the other hand, as the transistor width is increased, because the transistor operates deeper in the subthreshold region, the g_m/I_D ratio increases and requires smaller drain current for given R_j. $1/f$ noise decreases because the gate area is increased and $C_{\mathrm{inv}}/(C_{\mathrm{ox}}+C_d)$ is decreased. The simulated drain voltage noise at 1 MHz versus transistor width when R_j is once again 4 kΩ is also shown in Fig. 8(a). Fig. 8(b) shows the corresponding simulated NEP at 840 GHz versus the transistor width. When the transistor width is $\sim$ 3 μm, the NEP is near the minimum. Additionally, the matching network required for transistors with a larger width exhibit larger loss. For these, a width of 3.0 μm is chosen for the detector design.

B. On-Chip Antenna Design

The on-chip antenna is the same as that in [7], [8]. It is formed using the top aluminum layer ($\sim$ 1 μm thick) with the ground plane formed by stagger shunting metal 1 and metal 2 layers (Fig. 9). The width and length of each patch antenna are 83 μm, and the thickness of dielectric layer between the patch antenna and ground plane is $\sim$ 8 μm. The HFSS [25] simulated peak antenna gain and directivity are 5.8 dB and 7 dBi, respectively,



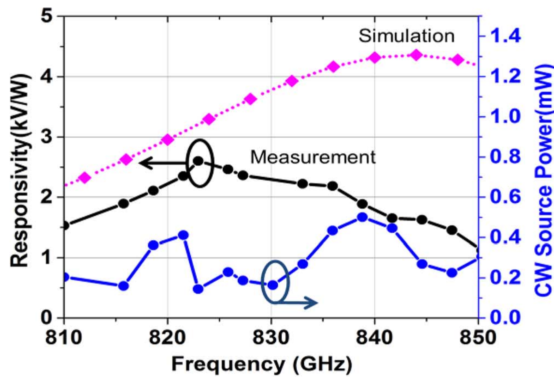
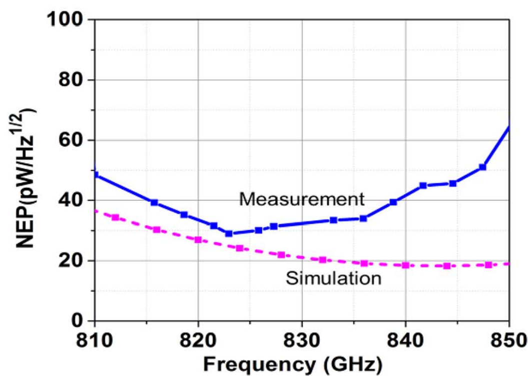


Fig. 9. Top and cross-sectional views of the on-chip patch antennas, ground planes, and signal lines.



(a)

(b)

Fig. 10. (a) Simulated and measured median responsivity of imaging array including the on-chip amplifier gain (left axis) and measured continuous wave power (right axis) of the signal source. (b) Simulated and measured median NEP at 1-MHz modulation frequency of imaging array versus input frequency.

and the radiation efficiency is 74%. The simulated −10-dB input match bandwidth is 22 GHz. A ground wall is made by stacking

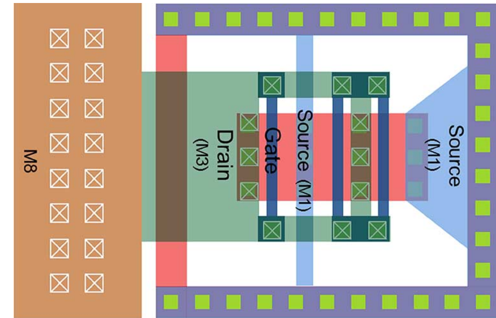


Fig. 11. Layout of a diode-connected transistor pixel. Gate and drain are tied using a Metal 3 (M3) connection and source and body are tied to ground using a Metal 1 (M1) connection. Double sided contacts for polysilicon gate reduce the gate resistance.

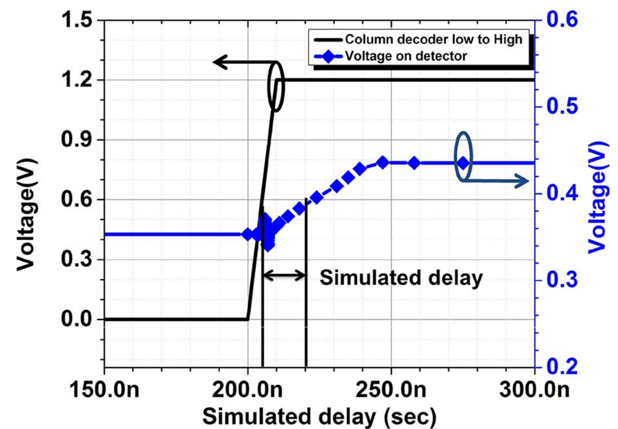


Fig. 12. System timing diagram simulated including post-layout extracted parasitics. When the least significnat bit of column decoder goes to low from high (solid line), the voltage on the data line of selected row (solid line with diamonds) increases from 0.35 V to 0.43 V. To create this output change in simulation, a pixel formed using a diode connected Slow Slow (SS) NMOS transistor is accessed following a read operation of a pixel formed using a diode connected Typical Typical (TT) NMOS transistor. The total delay for driving the data line including the on-chip amplifier input capacitance is ∼ 16 nS.

five layers (Metal 1 – Metal 5) of metal and connecting it to the ground to isolate the bias and rectified signals. The pixel pitch is designed to be a half of the wavelength in free space λ_0 ($\sim$ 170 μm) to mitigate the diffraction effects [26].

C. Pixel Design and Layout

Fig. 10(a) and (b) shows the simulated responsivity and NEP of a pixel including the on-chip amplifier gain. Responsivity is simulated by harmonic balance simulation and NEP is simulated using the noise and harmonic balance simulation in ADS. The detector is tuned at 840 GHz. The loss of antenna and matching network reduces responsivity by 45% and therefore, it increases NEP by 82%. Each pixel including its interconnect capacitance adds approximately 35 fF to the data bus line. For the array with eight imaging elements with an on-chip amplifier and bias circuitry, the capacitance associated with the array is 600 fF (8×35 fF+300 fF from bias circuitry), while the total capacitance including that for the amplifier is 1.4 pF (0.8-pF input capacitance of on-chip amplifier +600-fF pixel capacitance).

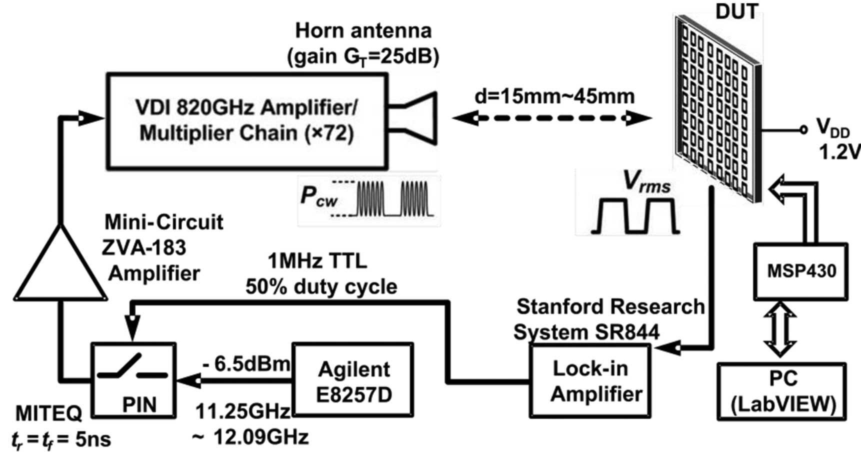


Fig. 13. Responsivity measurement setup.

A layout of diode-connected transistor is shown in Fig. 11. It consists of three fingers (1 μm each) and a p^+ guard ring. Also, to reduce the drain-to-body interconnect parasitic capacitance, the space from drain (Metal 3) to Metal 1 substrate connection is made to be greater than 1 μm. Also, the distance between n^+ diffusion and p^+ body tie is set at 0.9 μm. The gate and drain are tied using a Metal-3 line $\sim$ 5.75 μm away from the gate and then stacked up to the top metal (Metal 8). Double side polysilicon gate contacts are utilized to reduce the polysilicon gate resistance.

IV. Transient Behavior of Imaging Array

Fig. 12 shows the timing diagram for accessing an element. The delay from the column decoder to the output of the on-chip amplifier (in Fig. 1) is estimated using post-layout extraction and simulations. To create an output change in simulation, a pixel formed using a diode connected Slow Slow (SS) NMOS transistor is accessed following a read operation of a pixel formed using a diode connected Typical Typical (TT) transistor. The column decoder consists of three-input NOR gates followed by buffers (a chain of four inverters). Analog multiplexers I and II (in Fig. 1) consist of NMOS switches with an on-resistance of 15 Ω. The simulated delay associated with driving the data line and input capacitance of on-chip amplifier is $\sim$ 16 ns ($\simeq \tau$) for R_j of 4 kΩ in serial mode (in Fig. 1) with a capacitive load of $\sim$ 4.0 pF (4×0.8-pF input capacitance of on-chip amplifier $+8 \times 35$-fF pixel capacitance +300 fF from bias circuitry). Reducing R_j to $\sim$ 1 kΩ will allow increasing the number of elements in a row to $\sim$ 426 elements while maintaining the 10-MHz modulation frequency in the parallel mode (in Fig. 1). The corresponding capacitive load is $\sim$ 16 pF (0.8-pF input capacitance of on-chip amplifier $+426 \times 35$ fF pixel capacitance +300-fF from bias circuitry). It will take $\sim$ 20 μs to read from the entire array or a frame rate of $\sim$50 000 frames per second should be possible. Compared with the active pixel, when the number of pixels per row is increased to 426, the fill factor, the ratio between the pixel area including the ground plane to total area to $\sim$ 96% for this passive pixel architecture.

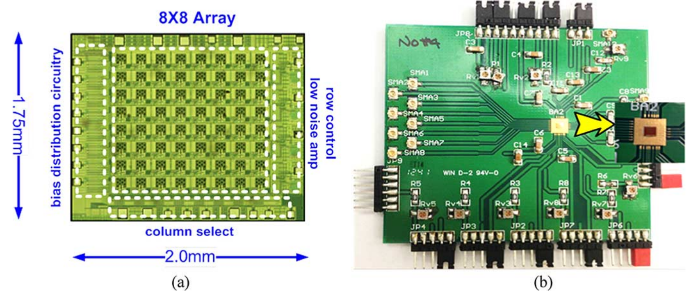


Fig. 14. (a) Microphotograph of 8×8 imaging array. (b) Photograph of imaging array on a printed circuit board.

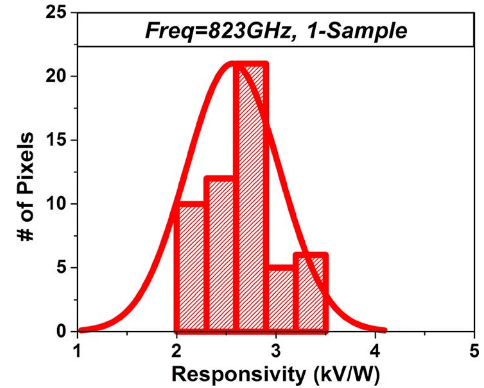


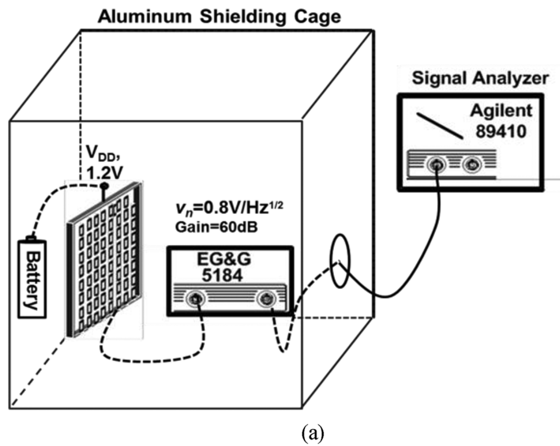
Fig. 15. Measured variations of responsivity at 823 GHz among 64 pixels of an imaging array.

V. Measurement Results

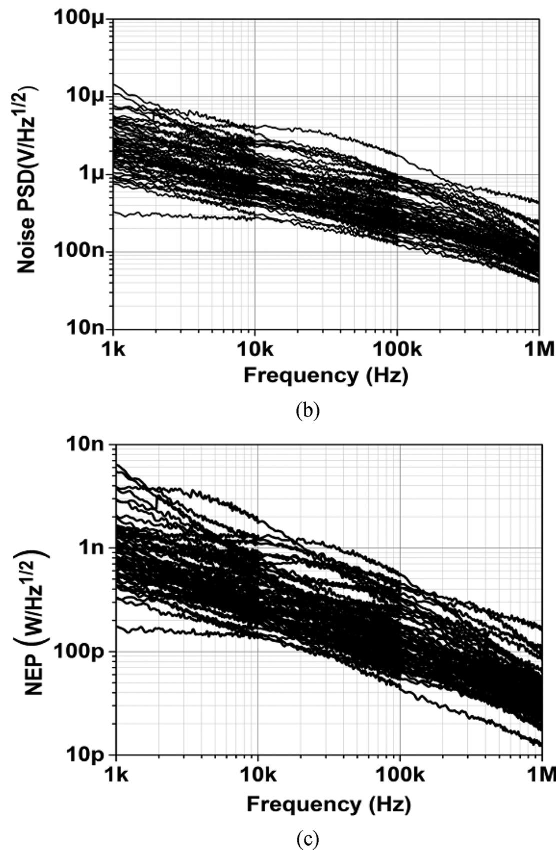
The measured output RMS voltage of imaging array is [8], [27] related to the responsivity by

$$\Re_v = \frac{\frac{\pi}{\sqrt{2}} V_{\rm rms}}{A_R \frac{P_{\rm cw} G_T}{4\pi r^2}} \tag{9}$$

where $V_{\rm rms}$ is the output voltage from a lock-in amplifier at a specified modulation frequency, $P_{\rm cw}$ is the radiated power of the continuous wave from a transmitter, G_T is the transmitter horn antenna gain (25 dB), A_R is the pixel aperture size (physical area of a single pixel), and r is the distance from the transmitter antenna to the imaging array.



(a)



(b)

(c)

Fig. 16. (a) Noise measurement setup. (b) Measured output noise of 64- pixels. (c) NEP of 64-pixels in an imaging array.

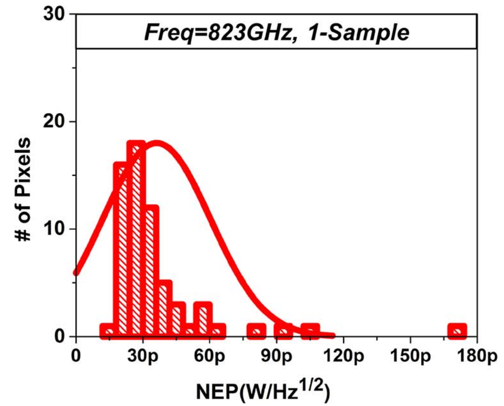
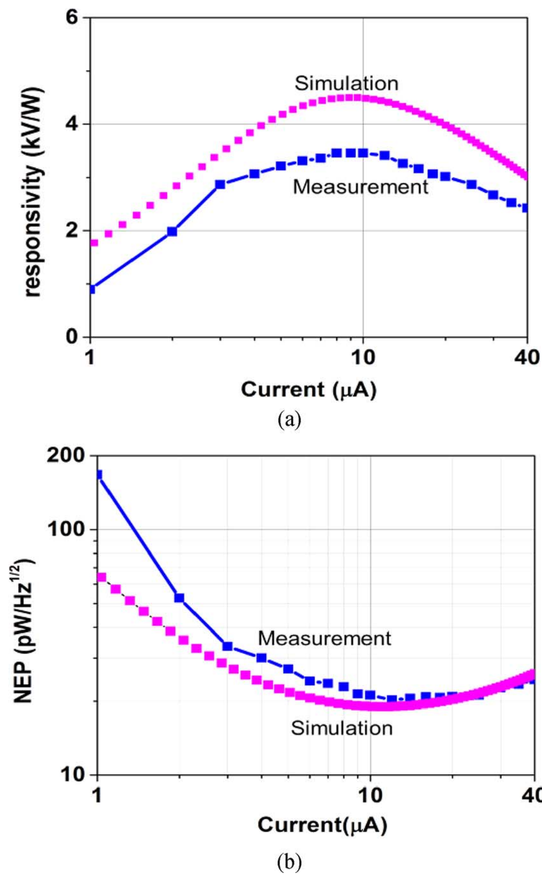


Fig. 17. Measured variation of NEP at 823 GHz and 1-MHz modulation frequency among 64 pixels of an imaging array.

The measurement setup is illustrated in Fig. 13 [8]. Fig. 14(a) and (b) shows a die photograph of the imaging integrated circuit and a photograph of the imaging array mounted on a printed circuit board with a biasing circuitry. An 11.17–12.05-GHz signal from an Agilent E8257D is fed into a VDI amplifier-multiplier-chain (AMC $\times$ 24) followed by a frequency tripler to generate a signal at 804–867 GHz. The signal is then radiated using a horn antenna. The output power of frequency multiplier is measured using an Erickson PM4 power meter while sweeping the frequency. The PCB containing the imaging array is directly mounted and aligned to the horn antenna at a distance ranging from 15 to 45 mm. An SR844 lock-in amplifier provides a TTL signal up to 1 MHz for modulation of the RF signal while simultaneously locking the detector output signal. The responsivity versus frequency plot for the sample with the median responsivity at 823 GHz is shown in Fig. 10(a). The responsivity was measured at a distance between the source and imager of 45 mm to mitigate the standing wave effect. The responsivity peaks at 823 GHz, and the median responsivity at 823 GHz is $\sim$ 2.6 kV/W including the 13.5-dB gain of on-chip amplifier. The measured maximum responsivity is $\sim$ 3.5 kV/W at 823 GHz. The maximum responsivity of detector by itself is 720 V/W at 823 GHz. Fig. 10(a) also shows the measured CW power from the source and the median responsivity.

Fig. 15 shows the distribution of responsivity at 823 GHz for the 64 pixels of an imaging array. The mean responsivity is 2.56 kV/W and with a standard deviation of 0.47 kV/W. The output noise of each pixel of an imaging array is measured using an EG&G 5184 external low-noise amplifier (input referred noise of 0.8 nV/Hz$^{1/2}$ and 60-dB gain) and a vector signal analyzer (Agilent 89410A) shown in Fig. 16(a). At 1-MHz modulation frequency, the output noise is dominated by flicker noise as shown in Fig. 16(b). The noise varies by an order of magnitude among the pixels. The flicker noise corner frequency is $\sim$ 6 MHz. The measured median NEP (median noise power spectral density/median responsivity) at 1-MHz modulation frequency versus frequency is also shown in Fig. 10(b). The NEP is minimized around 820 GHz. The mean NEP of array is 36 pW/Hz$^{1/2}$. The standard deviation of the NEP for the 64 pixels is 24 pW/Hz$^{1/2}$ and the distribution is shown in Fig. 17.

The measured peak responsivity frequency is $\sim$ 20 GHz lower than that of simulations. This corresponds to an around 2% shift of the peak frequency from the simulations. This is surprising especially in light of the fact the models in the CMOS process used for this work are rated for designs up to $\sim$ 10 GHz. This difference can easily be explained by wafer-to-wafer and run-to-run variations of dielectric layer thicknesses as well as the parasitic capacitances of matching elements and NMOS transistors. The measured peak responsivity is $\sim$ 2$\times$ lower. The parasitics of transistors in Fig. 3 determine the power degradation factor. The modeling uncertainty of these parasitics in combination with the dielectric layer thickness variations which affect the impedance matching and antenna performance



(a)

(b)

Fig. 18. (a) Simulated and measured responsivity of imaging element with the maximum responsivity at 823 GHz and 1-MHz modulation frequency versus pixel current. (b) Simulated and measured NEP of imaging element with the maximum responsivity at 823 GHz and 1-MHz modulation frequency versus pixel current.

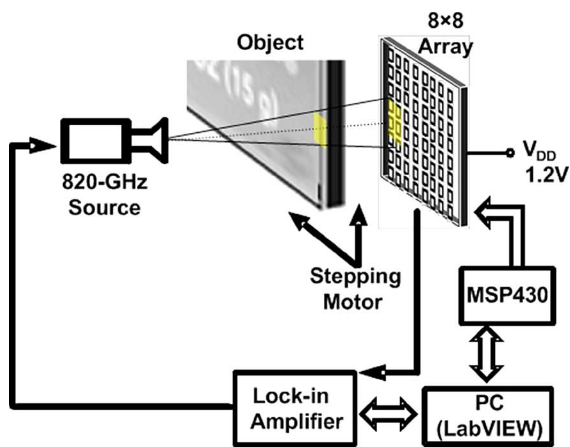
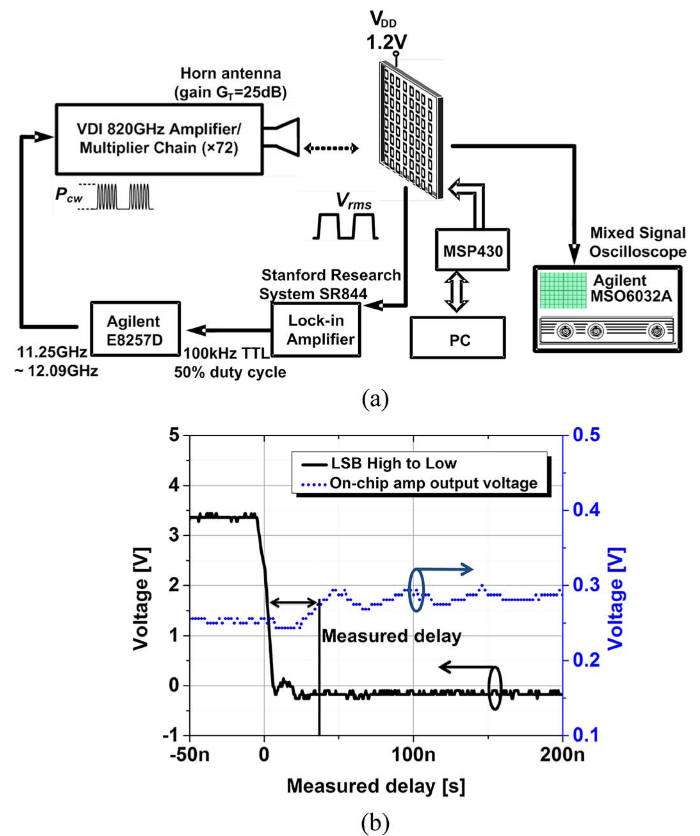


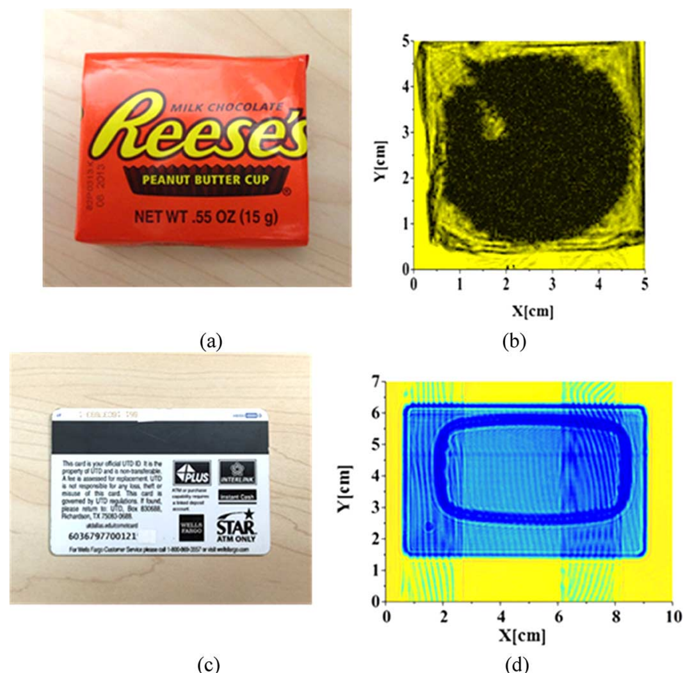
Fig. 19. THz lens-less active imaging setup.



(a)

(b)

Fig. 20. (a) System delay measurement setup and (b) measured on-chip amplifier output waveform (dotted line) when the LSB of the column decoder is changed to high from low (solid line, measured from MSP board).



(a) (b)

(c) (d)

Fig. 21. Images from the lens-less imaging setup.

may explain the $\sim 2\times$ lower measured responsivity. This in turn will explain the $\sim 2\times$ higher measured NEP.

Fig. 18(a) and (b) plot the simulated and measured responsivity and NEP at 823 GHz versus the diode current of the pixel with the maximum responsivity, respectively. Because of the comparison using the data for the sample with the maximum responsivity, the difference between the measurements and simulations are smaller than in Fig. 10. The simulated peak responsivity is within 40% of the measurements while the simulated minimum NEP is almost the same as that of measured. An operating frequency of 823 GHz was chosen because it is the frequency at which the responsivity is the highest and

TABLE I
PERFORMANCE COMPARISON OF THZ DETECTORS

References	Technology	Array size	Max Rv [V/W]	Minimum NEP [pW/$\sqrt{Hz}$]	Chopping Frequency	Pixel Multiplexing
			Un-cooled Bolometer			
‡[30]	200-nm CMOS ASIC	320×240	12.6M, 2.5 THz	6.4, 2.5THz	-	-
			Active imaging in room temperature			
†[15]	250-nm bulk	3×5	80k, 0.6 THz	300, 0.6 THz	30 kHz	No
†‡[9]	65-nm bulk	32×32	*115k, 0.86 THz	12000, 0.86 THz	-	Yes
			**140k, 0.86 THz	100, 0.86 THz	5KHz	
†‡[16]	65-nm bulk	3×5	800, 1 THz	66, 1 THz	1 kHz	No
†[11]	130-nm bulk	3×4	2.53k, 0.3 THz	-	400 Hz	-
§[18]	SBD in 130-nm bulk	2×2	250, 0.28 THz	33, 0.28 THz	1 MHz	No
§[8]		4×4	336, 0.28 THz	29, 0.28 THz		Yes (dual mode)
		single pixel	273, 0.86 THz	42, 0.86 THz		No
§This work	130-nm bulk	8×8	¦3.46k, 0.823 THz +2.56k, 0.823 THz	¦¦12.6, 0.823 THz ++36.2, 0.823 THz	1 MHz	Yes (dual mode)

Terahertz detector rectification is analyzed based on †distributed resistive self-mixing and §diode non-linear I-V relationship.
‡Silicon lens integrated to the chip.
*Video mode and **Non-video mode includes 5-dB off-chip VGA.
¦Maximum responsivity (including on-chip amplifier). ¦¦Minimum NEP.
+Mean responsivity. ++Mean NEP.
Unlike the previously reported NMOS sub-millimeter wave detectors, because the diode connected transistors are biased, the detector has 1/f noise even when RF input is zero. Because of this, the modulation frequency for this system is near 1 MHz instead of 1kHz to 100 kHz of the other MOS detectors.

NEP is the lowest. The measured responsivity peaks at 10-μA bias current. The corresponding responsivity and NEP are 3.46 kV/W and 21.2 pW/Hz$^{1/2}$, respectively. From the same pixel, the measured minimum NEP occurs at 12-μA bias current. The noise PSD at a modulation frequency of 1 MHz is 69 nV/Hz$^{1/2}$, which corresponds to the minimum NEP of 20.2 pW/Hz$^{1/2}$. The minimum NEP at 10-μA bias current among all the pixels is 12.6 pW/Hz$^{1/2}$. This is the lowest measured NEP for a THz detector fabricated in CMOS. The 8×8 imaging array occupies 2.0×1.7 mm^2 and the power consumption is 9.6 mW.

VI. THz Imaging

The imaging array was used in an imaging set up that does not require an external mirror or a lens to form images [8]. The setup in Fig. 19 consists of a THz radiation source, an imaging array chip on a PCB, a lock-in amplifier discussed in Section III, and an MSP430 board [28] for controlling the pixel selection. The entire system is controlled using LabVIEW [29]. Fig. 20(a) shows the setup for measuring the delay from the MSP430 board to an Agilent MSO6032A oscilloscope. While the column decoder output is changed from 001 to 000 (dashed line shows the waveform of least significant bit from the MSP430 board), the output voltage of the on-chip amplifier is measured using the oscilloscope. An external 1-nF capacitance shunt with a 40-Ω resistor is added at the output of the on-chip amplifier to prevent oscillation in the serial mode. The input impedance of the oscilloscope is 1 MΩ. The system delay is defined at the 50% point of the input and output waveforms in Fig. 20(b). The measured system delay is $\sim$ 40 nS. Noting the simulated delay through the on-chip amplifier of $\sim$ 15 nS and the delay associated with driving the decoder from the MSP430 board, this result is consistent with the 16-nS simulated delay from the decoder to the input of the on-chip amplifier.

In the current setup, the scanning time is limited by the mechanical stepping motors and communication latency between LabVIEW and the lock-in amplifier. Fig. 21(b) and (d) show 823-GHz images of a chocolate with an intentionally melted region and an identification card, respectively formed by the imaging array. The transmitted power was 200 μW, and the spacing between the transmitter and object and that between the object and imaging array was 15 mm, while the lock-in amplifier integration time was 10 mS. In Fig. 21(b), the shape of chocolate in the package and melted region (white colored) are evident. In Fig. 21(d), a metal coil in the card is easily seen. Additionally, scotch tape strips used to mount the card are also seen. The image SNR (ratio between the brightest and darkest areas) is 70 dB.

VII. Conclusion

An 820-GHz 8×8 imaging array utilizing a diode-connected NMOS transistor detector has been demonstrated in a 130-nm CMOS process. By utilizing a passive pixel scheme with four low noise amplifiers, this imaging array achieved a measured peak responsivity of 3.46 kV/W and the associated NEP at 1-MHz modulation frequency of 21.2 pW/Hz$^{1/2}$. The mean responsivity is 2.56 kV/W with a standard deviation of 18%. The mean NEP at 1-MHz modulation frequency is 36.2 pW/Hz$^{1/2}$ with a standard deviation of 67%. The minimum NEP at 1-MHz modulation frequency including the noise from the on-chip amplifier is 12.6 pW/Hz$^{1/2}$, which is the lowest measured among all THz detectors fabricated in a CMOS process. The performance of state-of-the-art CMOS active imaging arrays are compared in Table I. The NEP of imaging array in this

work is competitive to that of the best NMOS and Schottky diode detectors fabricated in CMOS. Compared to a bolometer array fabricated using a post CMOS fabrication process [30], the NEP is around 5 × higher. This work has also shown that the responsivity and NEP significantly vary. As the detector operating frequency is increased, it is inevitable that the device size will decrease. This of course is expected to increase the variability and approaches to reduce the variations will be required. As a matter of fact, the variability may turn out to be the factor that determines the viability of a device for THz detection. The measured mean responsivity and mean NEP are within a factor of two of simulated. Given the simplistic non-quasi-static model used for the simulation compared to the models in [13] and [31], the discrepancies are surprisingly small and are perhaps reasons for hope of reliably simulating detectors operating near THz.

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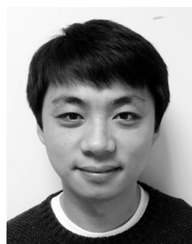

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