On-Chip Terahertz Electronics: From Device-Electromagnetic Integration to Energy-Efficient, Large-Scale Microsystems

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***Abstract*—**This paper summarizes our approaches which synthesize the optimum electromagnetic (EM)-wave environment around various silicon devices, in order to maximize the device efficiency with minimum passive loss and footprint. This has enabled multi-mW THz radiation in standard silicon processes. Various critical capabilities for future THz microsystems, including integrated phase locking, multi-pixel coherent imaging, and an ultra-broadband inter-chip waveguide link, are also demonstrated.

I. Introduction

Terahertz integrated circuits, especially those implemented in silicon, have emerged as a technology with low cost and wave processing capability of unprecedented complexity and precision. One exciting fact is, although the maximum oscillation frequency (f_{max}) of silicon transistors has not improved significantly with the recent device scaling technologies [1], both the THz radiated power and DC-to-THz efficiency have increased by four to five orders of magnitude [2] since the debut of CMOS THz sources in 2008 [3], [4]. This paper presents an overview of our work ranging from device analysis and integration with EM structures, to THz microsystems and new interconnect infrastructures. This progress clearly demonstrates the feasibility and great potential of THz circuits with large-scale integration and enhanced energy efficiency for non-invasive inspection, material identification and high-speed links.

II. Pushing the Device Limits for THz Generation

Due to the low f_{max} of transistors, signal amplification near f_{max} and harmonic power generation above f_{max} are normally performed simultaneously. A circuit example of this category is the harmonic oscillator, which can be generalized as a single device surrounded by a passive or active network (Fig. 1(a)). When the signal frequency approaches f_{max}, the drain current of a MOSFET has a significant delay with respect to the gate voltage v_g (Fig. 1(b)) [5], [6]. The delay is caused by the input *R-L-C* gate network, the transit time inside the channel, and the feed-forward current through the gate-drain parasitic capacitance (represented as $\Delta\varphi_1$ and $\Delta\varphi_2$ in Fig. 1(b)). To maximize the output power, the drain voltage v_d should keep in phase with the drain current, requiring an additional phase shift $\Delta\varphi_{opt}$ in the device voltage gain A_{f0} beyond the typical signal-inversion behavior. Such phase shift is approximately 30° in 65-nm CMOS processes [5], [6], and is as large as 90° in 130-nm SiGe HBT process [7]. If the phase of the transistor voltage gain is configured to be 180° (as in traditional oscillator designs), the output power is shown to be reduced by 4x in MOSFETs (Fig. 1(c)) [6] and even becomes negative (i.e. the transistor no longer amplifies) in SiGe HBTs [7]. Next, to maximize the harmonic generation efficiency, another device condition—harmonic-signal isolation between device terminals, is also required. This is particularly important for the commonly used multi-push oscillator design, where the reverse harmonic feedback factor (β_{2f0} in Fig. 1(a)) from the drain to the gate is close to unity; it causes not only significant harmonic-signal loss at the transistor gate, but also negative feedback through the device [6]. In comparison, if isolation between gate and drain at the desired harmonic is achieved, the output THz power improves by 5x in the simulation shown in Fig. 1(d). These analyses, applicable for both silicon and non-silicon transistors, indicate the potential of ~20-dB improvement towards useful THz power generation. This calls for new circuits to optimize the device operations.

Our first work addressing this issue is based on a loop of synchronized 260-GHz harmonic radiators in 65-nm CMOS (Fig. 2(a)) [6], [8]. Each radiator consists of a pair of magnetically-coupled "self-feeding" oscillators. A self-feeding oscillator uses a transmission line to connect the device gate and drain, and allows independent control of the traveling and standing wave components inside the line. At 130 GHz, a traveling wave is dominant; and with proper line length, it causes the transistor to oscillate with the optimum voltage gain phase. At 260 GHz, a standing wave is dominant, which prevents power leakage from the drain to the gate. Using 8 slot antennas, our chip is the first THz CMOS chip that generates milli-watt radiation (1.1 mW). Through an on-chip narrow-pulse amplitude modulation, the chip also offers a bandwidth of 25 GHz for spectroscopy and radar applications (Fig. 2(b)). The THz modulator is based on a pair of MOS varactors forming a tunable resonance, which exhibits an extinction ratio that is 2.3x higher than that of NMOS switch using resistive modulation in the device channel.

To further increase the output power, efficiency and radiator density, devices are tightly integrated with multi-functional EM structures supporting orthogonal wave modes. This is illustrated in a recent 320-GHz radiator work (Fig. 3) using a 130-nm SiGe HBT process [7], [9]. Each radiator is based on a "return-current-path gap" that couples two self-feeding oscillators. The gap, behaving as a two-conductor waveguide, supports the 160-GHz differential oscillation wave in quasi-TEM mode, while fully blocking the base-generated, in-phase 2nd-harmonic signals in TM mode (Fig. 3(b)). The aforementioned device operation conditions are therefore achieved. In addition, a pair of folded slots at the top of the structure behave as quarter-wave resonators at 160 GHz while creating 4 standing waves at 320 GHz. The standing waves are in phase, leading to backside radiation with ~50% efficiency. Without separate antennas, such a compact design enables integration of 16 synchronized radiators inside only 0.8-mm^2 area. The combined radiated power of

the array is 3.3 mW (Fig. 3(c)), representing the highest THz power in silicon reported to date. Due to the large beam collimation (~54x), the effective isotropic radiated power of the source is 0.18 W. Through a fully-integrated phase-locked loop (PLL), the output is also stabilized to an external 0.3-GHz clock, exhibiting a phase noise of -87 dBc/Hz at 10-MHz offset.

An alternative approach for THz generation is frequency multiplication. Although frequency multipliers require high input power in the sub-THz range and cannot be implemented in an array with power combining, they can be fully passive and provide a large tuning range. These advantages are demonstrated in a 480-GHz CMOS doubler using thick-gate, accumulation-mode MOS varactors [10]. When the channel length is 0.4 μm, the varactor exhibits a dynamic cutoff frequency of 0.9 THz and an optimal conversion efficiency of 11% (Fig. 4(a)). The doubler is based on a broadband ring structure with a magnetic-coupling interface for odd-mode signal injection at 240 GHz and an electrical combining interface for even-mode signal extraction at 480 GHz (Fig. 4(b)). These operations are frequency independent and exhibit ~1-dB measured output power fluctuation in a 20-GHz band. The output power of this doubler is 0.23 mW without saturation (equipment limited), and should exceed 1 mW before the gate oxide breakdown (Fig. 4(c)).

III. Towards High-Performance Microsystems

Multi-mW power generation in silicon has opened up numerous opportunities in new sensing and communication paradigms using low-cost THz microsystems. Using Schottky diodes with 2-THz cutoff frequency [11], we have reported antenna-fed detectors and multiplexed imaging arrays in a 130-nm CMOS process with a noise equivalent power (NEP) of 29 $pW/Hz^{1/2}$ at 0.3 THz and 42 $pW/Hz^{1/2}$ at 0.9 THz [12]. The sensitivity of these imagers, as well as other sensor work using silicon MOSFETs [13], is already comparable to that of III-V diode detectors [14], though it should be further improved to reduce the required THz power and energy consumption of source chips. For this purpose, coherent heterodyne detection is proposed with a simulated improvement of 10^4~10^5x (Fig. 5(a)). A chipset prototype in a 130-nm SiGe process is demonstrated by pairing our 320-GHz phase-locked transmitter with an array of subharmonic mixers (Fig. 5(b)) [15]. The local-oscillator signals of the mixers are generated from a THz PLL identical to that in the transmitter. The measured sensitivity with 1-kHz integration bandwidth is 70~80 pW (Fig. 5(c)), representing a 10x improvement compared to the prior incoherent sensors. Since the intermediate-frequency outputs preserve the phase of the local incident THz waves, when they are phase shifted and then summed in the digital domain, the resultant interference leads to a highly-directive sensor response. Electronic control of the phase shifting then enables rapid 2D steering of the sensing direction, which should eliminate the slow and bulky mechanical scanners inside current THz imagers. For high scanning resolution, large-format heterodyne sensors are needed and require new compact pixel design and a decentralized, scalable array architecture for high fill factor and energy-efficient operations.

Terahertz operation of integrated circuits also brings new capabilities to traditional electronic systems. High-speed, inter-chip communication is one of these exciting applications. Inter-chip wireless links have been reported [16], [17], but the energy efficiency and transmission distance are still poor due to the free-space path loss. These problems are expected to be solved by confining the THz wave inside low-loss dielectric waveguides. One critical part of this scheme is a broadband, efficient interface between the on-chip electronics and waveguide. Fig. 6(a) presents our design and prototype of a wave coupler utilizing only the back-end-of-line (BEOL) inside a standard 130-nm silicon chip [18]. Based on a leaky waveguide structure, the coupler fully shields the input THz wave from the lossy silicon substrate. By launching an anti-symmetric wave inside the coupler, a high-intensity, horizontal electrical field is exposed to the dielectric waveguide and matches the wave distribution of the desired fundamental waveguide mode. The coupler is also tapered with increasing cutoff frequency, which further "squeezes" the energy into the waveguide as the wave travels. The single-mode waveguide is made of laser-cut, low-cost Rogers 3006 material. Fig. 6(c) shows the measurement results of two back-to-back test structures using a 1-cm straight waveguide and a 2-cm waveguide with 2 bends. The links exhibit small average insertion loss (~11 dB) and dispersion. Both the 250-GHz center frequency and the 50-GHz bandwidth are the highest reported to date in inter-chip waveguide links. More importantly, the loss difference between the two links is indiscernible, indicating excellent transmission property of the THz waveguide. In server and radar backplanes, CMOS and SiGe I/O circuits built upon this infrastructure are expected to overcome the speed and efficiency bottlenecks of metal interconnects and solve the integration and temperature-sensitivity issues of photonic interconnects.

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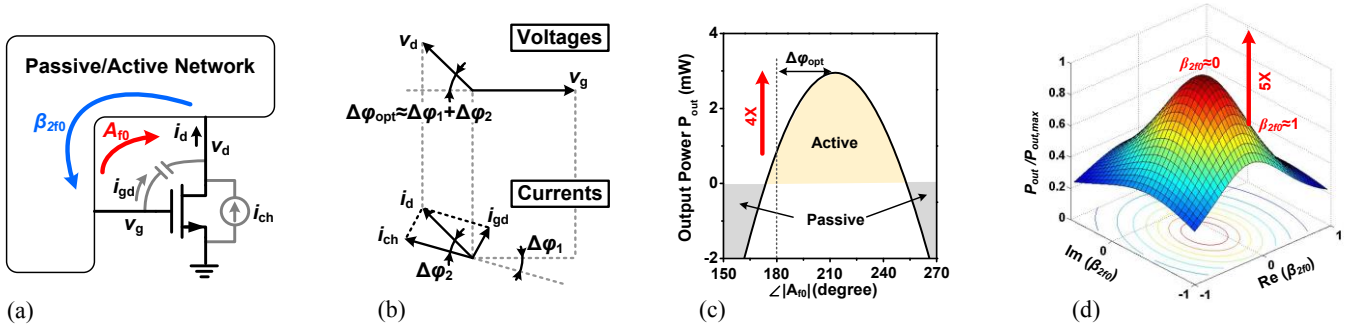

Fig. 1. (a) A generalized circuit scenario for a transistor-based THz source. (b) Extra phase shift requirement of device voltage gain caused by the device intrinsic delay and feedforward current. (c) Simulated fundamental output power (at 130 GHz) with varying gain phase of a NMOS (W/L=27μ/65n). (d) Normalized 2nd-harmonic (at 260 GHz) output power of the same device with varying harmonic feedback factor.

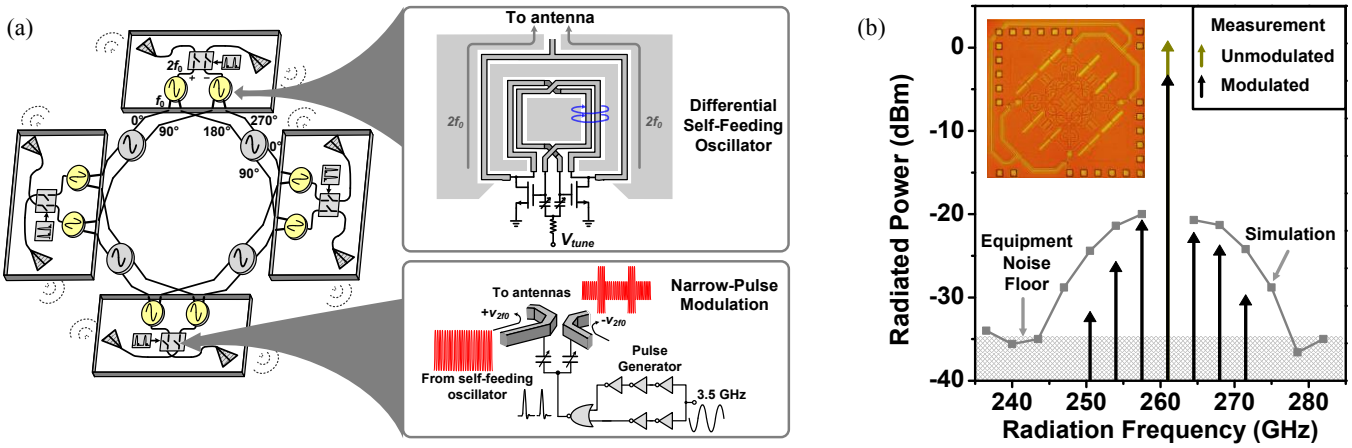

Fig. 2. A CMOS 260-GHz radiation source: (a) schematic, (b) chip micrograph and measured output power.

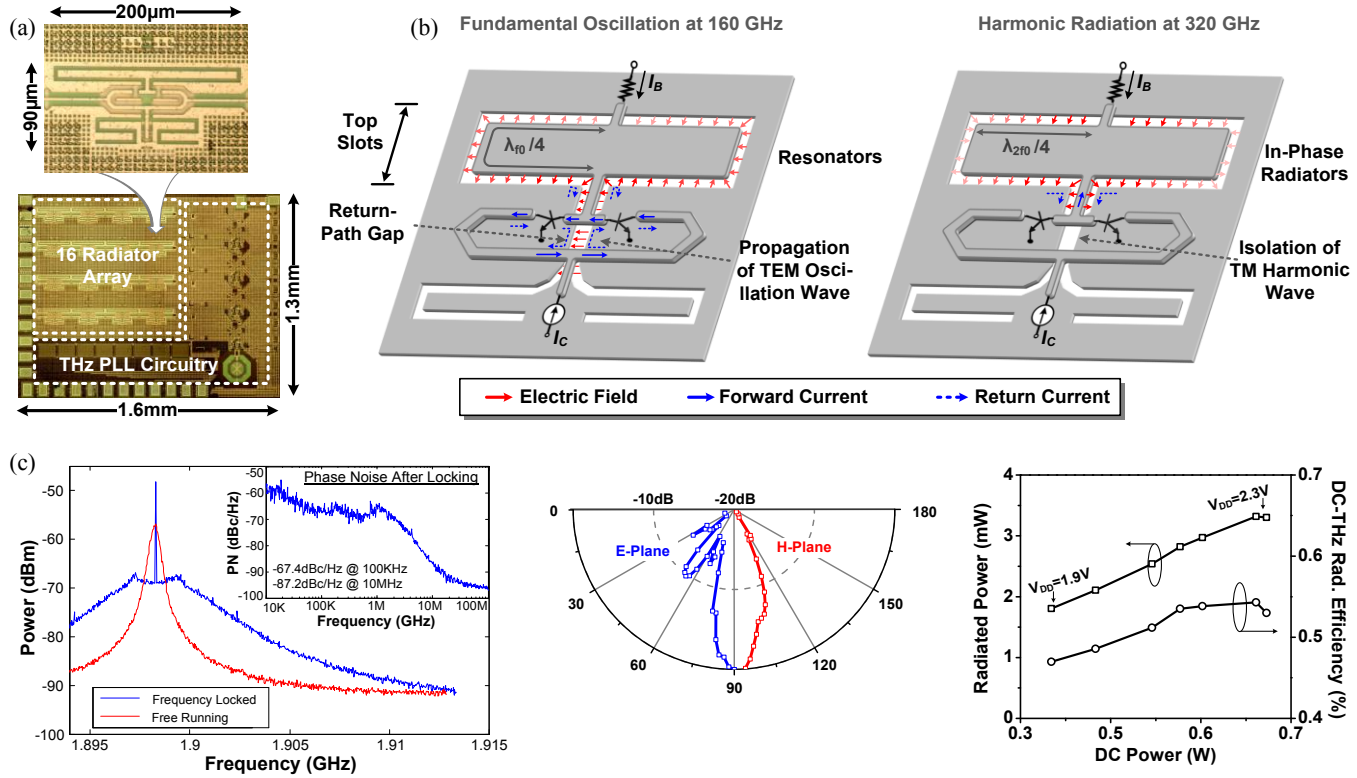

Fig. 3. A 320-GHz phase-locked radiator array using SiGe HBTs (a) chip micrograph, (b) field distribution of a radiator unit, and (c) measured phase noise spectrum, pattern and power of the radiated THz signal.

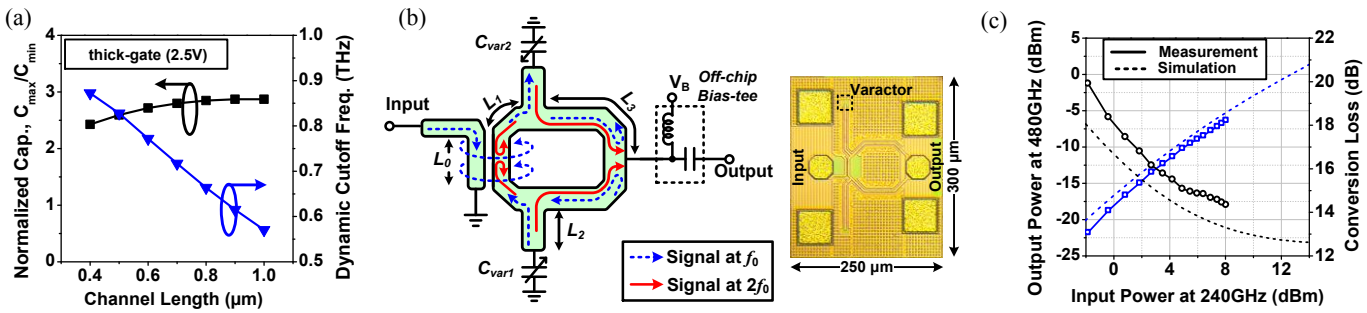

Fig. 4. (a) Capacitance tuning range and dynamic cutoff frequency of accumulation-mode MOS varactor. (b) A CMOS 480-GHz doubler based on a coupled ring structure. (c) Simulated and measured output power and conversion loss.

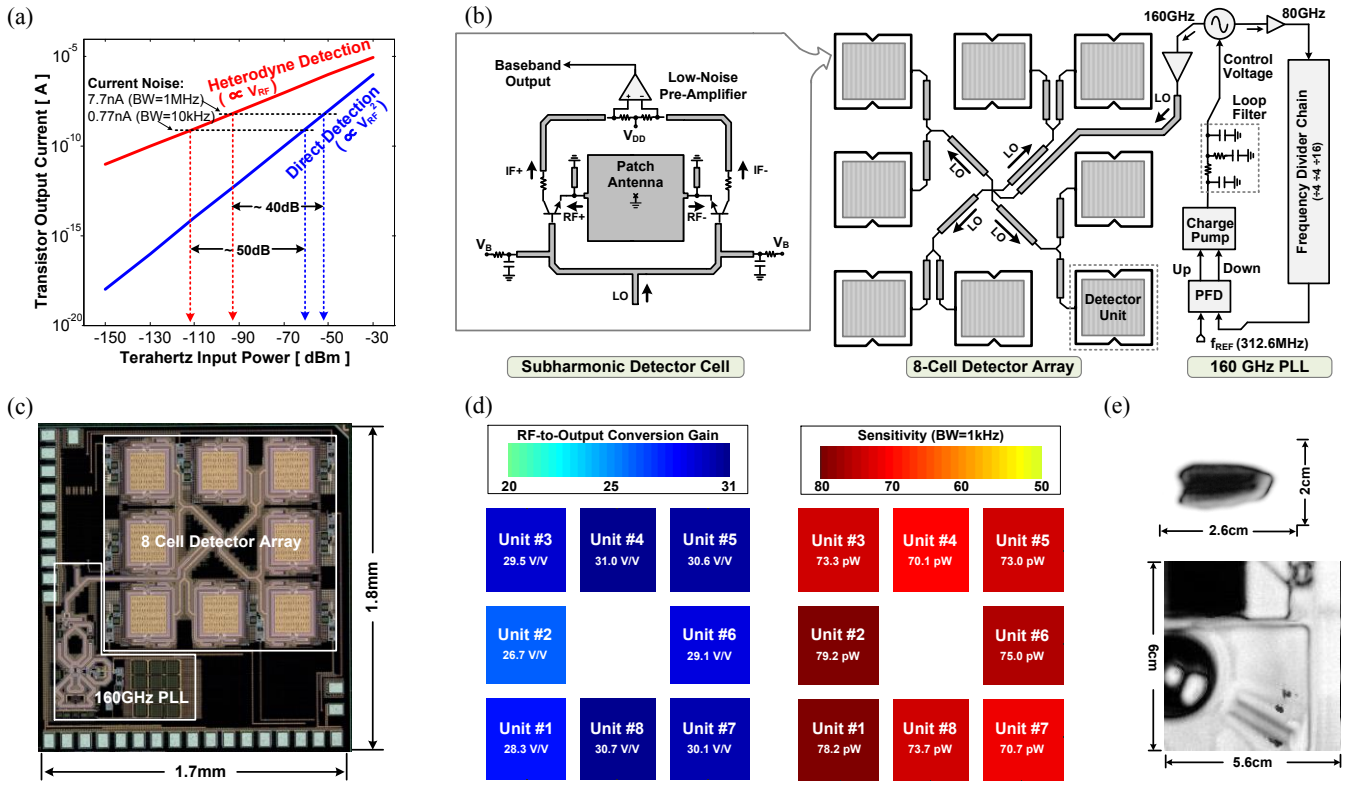

Fig. 5. (a) Comparison between heterodyne detection and direct detection. (b) Schematic, (c) chip micrograph and (d) measured conversion gain and sensitivity of a 320-GHz heterodyne sensor array. (e) Images of a human tooth and a floppy disk constructed using the 320-GHz SiGe transmitter and the 320-GHz SiGe sensor array.

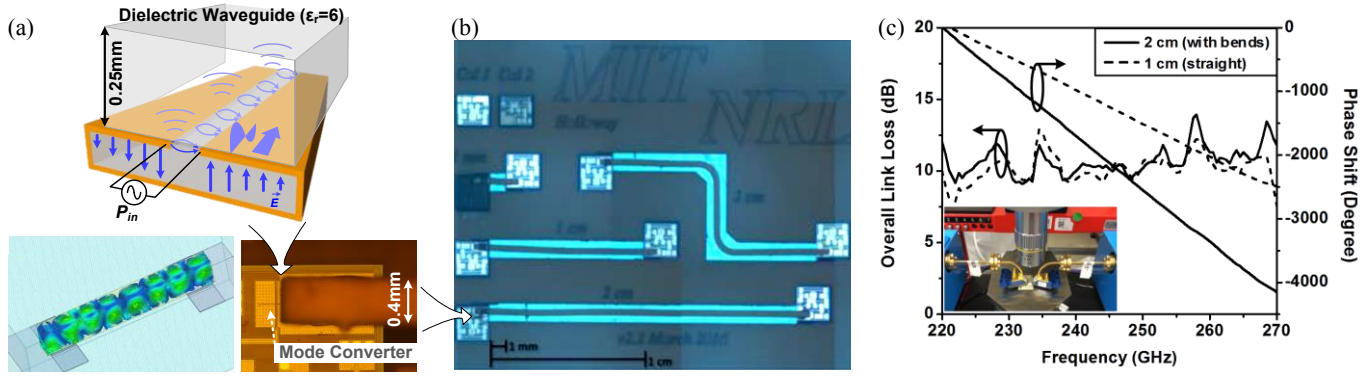

Fig. 6. (a) A fully-integrated, broadband leaky structure that couples a silicon chip and a dielectric waveguide. (b) Test structures of the inter-chip THz links. (c) Measured back-to-back loss and dispersion of the links.