A SiGe Terahertz Heterodyne Imaging Transmitter With 3.3 mW Radiated Power and Fully-Integrated Phase-Locked Loop

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***Abstract*—A high-power 320 GHz transmitter using 130 nm SiGe BiCMOS technology ($f_T/f_{\max}$ = 220/280 GHz) is reported. This transmitter consists of a 4 × 4 array of radiators based on coupled harmonic oscillators. By incorporating a signal filter structure called return-path gap coupler into a differential self-feeding oscillator, the proposed 320 GHz radiator simultaneously maximizes the fundamental oscillation power, harmonic generation, as well as on-chip radiation. To facilitate the TX-RX synchronization of a future terahertz (THz) heterodyne imaging chipset, a fully-integrated phase-locked loop (PLL) is also implemented in the transmitter. Such on-chip phase-locking capability is the first demonstration for all THz radiators in silicon. In the far-field measurement, the total radiated power and EIRP of the chip is 3.3 mW and 22.5 dBm, respectively. The transmitter consumes 610 mW DC power, which leads to a DC-to-THz radiation efficiency of 0.54%. To the authors' best knowledge, this work presents the highest radiated power and DC-to-THz radiation efficiency in silicon-based THz radiating sources.**

***Index Terms*—Terahertz, transmitter, BiCMOS, SiGe, radiated power, EIRP, phase-locked loop, heterodyne imaging, return-path gap.**

I. Introduction

ELECTROMAGNETIC radiations in the terahertz range have demonstrated great potential in the imaging applications for biomedicine, security, and industrial quality control [1]–[3], due to its high spatial resolution (compared to millimeter wave) and non-ionizing natures (compared to X-ray). At present, the barrier to the wide application of this emerging sensing technology is mainly due to the difficulty of the high-power signal generation. Conventional THz sources include quantum-cascade laser (QCL) [4], photoconductive emitter [5], vacuum electronics [6], and III-V Schottky diode multiplier chain [7]. However, these solutions have significant drawbacks, such as the high cost, large form factor, and stringent operation conditions (e.g., cryogenic cooling for QCL). Because of these, active THz imaging microsystems using integrated circuit technology are drawing increasing attention. In particular, imagers based on CMOS and BiCMOS processes are expected to not only resolve the above problems, but also achieve a high systematic integration level and high yield [8], [9]. This enables portable THz imaging equipment with a low cost.

However, there are several challenges towards this goal. First, the radiated power of existing THz transmitters is still insufficient. This is mainly due to the limited speed and breakdown voltage of the silicon transistors. The first THz CMOS radiator source reported in 2008 only generates 20 nW power at 410 GHz [10]. Since then, significant progress has been made with synergistic efforts in device, circuit, and electromagnetism. In [11], 390 μW power is obtained in the 288 GHz radiator based on a triple-push oscillator topology. In [12], the 338 GHz phased array achieves 810 μW power. In [13], a self-feeding oscillator array generates 1.1 mW radiated power at 260 GHz. Besides these work in CMOS, radiation sources in BiCMOS processes also demonstrate great potential, thanks to the superior speed and breakdown voltage of the SiGe heterojunction bipolar transistor (HBT) [14]. For example, radiators using a 130 nm SiGe BiCMOS process ($f_{\max}$ = 500 GHz, V_{CEO} = 1.6 V) achieve 1.3 mW of power at 245 GHz [15]and 74 μW (single element)/1 mW (incoherent array) of power at 530 GHz [16]. Fig. 1(a) summarizes these results, which follow a $P_{\mathrm{out}} \propto 1/f^3$ to $1/f^4$ relationship. To some extent, larger total radiated power can be obtained through the combination of an increased number of array elements. By comparison, the DC to THz radiation efficiency is more relevant to the performance of the devices and basic circuit blocks. It is particularly important for energy and thermal limited portable systems. Within less than a decade, the DC to THz radiation efficiency of silicon sources has increased by over 1000x (Fig. 1(b)). However, due to the approach of harmonic generation, the absolute efficiency level is still low. Previously reported highest DC to THz radiation efficiencies are 0.14% in CMOS [11], [13]and 0.33% in SiGe BiCMOS [15].

The challenge of the on-chip active THz imaging system also resides in the receiver side. Due to the lack of power amplification for THz signals ($f_{\mathrm{in}} > f_{\max}$), focal-plane arrays in silicon rely on the direct passive detection using nonlinear devices, such

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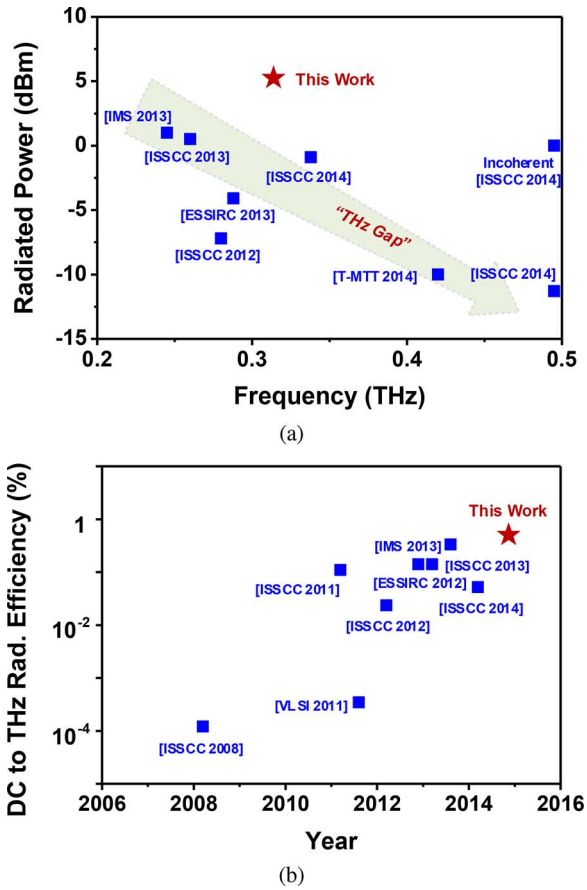


Fig. 1. The performance of the state-of-the-art THz radiator sources in silicon: (a) the total radiated power at varying frequencies and (b) the achieved DC to THz radiation efficiency over the past few years.

as Schottky diode [8]and MOSFET [9]. This leads to limited sensitivity and further requires high-power generation from the transmitter. On the other hand, due to the Rayleigh diffraction limit [17]and the usage of resonant antenna coupling, the size of an imaging pixel at THz, especially at low-THz ($\sim$ 300 GHz) is large. It is therefore difficult to accommodate a large number of pixels on a single silicon die. Therefore, mechanical scanning is commonly used, which unfortunately prohibits the miniaturization of the imager and leads to long imaging time. To solve this issue, capability of electronic beam scanning is highly desired.

In this paper, we describe the development and characterization of a high-power 320 GHz transmitter, which was first presented by the authors in [18]. Using a 130 nm SiGe:C BiCMOS process ($f_T/f_{\max} = 220/280$ GHz, $BV_{\text{ceo}} = 1.6$ V [14]), this transmitter achieves a record total radiated power of 3.3 mW and DC to THz radiation efficiency of 0.54% (shown in Fig. 1). It also has a fully-integrated phase locking capability. Although a 300 GHz phased-locked loop (PLL) with a probed output power of 40 μW is presented earlier in [19], to our best knowledge, our work is the first demonstration of phase locking in high-power THz radiating source. In a heterodyne imaging system, phase locking between the transmitter and receiver enables significant sensitivity enhancement and digital beam forming for the receiver (not implemented in this work). The key to the high-power generation of this work is a new THz radiator structure based on a return-path gap coupler. Design details of this radiator are presented in Section II. Section III describes the overall architecture of the transmitter as well as the on-chip phase-locked loop (PLL). The experimental results of the SiGe prototype are given in Section IV. Finally, a performance comparison with the state-of-the-arts and a conclusion are given in Section V.

II. Radiator Design for High-Power and Energy-Efficient THz Generation

There are generally two approaches for generating THz signals in silicon: harmonic oscillators and frequency multipliers. While both approaches utilize the nonlinear harmonic generation of the devices, harmonic oscillators, which are self-sustaining, do not require external RF input, and are therefore normally more energy efficient [20]. Although they have smaller output tuning bandwidth compared to frequency multipliers [21], such issue is not critical for two-dimensional THz imaging. Therefore, the proposed THz radiator is based on a harmonic oscillator.

It is noteworthy that our radiator design follows a bottom-up, device-centric methodology. Terahertz circuits operate close to the activity-inactivity boundary of transistors; the performance is therefore highly sensitive to the device efficacy. We show in this section that, in our design, instead of inserting devices into conventional circuit topologies, the optimum conditions of a single SiGe HBT are first analyzed. Then, a novel electromagnetic-wave structure, called return-path gap coupler, is designed to achieve these conditions for the highest harmonic generation out of the HBT. In particular, this single structure simultaneously performs fundamental oscillation, harmonic generation, and on-chip radiation, hence minimizes the radiator loss and footprint.

A. Optimum Conditions for Harmonic Generation at THz

To maximize the harmonic output power from a radiating oscillator, the first step is to maximize the oscillation activity of the transistor at the fundamental frequency, f_0. In [22], an optimum complex voltage gain of a two-port active network ($A_{\text{opt}} = v_c/v_b$ for a SiGe HBT) is derived that maximizes the net power generated from the device. In particular, it is found that an extra phase shift beyond the conventional 180° inversion behavior of the transistor is needed. This is mainly due to the pico-second intrinsic delay of the devices, as well as the capacitive feedforward path between the two terminals (e.g., C_μ between the base and collector of an HBT) [13]. As one example, for a 130 nm SiGe HBT with a total emitter length of 4.5 $\times$ 2 μm and a collector current of 7 mA, the simulated optimum phase of the base-to-collector complex voltage gain is plotted in Fig. 2. It can be seen that at 160 GHz an extra phase shift of 89° is required. Unfortunately, conventional push-push oscillators [10]do not meet such optimum conditions, and therefore lead to smaller oscillation power. Triple-push topology ([11], [16], [22]) can achieve the optimum phase, but the 3rd-order harmonic generation is normally less efficient than the 2nd-order harmonic generation. Meanwhile, due to the ring topology, it is difficult to connect the oscillator output to an on-chip antenna, which is big in size ($\sim \lambda/2$). To solve this problem, in [13], we proposed a self-feeding oscillator design. The basic schematic of the oscillator is shown in Fig. 3, where the oscillation feedback path is formed via a transmission line. The transistor and

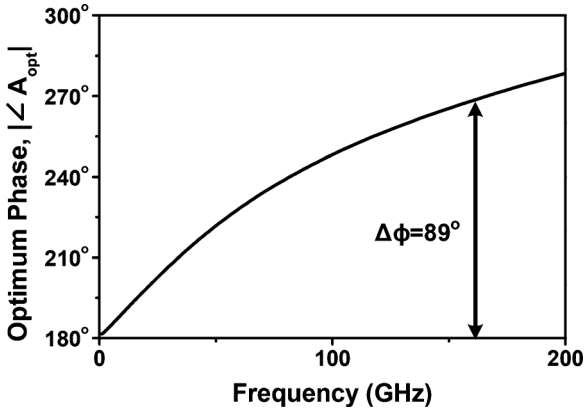


Fig. 2. The simulated optimum phase of the complex voltage gain for a 130 nm SiGe HBT ($L_e = 4.5 \times 2\ \mu$m). Please note that the phase of $A_{\rm opt}$ is negative, representing the physical delay from the input to the output of a transistor.

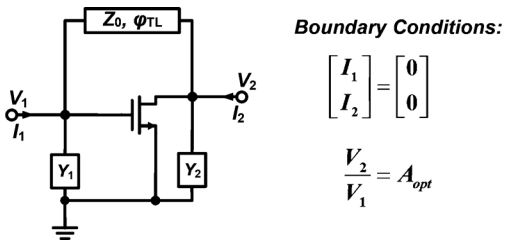


Fig. 3. The simplified schematic of the self-feeding oscillator proposed in [13]. For a self-sustaining oscillator with optimum transistor voltage gain $A_{\rm opt}$, the boundary conditions shown in the figure are required and lead to the relation derived in (1).

reactive components Y_1 and Y_2 are considered as the active and passive boundary conditions for the wave propagation inside the line. When the characteristic impedance, Z_0, and the electrical length, $\varphi_{\rm TL}$, of the self-feeding transmission line meet the following condition:

$$Z_0 \sin\varphi_{\rm TL} = \frac{A_{{\rm opt},I}}{g_{11} + {\rm Re}(A_{\rm opt} \cdot y_{12})}, \qquad (1)$$

the optimum gain $A_{\rm opt}$ of the device is achieved [13]. In (1), $A_{{\rm opt},I}$ is the imaginary part of $A_{\rm opt}$.

Secondly, for harmonic-signal generation, it is found that load impedance matching alone is not sufficient to fully optimize the generation efficiency [13]. In specific, harmonic-frequency isolation between the two terminals of a transistor is required, in order to avoid the self-power loading/cancellation effect. It is noteworthy that such harmonic isolation is not realized in conventional push-push oscillator or triple-push oscillator. The CMOS self-feeding oscillator in [13]achieves decent isolation by using a quarter-wavelength ($\varphi_{\rm TL} = \sim 90°$ at $2f_0$, or $\sim 45°$ at f_0) self-feeding line to transform the low gate impedance into a high impedance; the harmonic signal generated at the drain node is therefore blocked from the gate. This solution, however, has some limitations: (i) according to (1), the values of Z_0 and $\varphi_{\rm TL}$ are coupled. But, the $\varphi_{\rm TL}$ of $\sim 45°$ may result in a Z_0 that is too low or too high, depending on the particular devices. (ii) For SiGe HBT, the harmonic generation is most effective at the base junction of the device [16]. The above quarter-wavelength impedance transformation approach is therefore not feasible. So a new, more general harmonic signal isolation method is needed.

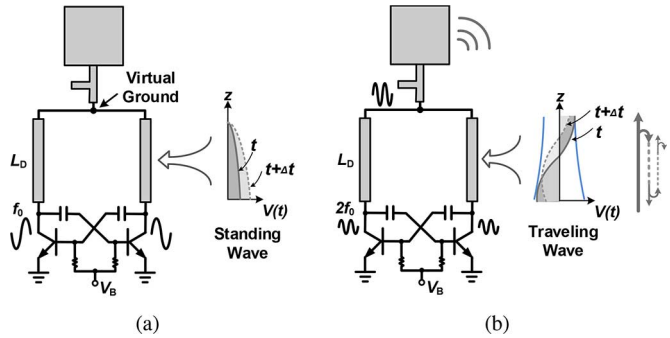


Fig. 4. A typical push-push oscillator: (a) differential standing-wave oscillation inside the near quarter-wavelength-long resonator, and (b) common-mode 2nd-harmonic signal extraction in the form of traveling wave with internal multi reflections.

Finally, in oscillators based on multi-push structure, it is common to use transmission lines or inductors to form resonance tank for the fundamental oscillation at f_0. At the end of the tank, where the multi-phase fundamental signals cancel, harmonic power is combined from these branches. Such configuration, however, introduces significant loss to the harmonic signal. Shown in Fig. 4, the 2nd-harmonic signal generated from the HBT needs to travel along the entire transmission line before it reaches the output antenna. Since at f_0, standing-wave oscillation is formed (Fig. 4(a)), the length of the transmission line is close to a quarter wavelength $\lambda_{f_0}/4$. This means at $2f_0$, the length of the line is near half wavelength $\lambda_{2f_0}/2$. More importantly, since impedance matching is only done at the output, significant multiple reflections normally occur inside the line (Fig. 4(b)). This further increases the ohmic loss for the harmonic signal [23]. Due to this reason, it is highly desired that the harmonic-signal radiation can occur right beside the devices. Although the distributed active radiator (DAR) structure proposed in [24] meets this requirement, it does not achieve the optimum conditions for fundamental oscillation and harmonic generation due to the usage of cross-coupled pair similar to the push-push oscillator.

In summary, to generate the maximum THz radiation, we need to achieve (i) optimum complex voltage gain of the transistor at f_0, (ii) harmonic isolation between the two terminals of the transistor at nf_0 (assume nth-harmonic signal is the output), and (iii) instant harmonic-signal radiation near the transistor. Unfortunately, to the best knowledge of the authors, no prior THz radiator design can simultaneously achieve these three conditions.

B. High-Power THz Radiator Design Based on a Return-Path Gap Coupler

To address the above issues, we propose a new second-harmonic $(2f_0)$ THz radiator in our transmitter. It is built on a differential self-feeding oscillator structure, so that the fundamental (f_0) oscillation power is maximized (Section II.A). Meanwhile, to achieve the harmonic-signal isolation (thus optimum harmonic generation efficiency), a signal filter is needed on the oscillator feedback path: it should be transparent to the oscillation signal at f_0, but opaque to the generated signal at $2f_0$. Although this matches the operation of a low-pass filter (LPF), it is noteworthy that frequency filtering in THz range

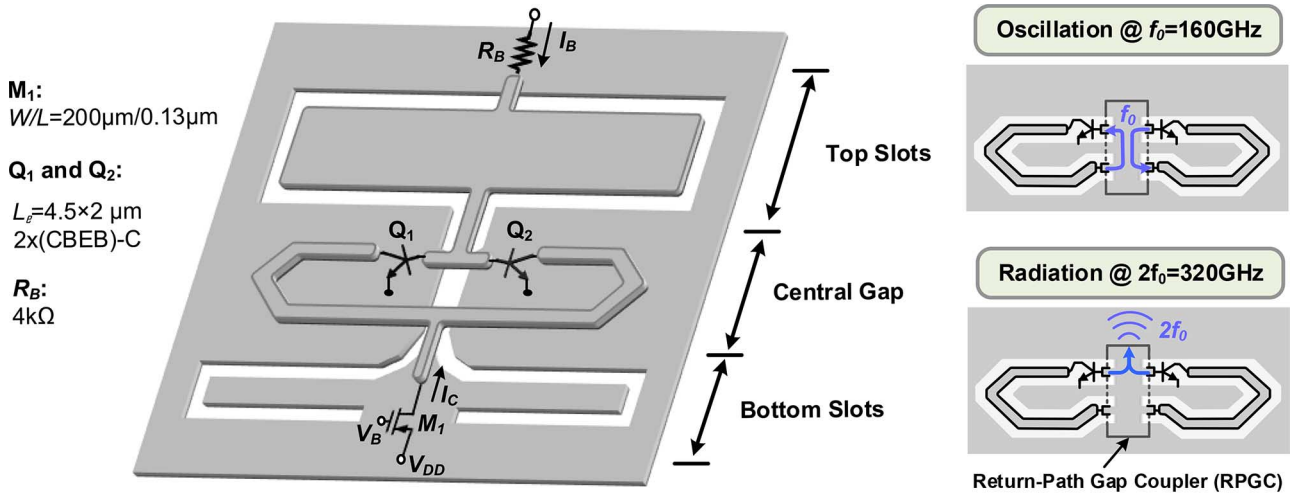


Fig. 5. Proposed THz radiator design: (a) the full schematic and the electromagnetic-wave structure, and (b) summarized operations for fundamental oscillation and 2nd-harmonic radiation. Please note that the structure is not drawn to scale.

is not only lossy, but also occupies large area [25], [26]. In addition, according to (1), the significant phase shift introduced by the LPF at f_0 may either reduce the oscillation frequency, or lead to a value of Z_0 that is too small to implement.

Instead of filtering the signals based on their *frequencies*, our proposed radiator design utilizes the orthogonality of different wave *modes*. By implementing a *return-path gap coupler* (RPGC) inside the self-feeding oscillator (Fig. 5(b)), the proposed radiator simultaneously achieves optimum fundamental oscillation, harmonic-signal generation and on-chip radiation. The structure of the radiator is shown in Fig. 5(a). The transmission lines connecting the transistors are based on the grounded coplanar waveguide (GCPW, the grounded side walls are not shown for the simplicity of the illustration). The signal trace uses the top copper layer (3 μm thick), and the bottom ground uses overlapped M1-to-M3 layers for better ground conductivity and DRC compliance. Next, to better describe the operations of the RPGC at f_0 and $2f_0$, the physical structure of the radiator is divided into three parts: top slots, central gap, and bottom slots (Fig. 5(a)).

By symmetry, the two transistors have both odd (out-of-phase) and even (in-phase) modes for the oscillation at f_0 (if oscillation can occur). For the odd-mode oscillation signal at f_0, the distributions of the electric field, forward current and return current are illustrated in Fig. 6[1]. When the differential signals generated from the HBT collectors meet after traveling along the GCPW lines, a virtual ground is formed at Node A. Meanwhile, the return currents of this signal pair, though encountering the gap in the ground plane, can continue traveling along the edges of the gap. Due to the differential phase, the return currents induce a transverse electric field inside the gap. The Poynting vector ($\vec{S} = \vec{E} \times \vec{H}$) of the TEM wave inside the gap carries the oscillation power towards the base side. At Node B of the base GCPW lines, once again a virtual ground is

[1]Please note that the directions of the solid blue arrows in Fig. 6 only illustrate the relative phase difference of the current, not the directions of the power flow. The power flow along the self-feeding lines and the RPGC is always from the collector to the base of the HBT.

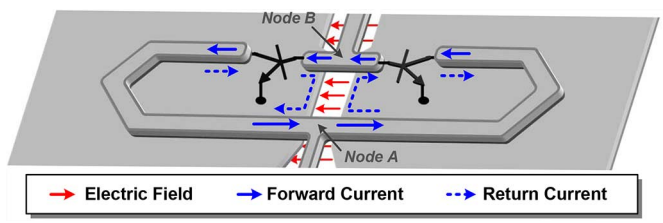


Fig. 6. The current and electric-field distribution for the odd-mode oscillation at f_0 in the central gap.

formed, where forward currents are induced by the incident return-current pair. This can be interpreted as the reverse process of what occurs at Node A, due to the reciprocity of the similar metal structures. Therefore, the RPGC supports the propagation of odd-mode signal, and the oscillation of the radiator at f_0 is similar to a normal self-feeding oscillator pair. Please note that the structure in Figs. 5 and 6 is not drawn to scale. The actual physical length of the return-path gap is only $\sim$ 17 μm, so that the extra phase delay added to the self-feeding path is minimized (but not negligible). More discussions on this issue will be given in Section II.C.

For the odd-mode operation, the role of the top and bottom slots is twofold:

- They confine the self-feeding traveling wave within the central gap of the RPGC. The length of the top slots of the RPGC is quarter wavelength at f_0 (shown in Fig. 7), which transforms the short termination at Node C (virtual ground in the odd mode) to open at the edges of the RPGC central gap ($Z_{f_0.\mathrm{top}} \to \infty$).
- The impedances that the top and bottom slots of the RPGC present to the central gap are in shunt with the base-emitter junctions of the HBTs:

$$Y_1 = \left(\frac{Z_{f_0.\mathrm{top}} // Z_{f_0.\mathrm{bottom}}}{2} \right)^{-1}, \qquad (2)$$

where Y_1 is the reactive termination needed in the self-feeding oscillator (Fig. 3). The bottom folded slots are

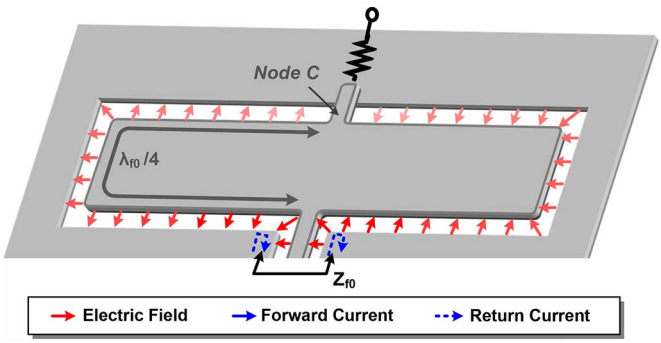


Fig. 7. The standing-wave distribution for the odd-mode oscillation at f_0 in the top slots.

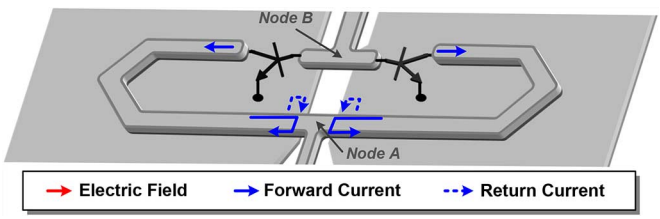


Fig. 8. The current and electric-field distribution for the even-mode oscillation at f_0 in the central gap.

slightly shorter than quarter wavelength in order to provide a weak inductance required by the calculated Y_1[2].

Overall, the four standing waves in the top and bottom slots of the RPGC block the leakage of the return-path currents traveling in the central metal gap. It is also noteworthy that these slots are folded into the transverse direction, because this way the standing wave inside each folded half section is out-of-phase with the neighboring standing waves. This is critical to the elimination of the radiation from these standing waves, which causes loss to the oscillation signals at f_0.

As mentioned previously, there is also an even (in-phase) oscillation mode of the HBTs. However, this undesired mode is not supported by the return-path gap. Shown in Fig. 8, when the even-mode signals meet at Node A, which presents an open, they are reflected back. Meanwhile, the even-mode return currents also cannot propagate along the edges of the return-path gap. In fact, such balanced wave is related to the TM mode of the metal gap. And, for such two-conductor waveguide, the cutoff frequency of the lowest TM mode is on the order of [23]:

$$f_{c,\mathrm{TM}} \sim \frac{1}{2d\sqrt{\mu\epsilon}}, \tag{3}$$

where d is the distance between the two edges of the gap, and μ and ϵ are the permittivity and permeability of the dielectric inside and around the metal gap. In our design, the gap distance d is 12 μm and the relative dielectric constant is $\sim$ 4, which result in a cutoff frequency of $\sim$ 6 THz. Therefore, the even-mode signals at f_0 of 160 GHz are fully blocked by the return path gap. The feedback path is not formed and the even-mode oscillation does not occur.

[2]The calculations for the values of Y_1 and Y_2 in Fig. 3 are presented in [13]. In the proposed RPGC design, the value of Y_2 is intentionally designed to be near zero.

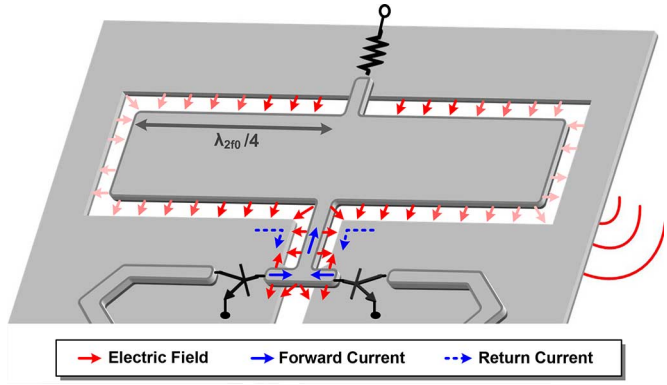


Fig. 9. The standing-wave distribution for the even-mode harmonic signal at $2f_0$ in the top slots.

Differential oscillation at f_0 leads to an even-mode 2nd-harmonic generation at the base junctions of the HBT pair. Therefore, the signal at $2f_0$ is also blocked by the RPGC. The full isolation between the base and collector of the HBTs increases the harmonic generation efficiency. On the other hand, as shown in Fig. 5(a), the common edge of the two top slots is connected to the bases of the HBTs, and the signal at $2f_0$ then creates standing-wave patterns as shown in Fig. 9. Note that the length of each slot at f_0 is quarter wavelength (Fig. 7). That means at $2f_0$, the length of each folded *half* slot is quarter wavelength. With such dimension, the top slots behave as a folded slot antenna [27], in which the four standing waves inside the half-slot sections are in-phase and efficiently radiate the 2nd-harmonic signal into the silicon substrate (and eventually coupled into the free space, as is shown in Section IV).

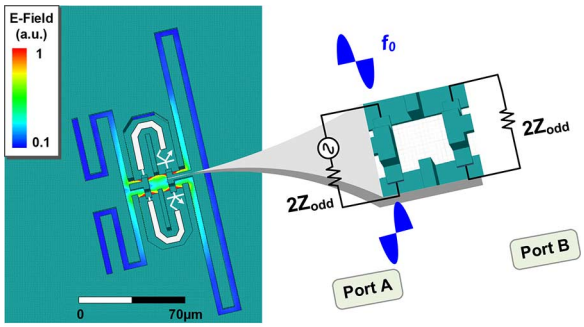
Lastly, it can be seen from Fig. 5(a) that the DC biases of the base and the collector of the transistors are naturally separated in the proposed RPGC-based radiator. Such separation, achieved without using any lossy AC coupling capacitor, is particularly important for SiGe HBTs due to the significant difference between the base and collector biases ($V_B \approx 0.8$ V, $V_C \approx 1.6$ V).

C. Simulation Results

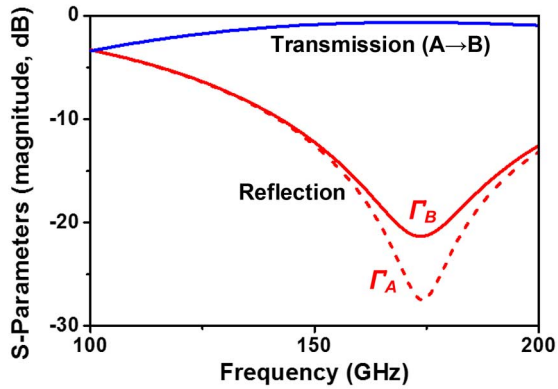
The operations described above are verified by the full-wave electromagnetic simulations using HFSS [28]. First, the return-path gap structure is stimulated by a differential (odd-mode) signal. The two-port simulation set up is shown in Fig. 10(a)[3]. Fig. 10(a) also presents the intensity distribution of the electric field inside the slots of the structure at the fundamental oscillation frequency of 160 GHz. It can be seen that the odd-mode signal is able to propagate along the return-path gap, and transfer from the differential Port 1 to Port 2. Meanwhile, standing waves are formed inside the four folded RF-choke slots. The results of the S-parameter simulation are plotted in Fig. 10(b). At 160 GHz, the insertion loss (S_{21}) of the structure is only 0.6 dB, which proves that the return-path gap is transparent to the differential oscillation signal.

Although the RPGC inserted in series with the transmission lines of the self-feeding oscillator pair does not add much loss, the induced phase shift cannot be ignored. This means the values

[3]The self-feeding lines and the two transistors (in white) in Figs. 10(a) and 12(a) are only for the purpose of illustration. They are not included in the actual EM simulation structure.

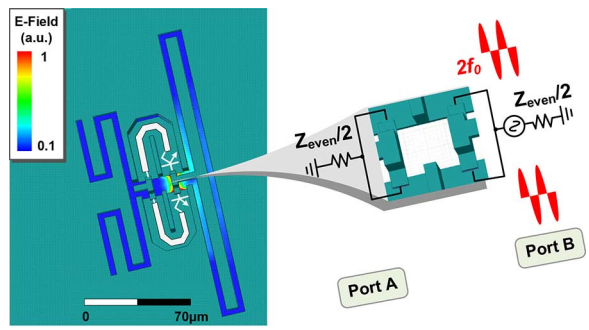


(a)



(b)

Fig. 10. Full-wave electromagnetic simulation of the THz radiator: (a) odd-mode excitation/loading ports and the intensity distribution of the electric field (b) S-parameters near the fundamental oscillation frequency of 160 GHz.



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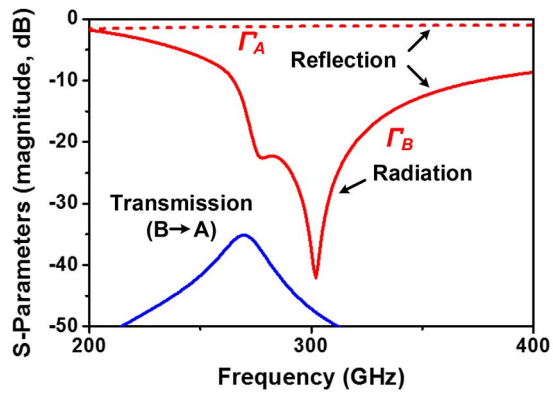

(b)

Fig. 12. Full-wave electromagnetic simulation of the THz radiator: (a) even-mode excitation/loading ports and the intensity distribution of the electric field (b) S-parameters near the 2nd-harmonic frequency of 320 GHz.

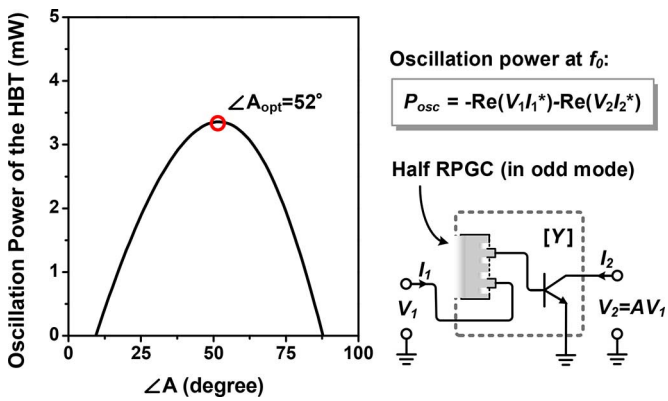

Fig. 11. The two-port active network including a SiGe HBT and a series half-RPGC structure at the transistor base. Also shown is the simulated optimum phase of the complex voltage gain of such active network at 160 GHz.

of Z_0 and φ_{TL} in (1) are not only determined by the parameters of the HBT itself, but also by the RPGC. It is noteworthy that (1) is actually applicable to any two-port active network. Therefore, the HBT and one half of the RPGC (in odd-mode operation) can be considered to be a new equivalent "transistor" (Fig. 11). By simulating the Y-parameters of such combined network, we see that the optimum phase of the voltage gain is 52° (or −308°). The associated peak oscillation power is 3.4 mW. Based on these and (1), the self-feeding line in the final design has a characteristic impedance Z_0 of 55 Ω and an electrical length φ_{TL} of 35° at 160 GHz.

For the even-mode operation, the simulation setup is presented in Fig. 12(a). The stimulus from Port B represents the in-phase 2nd-harmonic signal generated at the two bases of the SiGe HBTs. At 320 GHz, the intensity distribution of the electric field inside the slots is shown in Fig. 12(a), too. It is evident that the injected signal is fully blocked by the return-path gap. Meanwhile, four standing waves inside the folded slots on the right are formed. As indicated in Fig. 12(b), the simulated isolation between the two sides of the return-path gap is better than −30 dB, meaning that the structure is opaque to the even-mode signal. Please also note that the small reflection coefficient at Port B (Γ_B) means that the 2nd-harmonic signal is fully absorbed by the structure. In fact, the signal is turned into a downward-propagating radiation wave inside the silicon; and the simulated radiation pattern is shown in Fig. 13. The directivity in the perpendicular direction is 5.6 dBi. To reduce the excitation of the substrate wave inside the silicon (250-μm thick), a backside hemispheric silicon lens is assumed in the simulation (modeled as a semi-infinite silicon boundary condition beneath the chip substrate) [29]. The simulated radiation efficiency, including $\sim$ 30% power reflection at the silicon-to-air interface [13], is $\sim$ 50%. The additional loss is due to the finite substrate resistivity ($\sim$ 10 Ω·cm). The simulated output power of each radiator is $\sim$ 0.28 mW.

Lastly, according to Figs. 10(b) and 12(b), the orthogonal behaviors of the proposed structure for odd and even mode signals have a very broad bandwidth. This increases the robustness of the design with the presence of the process-voltage-temperature

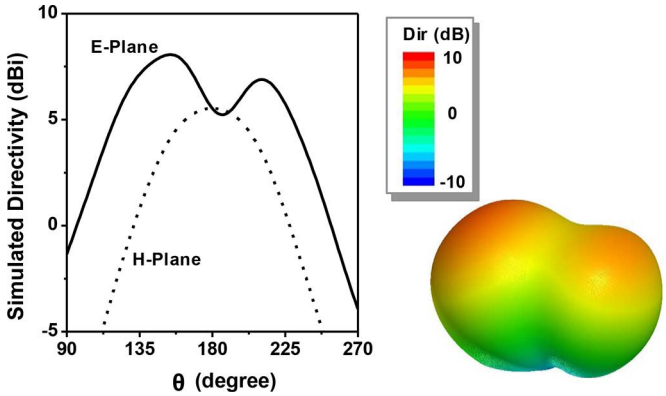

Fig. 13. The simulated radiation pattern of the proposed 320 GHz radiator unit. A backside hemispheric silicon lens is assumed.

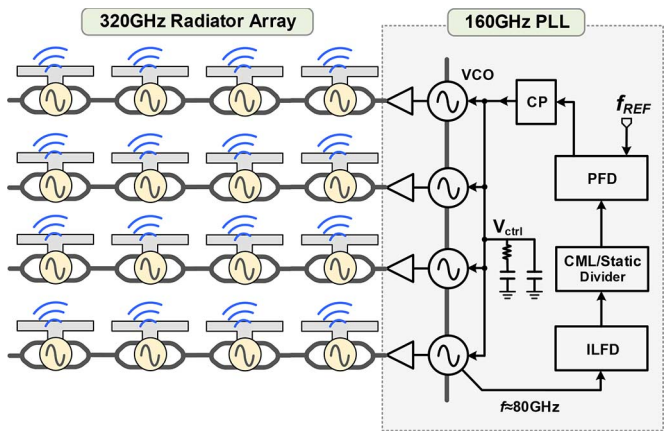

Fig. 14. The architecture of the 320 GHz transmitter with a fully-integrated phase-locking loop (CP: charge pump, PFD: phase/frequency detector, CML: current-mode logic, and ILFD: injection-locking frequency divider).

(PVT) variations, and makes it suitable for future implementations of wide-tuning source and broadband data transmitter.

III. Design of a 320 GHz Transmitter

The proposed RPGC-based THz radiator is integrated into a 4×4 array of a 320 GHz transmitter for heterodyne imaging system (shown in Fig. 14). Compared to the incoherent fully-intensity-based detection (e.g., [8], [9]) where the incident THz wave undergoes a self-mixing, in a heterodyne receiver (not implemented in this work) it is mixed with an LO signal with much larger power. The output response, as well as the imaging sensitivity, are therefore greatly enhanced [30]. A heterodyne multi-pixel system also enables electronic beam scanning, because each receiver pixel preserves the phase of the incident THz wave, and the signal phase shifting/combining can be then performed in the digital domain. This could potentially eliminate the needs for the mechanical scanning in conventional THz imaging systems. To perform heterodyne detection in such an imaging system, it is critical to lock the phase of the RF signal in the transmitter and the LO signal in the receiver. To achieve this goal, in Fig. 14, the 16-element radiator array is phase-locked by a fully-integrated PLL through injection locking at 160 GHz. Next, design details of some critical transmitter elements are given.

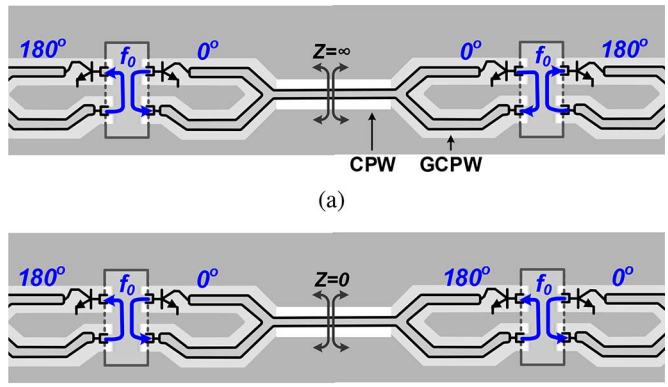

Fig. 15. The mutual coupling between adjacent radiators: (a) in-phase coupling mode (supported) and (b) out-of-phase coupling mode (unsupported).

A. Coupled Radiator Array

Although the proposed return-path gap structure in Section II.B optimizes the generation of THz radiation, the absolute power level from a single radiator is still limited by the HBT size. Therefore, a 16-element array is implemented for increasing the total radiated power. The power combining is obtained through the constructive superposition of the radiated waves in the far field. Such quasi-optical power combining [31]is efficient, broadband, and highly scalable. The array is partitioned into four rows, inside which elements are passively coupled. The mutual coupling between radiators is through a CPW transmission line tapping on the self-feeding lines of the radiators (shown in Fig. 15). By symmetry, there are in-phase and out-of-phase coupling modes in the steady state[4]. In the in-phase coupling mode (Fig. 15(a)), the boundary between two units is equivalent to an open termination, hence the added CPW lines behave as shunted capacitors. To minimize the impact of such capacitors, the signal path of the CPW lines is designed to be very narrow ($W = 3$ μm) and far from the ground plane ($D = 6$ μm). On the other hand, the out-of-phase mode (Fig. 15(b)) leads to a virtual ground at the connector of the coupling lines. It presents a highly inductive susceptance in shunt with the self-feeding lines, which greatly reduces the oscillation power. This undesired mode is therefore automatically suppressed. It is noteworthy that the above analyses assume that all radiator units are identical. According to the Adler's equation [32], if their free-running oscillation frequencies are different, a phase shift between the adjacent units occurs with the injection locking. Nevertheless, such undesired phase shift is not significant in our design, because of the small mismatch of the free-running oscillation frequencies (verified by the measurement shown in Fig. 20) and the strong coupling strength.

Due to the compactness of the proposed radiator, the entire 16-element array, equipped with functions of fundamental oscillation, harmonic generation, and radiation, only occupies an area of 0.9×0.9 mm^2. As a result, the achieved radiator density is $\sim$ 4X higher than the prior arts [12], [16], [24]. The small

[4] Any coupling phase between 0° and 180° leads to net power flow between units, and is therefore unstable. The mutual dragging and pulling eventually converges back to either in-phase or out-of-phase modes.

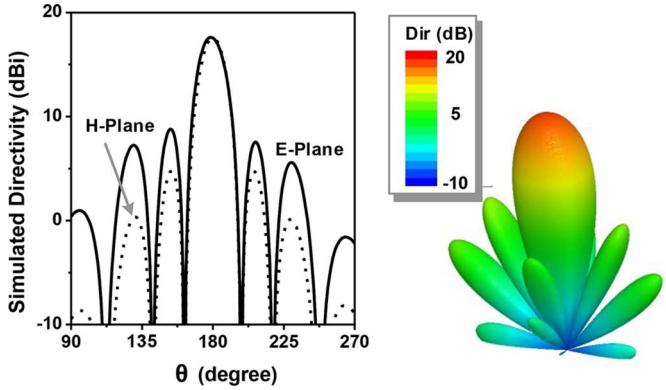

Fig. 16. The simulated radiation pattern of the 320 GHz 4×4 radiator array. The pitch between the elements is 220 μm, and a backside hemispheric silicon lens is assumed.

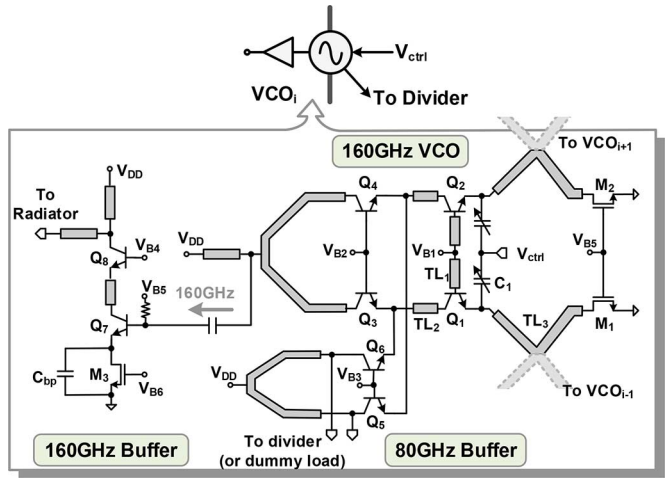

Fig. 17. The schematic of the 160 GHz VCO inside the on-chip phase-locked loop.

radiator pitch also suppresses the side lobes of the combined beam. The simulated radiation pattern of the array, with a directivity of 17.6 dBi, is shown in Fig. 16. This again assumes that a hemispheric silicon lens is attached on the back side. The simulated directivity without the lens is $\sim$ 12 dBi.

B. On-Chip Phase-Locked Loop

Shown in Fig. 14, the on-chip PLL consists of four coupled 80 GHz VCOs, providing their 2nd-harmonic (160 GHz) signal to synchronize each radiator row via injection locking. A divider chain samples the phase/frequency of the VCO linear array and then a global phase/frequency control signal V_{ctrl} is provided through a phase detector cascaded by a charge pump. Fig. 17 presents the schematic of the VCO, including two output buffers at 80 GHz and 160 GHz. In principle, heterodyne imaging uses a single-tone wave, and does not require frequency tunability. However, in practice, this is still needed to cover the process variability between the transmitter and receiver. In conventional cross-coupled VCO, the large, untunable C_π is in parallel with the varactor. So, in order to increase the tunability, the size of the lossy varactor should also be large, which is detrimental to the oscillation power. To obtain a better tradeoff between the oscillation power and tuning range, our 80 GHz VCO is based on a differential Colpitts oscillator topology, in which the resonance tank on one side of the VCO is mainly formed by the transmission line stub TL_1, MOS varactor C_1, and the C_π of the HBT transistor Q_1. Compared to the cross-coupled topology, the varactor C_1 is in series with C_π; so, for the same HBT size and tuning range ($\sim$ 6 GHz in simulation), we can use a smaller varactor and increase the oscillation swing.

The 80 GHz VCO has two common-base cascode stages in parallel ($Q_3 \sim Q_6$). Q_3 and Q_4 provide low-impedance terminations to the collectors of Q_1 and Q_2, which is required by the three-point nature of Colpitts oscillators [33]. Meanwhile, Q_3 and Q_4 also increase the generation of the 2nd-harmonic signal at 160 GHz, which is then further amplified by a cascode buffer stage Q_7 and Q_8. The signal is then injected into the radiator array through the CPW coupling line of the rightmost radiator. For the VCO at the bottom row in Fig. 14, Q_5 and Q_6 are used as a differential buffer to provide the 80 GHz output to the divider chain inside the PLL. The transmission line TL_2 is for tuning out the capacitance presented by the emitters of $Q_3 \sim Q_6$. Lastly, three 130 nm MOSFETs $M_1 \sim M_3$ are used to regulate the HBT currents. These MOSFETs have big size, and TL_3 at the emitter of Q_1 is used to transform the large drain capacitance of M_1 into a weakly inductive impedance, so that the tuning range and oscillation power of the VCO are not reduced.

The adjacent VCOs are strongly coupled through a direct connection of the intermediate nodes of TL_3 (Fig. 17). Similar to the radiator coupling described in Section III.A, the VCOs are coupled with in-phase mode, and the coupling junction at TL_3 presents open, hence has no impact in the steady state to the VCOs. Since each VCO is coupled to its neighbors, and the only global signal is the low-frequency varactor bias control V_{ctrl}, this proposed PLL architecture is highly scalable, and can accommodate even bigger radiator size for higher output power.

As Fig. 14 shows, the frequency divider chain of the PLL consists of injection-locking dividers (80 GHz to 10 GHz), CML dividers (10 GHz to 1.25 GHz) and a static divider, with a total division ratio of 256. The loop bandwidth is $\sim$ 2 MHz. The phase of the radiated wave at 320 GHz is then locked to an externally applied reference clock at $\sim$ 310 MHz.

IV. Prototype and Experimental Results

The proposed 320 GHz transmitter is implemented using the STMicroelectronics 130-nm SiGe:C BiCMOS process. The micrographs of the chip, as well as a radiator unit, are shown in Fig. 18(a). The entire chip, including the 4×4 radiator array and the PLL, occupies an area of 1.6×1.3 mm^2. The packaging is shown in Fig. 18(b). First, the chip is mounted onto a high-resistivity silicon wafer ($\sim$ 0.3 mm thick and $\sim$ 1 cm^2 large). The wafer is then glued to a PCB with a hole, so that the exposed front side of the chip is wire-bonded to the metal leads on the PCB for the connections of DC power, bias, and the PLL reference clock signal. Finally, a hemispheric, high-resistivity silicon lens (with a diameter of 1 cm) is attached on the other side of the wafer. Compared to the package in [13], the insertion of the high-resistivity wafer between the chip and the lens allows for

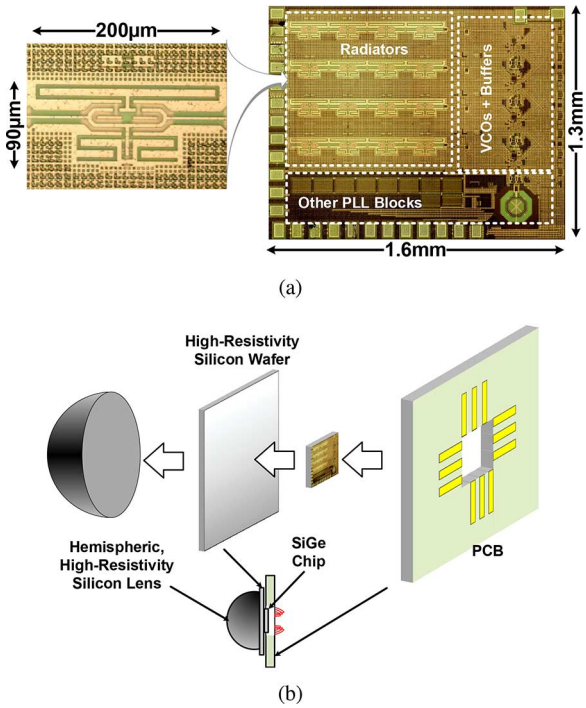

Fig. 18. (a) The microphotograph of the 320 GHz transmitter using 130-nm SiGe BiCMOS process. The THz radiator based on the return-path gap coupler is also shown. (b) The chip packaging with the backside attachment of a silicon lens.

easier alignment. Although the radiator is not located exactly at the spherical center of the lens, the beam collimation due to such offset is still not significant for two reasons: (1) the offset is much smaller than the lens diameter (0.5 mm versus 1 cm). (2) The beam is concentrated in the perpendicular direction, for which the refraction (at the lens surface) due to the offset is minimal [13].

The measurement setup is shown in Fig. 19. The output THz beam of the chip is received by a diagonal horn antenna. For testing the frequency and spectrum of the radiation, a VDI WR-3.4 even-harmonic mixer (EHM) is used to mix the input THz signal with the 16th harmonic of an externally-applied LO signal ($\sim$ 20 GHz). The measured spectrum of the down converted IF output is shown in Fig. 20. When the on-chip PLL is turned off, the radiator rows are not synchronized and oscillate at their own free running oscillation frequencies. This is indicated in the multiple spurs in Fig. 20(a). The number of spurs does not equal to the number of the radiator rows $(N=4)$; this may be due to the mutual pulling between the adjacent rows through the silicon substrate [34]. When the on-chip PLL is turned on, a single, coherent radiation is measured, as shown in the spectrum in Fig. 20(b). Due to the constructive power combining, the output power is 7-dB higher than the radiation measured in the former case. Such locking works over a small frequency range (0.2 GHz) due to the large oscillation power of the THz radiator array compared to the relatively small injection strength from the 160 GHz PLL [34]. The measured phase noise of the radiation is -79 dBc/Hz at 1 MHz offset.

Next, to measure the absolute power of the radiation, an Erikson power meter (with a WR-10 input) is used, which provides enhanced accuracy compared to the power measurements using highly nonlinear and lossy harmonic mixers [22], [35], [36]. Shown in Fig. 19, an additional $1''$ WR-10 waveguide is used to protect the metal flange of the sensor head, and another $1''$ WR-10 to WR-3.4 taper is used to connect to the horn antenna with a smooth transition. The total loss of such additional connection is 0.7 dB. To begin with, the distance between our transmitter and the horn antenna, d, is changed from 4 cm to 9 cm. The associated power received by the horn antenna, P_r, is plotted in Fig. 21. It can be seen that when the distance is larger than 6 cm, the roll-off of the received power complies with the Friis transmission equation ($P_r \propto d^{-2}$ [37]). Because of this, all the subsequent measurements are based on the far-field distance limit of 6 cm. With this distance, the received power is 61 μW, resulting in a transmitter effective isotropic radiated power (EIRP) of 22.5 dBm.

Using the harmonic mixer, the radiation pattern of the transmitter is measured by rotating the chip in both azimuth φ and elevation θ directions (Fig. 19). When the silicon lens is attached on the back side of the chip, the radiation pattern is shown in Fig. 22(a). The measured directivity is 17.3 dBi and the 3 dB beamwidth is $\sim 20^\circ$. Such high directivity is due to the coherent 16-element array configuration, and is consistent with the simulation presented in Section III. In addition, the radiation performance without the backside silicon lens is also characterized. It is expected that the output beam will undergo more divergence at the silicon-to-air interface, due to the more significant refraction near the critical angle ($\theta_c = 16^\circ$ [13]). Nevertheless, the measured pattern shown in Fig. 22(b) still has a high directivity of 13 dBi, with an associated 3-dB beamwidth of $\sim 54^\circ$ (H-plane) and $\sim 26^\circ$ (E-plane). The asymmetric profile is due to the different reflection rates for s-polarized wave and p-polarized wave [17].

Finally, the supply voltage of the transmitter, V_{DD}, is swept. The associated total radiated power, DC power consumption, as well as the DC to THz radiation efficiency, are plotted in Fig. 23. Here, the total radiated power of the chip equals to the measured EIRP subtracted by the measured directivity. At the V_{DD} of 2.15 V, the total radiated power reaches its maximum of 5.2 dBm (3.3 mW), and the associated DC power is 610 mW. This leads to a DC to THz radiation efficiency of 0.54%. It is noteworthy that even when the backside silicon lens is removed, the measured total radiated power and the DC to THz radiation efficiency are still as high as 0.9 dBm (1.2 mW) and 0.2%, respectively. The relatively small degradation indicates that when a highly directive beam (perpendicular to the silicon-air interface) is generated from a large-array configuration, the undesired impact of the substrate-mode wave is less significant.

V. Conclusion

In Table I, the performance of the proposed transmitter is summarized and compared with the other state-of-the-art THz radiators in silicon. It can be seen that this work achieves the highest radiated power and DC to THz radiation efficiency. These two metrics (when no silicon lens is used) are also the highest among the sources without silicon lens or non-standard wafer thinning. These clearly demonstrate that the proposed compact radiator design based on the return-path gap coupler has fully optimized the THz generation potential of the silicon

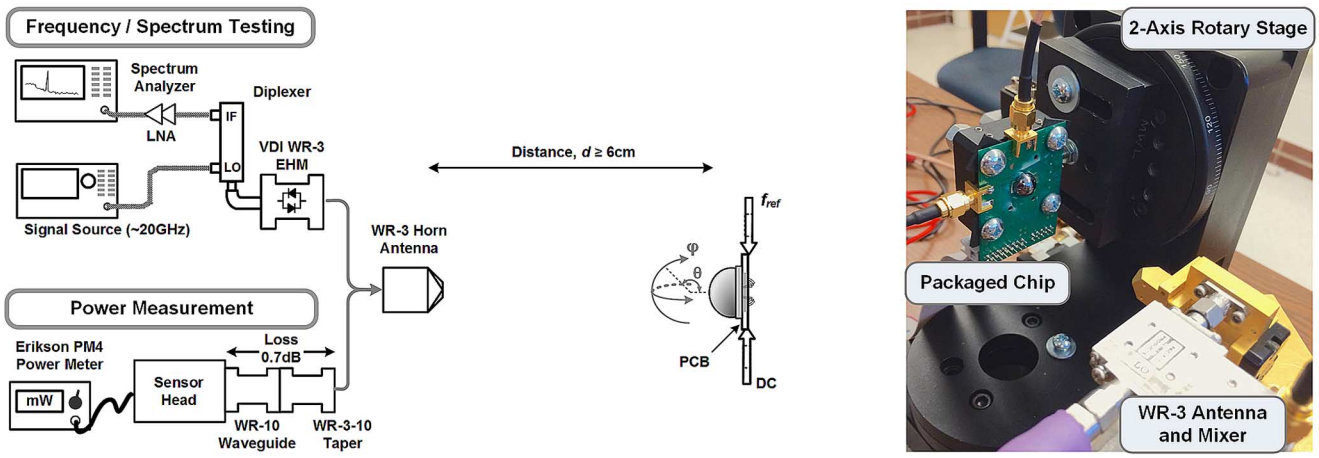

Fig. 19. The measurement setup for the 320 GHz transmitter and a photo of the packaged chip.

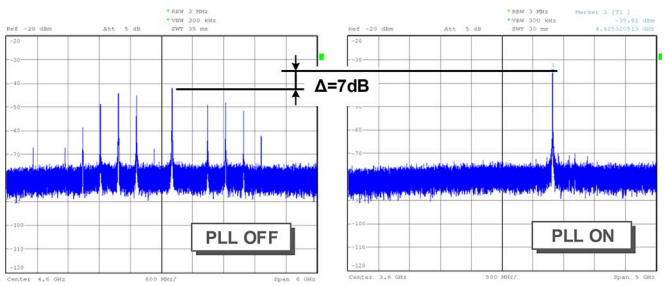

Fig. 20. The measured down-converted spectrum of the transmitter radiation: (a) on-chip PLL is OFF and (b) on-chip PLL is ON.

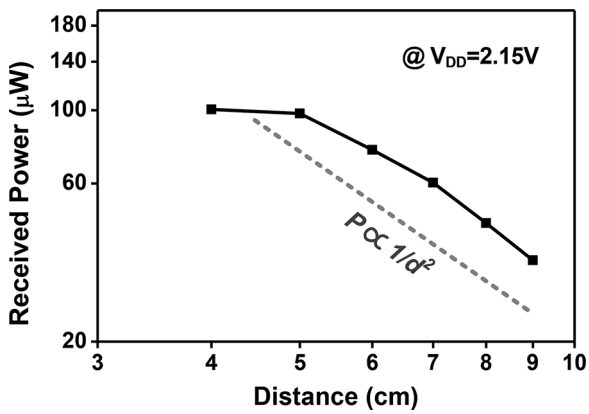

Fig. 21. The received radiated power of the power meter at varying distance, *d*, from the 320 GHz transmitter chip.

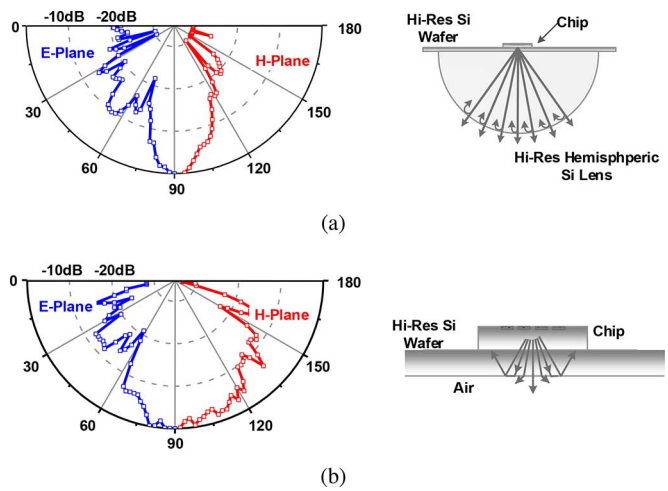

Fig. 22. The measured radiation patterns of the 320 GHz transmitter (a) with a hemispheric silicon lens attached at the back of the chip, (b) direct backside radiation without a silicon lens.

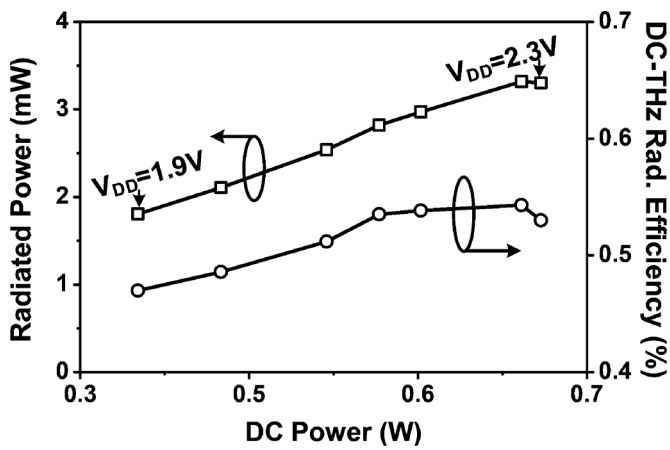

Fig. 23. The total radiated power of the 320 GHz transmitter, as well as the associated DC-to-THz radiation efficiency, at different DC power supply voltage and dissipation power.

transistors. Please note that the proposed device analysis approach and radiator design can also be applied to CMOS and other III-V integrated circuit technologies. It is noteworthy that the first THz on-chip PLL is presented in [19], but the output signal of the PLL is measured through wafer probing. To the best of our knowledge, our work is the first demonstration of fully-integrated phase locking for THz *radiation* sources, which is a critical step towards future THz sensing microsystems.

ACKNOWLEDGMENT

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TABLE I
PERFORMANCE COMPARISON OF TERAHERTZ SOURCES IN SILICON

References	Technology (f_{max})	Frequency (GHz)	Total Radiated Power (mW)	EIRP (dBm)	Phase Noise @ 1 MHz (dBc/Hz)	DC Power (W)	DC-to-THz Radiation Efficiency (%)	Area (mm^2)	Phase Locked?	Note
[11]	65-nm CMOS (190 GHz)	288	0.4	N/A	-87	0.28	0.14	0.29	No	Silicon Lens
[12]	65-nm CMOS (250 GHz)	338	0.8	17.1	-93	1.54	0.053	3.9		
[13]	65-nm CMOS (250 GHz)	260	1.1	15.7	-78	0.8	0.14	2.3		Silicon Lens
[15]	130-nm SiGe (500 GHz)	245	1.3	7	N/A	0.38	0.33	3.2		Extra Wafer Thinning
[16]	130-nm SiGe (500 GHz)	530	0.09 (Single Unit)	25	N/A	0.16	0.06	0.025		Silicon Lens
			1 (Incoherent Array)	N/A		2.5	0.04	4.2		
[24]	45-nm CMOS (190 GHz)	280	0.2	9.4	N/A	0.82	0.023	7.2		Extra Wafer Thinning
[19]	90-nm SiGe (315 GHz)	295	0.04 (Probed Power)	N/A	-82.5	0.38	N/A	2.6	Yes	Non-Radiating
This Work	130-nm SiGe (280 GHz)	317	1.2	13.9	-79	0.61	0.2	2.1		
			3.3	22.5			0.54			Silicon Lens

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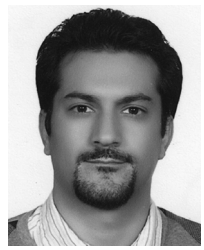

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