A CMOS Molecular Clock Probing 231.061-GHz Rotational Line of OCS with Sub-ppb Long-Term Stability and 66-mW DC Power

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Abstract

Recent progress of on-chip spectroscopic systems enables a new set of highly-stable frequency references (i.e. clocks) with low cost, power and volume. It is based on the rotational spectrum of gaseous molecules in sub-THz regime, a physical mechanism alternative to that in traditional atomic clocks. This scheme also enables fast start-up operation and robustness against mechanical vibration and external electromagnetic fields. This paper demonstrates the first chip-scale molecular clock in 65nm CMOS which probes the 231.061GHz spectral line of Carbonyl Sulfide ($^{16}O^{12}C^{32}S$). The clock consumes only 66mW DC power and has a measured Allan deviation of 3.8×10^{-10} with an averaging time of $\tau=10^3$s.

Introduction

Stable frequency references are critical for equipment used in navigation, communication and sensing. The widely adopted mechanical-resonance oscillators, such as crystal oscillator and MEMS oscillator, suffer from long-term frequency drifts due to external disturbances (vibration, temperature change, etc.) and aging. By optically probing the invariant electron transition of atoms, an atomic clock significantly improves the long-term stability. Chip-scale atomic clock (CSAC) further achieves clock miniaturization using coherent population trapping (CPT) [1, 2], but has exceedingly high cost and hence limited applications. Here, we show that sub-THz rotational spectral lines of gaseous molecules are a promising set of timebase for portable clocks. Compared to cesium (Cs) atomic clocks, our selected OCS molecular spectral line does not require the slow and power-consuming heaters for alkali evaporation, and is by nature less sensitive to external electromagnetic fields (e.g. Zeeman-shift coefficient is 98ppt/Gauss for OCS at 231.060983GHz and 150ppb/Gauss for Cs at 9.1926GHz). Thus, lower power, instantaneous start-up and better long-term stability are enabled. Its absolute linewidth 100~1000× larger than that in CSACs also leads to a high clock loop bandwidth of ~100 kHz, providing error corrections under rapid mechanical vibration. More importantly, this scheme, combined with recent progress in on-chip THz spectrometers [3], allows for clock implementation on low-cost silicon chips without any electro-optical assembly needed in atomic clocks. In this paper, we report the first molecular clock using a 65nm CMOS technology.

Architecture of Molecular Clock

The CMOS molecular clock is illustrated in Fig. 1. A rotational spectral line of OCS near f_0=231.060983GHz is chosen. The OCS gas with 5-Pascal pressure is held inside a WR4.3 waveguide gas cell, the length (L=140mm) of which is optimized for maximum spectroscopic signal-to-noise ratio (SNR) [4]. Fig. 1 also presents the measured spectral profile with a quality factor of $Q=2.6\times10^5$. The Tx probing signal ($f_C\approx$231.061GHz) is FSK-modulated (modulation frequency f_m=16kHz and frequency deviation Δf=1MHz) and detected by a square-law detector in Rx. The intensity of two sidebands of the FSK signal is shaped by the absorption line profile, and any frequency offset (f_C - f_0) leads to absorption imbalance and causes envelope fluctuation (at f_m) of the detector output. A feedback error voltage is then generated, which indicates the sign and magnitude of the frequency offset. After amplification and low-pass filtering, it is fed into a voltage-controlled crystal oscillator (VCXO) in the Tx to establish a dynamic frequency compensation for its 80-MHz output.

Probing Signal Generation and Detection on CMOS

Fig. 2 shows the Tx including a 224~242GHz fractional-N phase-locked loop (PLL). The sub-THz signal is extracted from a frequency quadrupler chain, which utilizes the nonlinearity of MOSFETs driven by a 57.8GHz harmonic oscillator. A 40-bit MASH 1-1-1 Δ-Σ modulator enables *ppt*–level frequency tuning resolution. The FSK modulation is performed by periodically changing the control word of the Δ-Σ modulator. The f_m and Δf of FSK are selectable with a resolution of 3-bit. Fig. 3 gives the schematic of the Rx. A NMOS transistor biased at sub-threshold is utilized as a square-law power detector. A low-noise folded-cascode op-amp further amplifies the baseband signal. Finally, the error signal is detected by an on-chip lock-in detector, which is referenced to f_m. To couple the probing signal from/into the chips, a pair of custom-designed chip-to-waveguide transitions using quartz probes is implemented. The loop filter is off-chip for post-fabrication adjustments of loop parameters.

Measurement Results

The measured loss of the gas cell is 7.3dB (Fig. 5 (left)). Fig. 5 (right) presents the output spectrum (no FSK) of the Tx at 231.061GHz. The output power including the loss of chip-to-waveguide transition (~10dB) is -20.2dBm (Fig. 6). This power level avoids spectral broadening due to saturation [4]. The measured phase noise is -68.4dBc/Hz with a frequency offset of 1MHz. The measured noise equivalent power (NEP) of the Rx, including the transition loss, is 501pW/Hz$^{0.5}$ at f_m=16kHz (Fig. 6). Fig. 7 shows the packaged CMOS molecular clock as well as the dispersion curve (V_{error} versus f_c-f_0) measured by the FSK signal (in an open loop) with a SNR of 53dB. The molecular clock is locked onto the zero-crossing point of the curve. Fig. 8 (left) presents the measured instantaneous frequencies of the closed-loop clock and the free-running VCXO over 4000s. The measured stability (quantified by Allan deviation [5]) reaches 2.4×10^{-9} for τ=1s and 3.8×10^{-10} for $\tau=10^3$s. The suppression factor of VCXO frequency drift is ~10× through the molecular-clock regulation, and is expected to be higher under large ambient-temperature change. Shown in Table I, the CMOS clock achieves high stability (comparable to that in [1]), faster response (thanks to the much larger absolute linewidth), start-up speed, and significantly simplified construction. Currently, the drift of our prototype is mainly due to the OCS gas leakage of the set up (0.1Pascal/hr), which can be improved with a hermetic package. This, along with improved chip-waveguide transition design with reduced

loss (i.e. ~10× higher *SNR*), will lead to a predicted stability below 10^{-11} (τ=10^3s) (Fig. 8). The chip consumes 66mW power and the waveguide gas cell has a volume of 5.6cm^3.

References

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[2] Microsemi. Quantum^{TM}, SA.54s chip scale atomic clock, 2017.
[3] C. Wang, et al., *JSSC*, pp. 3361-3372, Dec. 2017.
[4] C. H. Townes, Microwave spectroscopy, Courier Corp., 2013.
[5] W. Riley, Handbook of Freq. Stability Analysis, NIST, 2008.

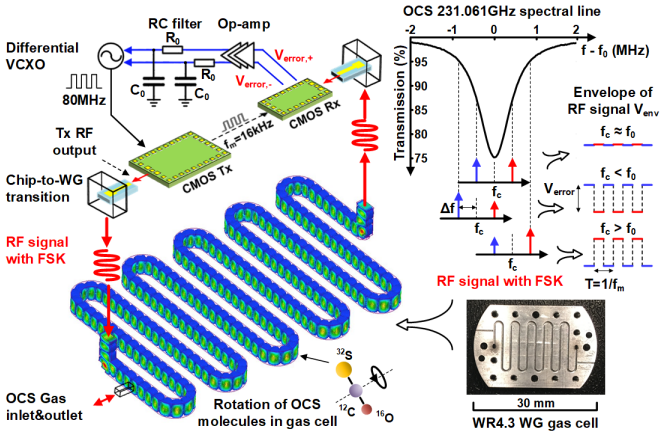

Fig. 1 System architecture of the molecular clock by probing the 231.061GHz OCS spectral line in a WR4.3 bended waveguide gas cell.

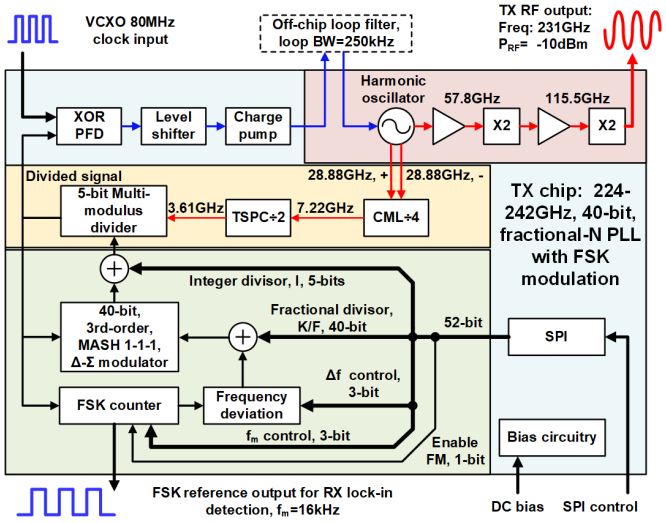

Fig. 2 Schematic of the clock Tx with a 40-bit fractional-N PLL.

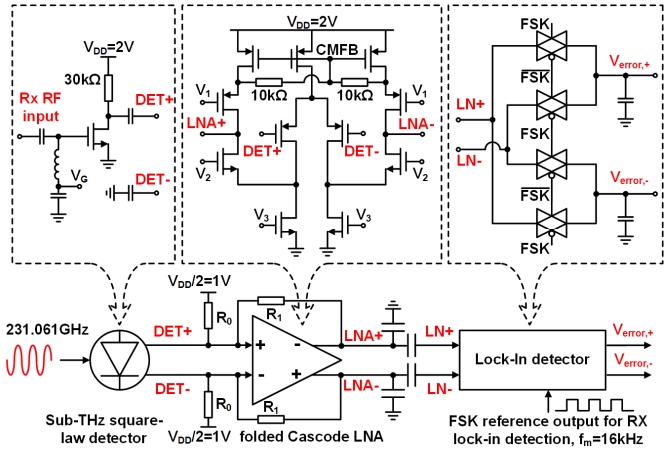

Fig. 3. Schematic of the clock Rx with THz and lock-in detectors.

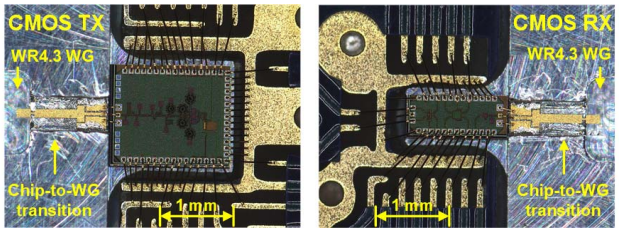

Fig. 4. Photograph of wire-bonded CMOS Tx and Rx chips.

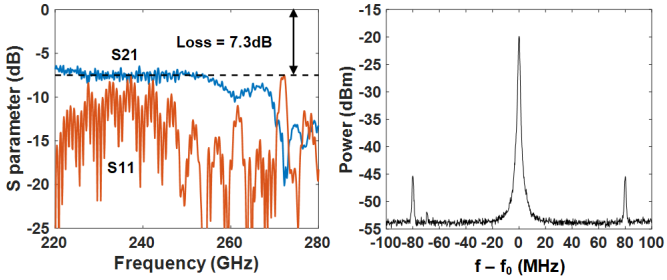

Fig. 5. The measured S-parameters of the waveguide gas cell (left) and the output spectrum of Tx at f_0=231.010GHz (no FSK) (right).

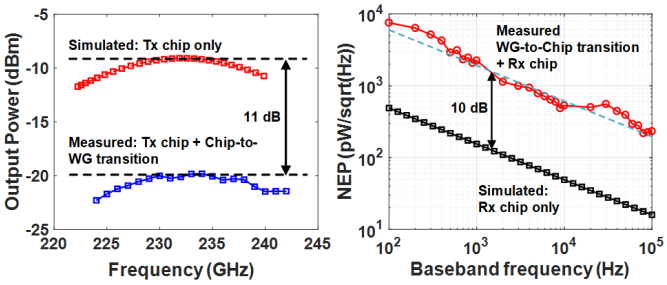

Fig. 6 The measured Tx output power at 224~242GHz (left) and the Rx noise equivalent power (NEP) at 231GHz (right).

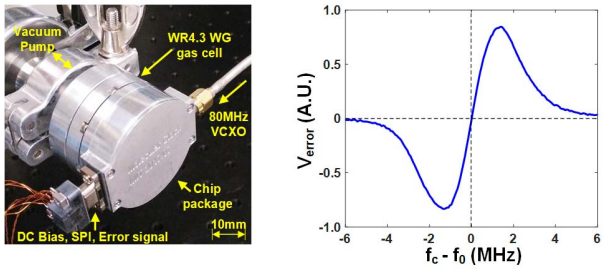

Fig.7 Photograph of the packaged CMOS molecular clock (left) and the dispersion curve of the spectral line obtained by the chip (right).

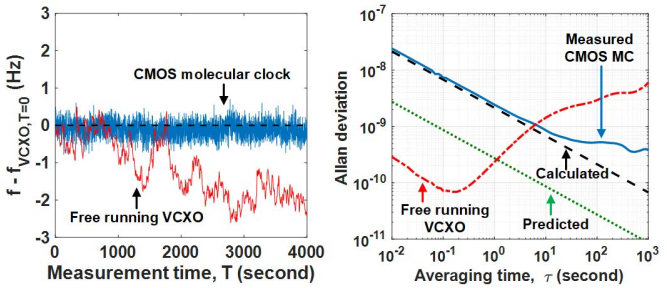

Fig.8 Measured instantaneous frequency w/ and w/o locking (left) and the measured Allan deviation (right) using a Keysight 53230A counter.

TABLE I PERFORMANCE COMPARSION

	Allan Deviation (10^3 s)	Linewidth (kHz)	$t_{turn-on}$ (second)	P_{DC} (mW)	Implementation
This Work	3.8×10^{-10}	880	<1	66 [1]	65nm CMOS
CSAC [1]	3×10^{-10}	~1	N/A	26 [2]	Electronics + Gas-Cell-Integrated Laser & Heater
CSAC [2]	1×10^{-11}	~1	180	120	

[1] The power of the VCXO is not included.
[2] The power of off-chip heater, laser, and other components is not included.