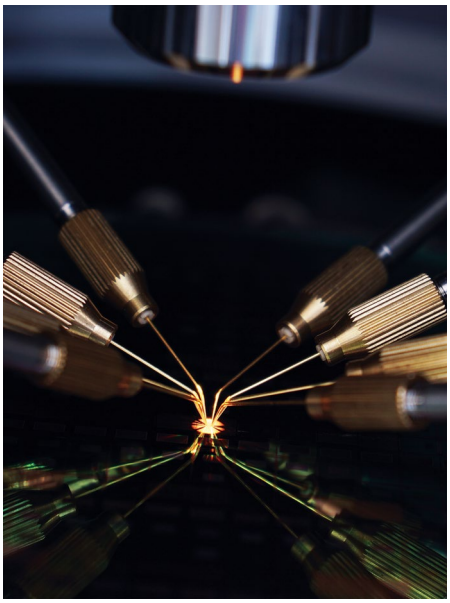
CMOS with a spin

Compatibility with established complementary metal–oxide–semiconductor (CMOS) processes could be a key factor in the success of an emerging device technology.

Computing hardware is approaching a crossroads. The scaling of traditional CMOS technology, which has sustained progress in the field for decades, is approaching its limits. At the same time, the demand for ever more powerful and energy-efficient computers — required, for example, to drive improvements in machine learning and adapt to the data-intensive needs of an expanded Internet of Things (IoT) — remains. Where exactly the field goes next to meet these challenges is uncertain, but there is no shortage of ideas.

One such idea is spintronics, which exploits the spin of electrons for data storage and processing. To start, the approach has already yielded magnetic random access memory (MRAM), a non-volatile memory capable of fast operation and high endurance. In these devices, data is stored in magnetic tunnel junctions. Initially, switching was achieved using a magnetic field, but it can now be done electrically using an effect known as spin-transfer torque (STT). The technology — STT-MRAM — has generated a range of industrial investments. Last year, for example, researchers from Samsung Electronics[1] and Intel[2,3] reported integrating STT-MRAM into their CMOS logic chip manufacturing processes, and last month Everspin Technologies announced[4] that it had begun pilot production of a 1-Gbit STT-MRAM product.

Looking further ahead, two-dimensional materials, as well as the designer stacks of two-dimensional materials known as van der Waals heterostructures, offer an intriguing platform for the development of beyond-CMOS spintronic devices. In a Review Article in this issue of *Nature Electronics*, Weisheng Zhao and colleagues explore the development of two-dimensional spintronics, examining, in particular, the potential of the approach to deliver devices and circuits for low-power data storage and processing. They also discuss the challenges that exist in creating practical systems, including the need for accurate theoretical device models, new device architectures, and batch fabrication methods.



Photograph of a ternary logic circuit, which is fabricated on 8-inch wafers using commercial silicon CMOS processes, surrounded by electrical probe needles. Credit: image courtesy of Jae Won Jeong, UNIST

Abandoning CMOS technology entirely is unlikely to be the first step for any emerging platform and thus integration with the established industrial process will be key. The power and potential of this approach is highlighted in research Articles elsewhere in this issue.

In the first Article, Ruonan Han, Dirk Englund and colleagues consider the CMOS integration of quantum sensors, and those based on nitrogen–vacancy centres (a point defect in diamond), in particular. Such sensing technology is typically bulky and made from discrete components. The integrated approach combines all the crucial ingredients for nitrogen–vacancy control and measurement in one monolithic chip, creating a platform that can be used for quantum magnetometry and thermometry.

In the second Article, Wei Lu and colleagues consider the integration of memristors with CMOS. Conventional computers have a von Neumann architecture in which memory and processing units are separated, and the need to transfer data between the units limits computing speed and wastes power. Memristors, which are resistive devices with memory, could be of value here as they can store and process information in the same physical location. They have already been used in a variety of relatively sophisticated machine learning and neuromorphic computing applications, and now by integrating a memristor crossbar array with CMOS control circuitry, Lu and colleagues have created a fully-functional, programmable neuromorphic computing chip.

As Mark Lee and colleagues highlight in another Article in this issue, CMOS compatibility is not just a problem for emerging memory and logic devices — it is also a concern for thermoelectric generators. These generators can turn waste heat into electrical energy, and the researchers create silicon-based devices fabricated on an industrial CMOS process line. As a result, the generators are compatible with integrated circuit technology, and could, in particular, be used to power IoT devices.

In pursuit of energy-efficient computing, such as that required by IoT devices, one approach is to move from a binary logic system to a ternary one. Here again compatibility with current technology is important. And in the final Article in this issue, Kyung Rok Kim and colleagues report an energy-efficient ternary logic technology that can be fabricated on the wafer scale with CMOS processes. ❐

Published online: 15 July 2019
https://doi.org/10.1038/s41928-019-0281-7

References
1. Song, Y. J. et al. *2018 IEEE Int. Electron Devices Meet.* https://doi.org/10.1109/IEDM.2018.8614635 (2018).
2. Golonzka, O. et al. *2018 IEEE Int. Electron Devices Meet.* https://doi.org/10.1109/IEDM.2018.8614620 (2018).
3. Raychowdhury, A. *Nat. Electron.* **1**, 618–619 (2018).
4. Everspin enters pilot production phase for the world's first 28 nm 1 Gb STT-MRAM component *Everspin Technologies* (11 June 2019); https://go.nature.com/2YyBn0x