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Filling the Gap With Sand

When CMOS reaches THz

Terahertz (THz) radiation ranging from 300 GHz to 10 THz [1] has attracted a growing number of researchers over the past decade. They are enthusiastic about its great potential for biomedical diagnoses, security screening, and high-speed communication. For instance, a THz wave can propagate through dry, nonmetallic, and nonpolar materials with small attenuation. This ability, combined with its small wavelength (versus microwave) and photon energy (versus X-ray), makes a THz wave an ideal option for nonionizing medical imaging, such as a burn injury assessment [2] or skin cancer diagnosis [3]. A short-range wireless link operating at such an unallocated band is also expected to significantly boost transmission speeds. In [4], a 25-Gb/s link with a 220-GHz carrier was demonstrated over a distance of 50 cm. A higher data rate of 100 Gb/s is anticipated in the near future [5].

So why did we not exploit this promising spectrum earlier? The main technical constraint is a THz gap. As Figure 1 shows, the THz frequency is too high for electronic devices, mainly due to the excessive loss and limited carrier velocity. In addition, it is too low for photonic devices because it lacks material with a sufficiently small bandgap [6]. As a result, although significant efforts are made in electronic (e.g., high-mobility materials) and optic (e.g., a quantum-cascade laser with cryogenic cooling) societies, the generated signal THz power still is much lower than other spectrums. A similar trend occurs in signal detection too, where such a gap isolates the two-decade spectrum from our spectrum-congested world.

This article presents some of our efforts from the electronic side. Instead of using expensive materials, we rely on silicon CMOS, a technology that is probably the most viable but often ignored, due to its speed and power-handling capability. CMOS

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is expected to drastically reduce the cost and size of current THz systems. Meanwhile, THz components can be built with other analog/digital signal-processing circuitry on the same die, which enables unprecedented levels of integration and flexibility. This can trigger tremendous opportunities for the portable medical device market, such as detecting tooth cavities in vivo [3] and analyzing breath to diagnose disease [7]. In the following sections, we first discuss the challenges in THz CMOS and then show how we fill the THz gap with silicon chips that originate from sand.

THz Design in CMOS: Challenges

Historically, circuit designers have always enjoyed the steadily faster devices brought by the downscaling of CMOS technology. One benefit was that conventional design topologies could often be extended to higher frequencies whenever a more advanced technology node was ready. For example, an oscillator (e.g., cross-coupled oscillator) working at the cellular band can be easily modified into a 60-GHz generator by shrinking the capacitor and inductor (and probably the transistor as well) inside the resonance tank, as long as the transistor is fast enough.

Unfortunately, as we approach the THz regime, such a benefit is very likely to be over for two reasons.

1) The fundamental operation frequency becomes so close to the cutoff frequency of the devices that the active power the device could provide is scarce. (Note that the cutoff frequency for transistors in THz design is often referred to the *maximum oscillation frequency*, f_{max}, which incorporates all of the device's loss mechanisms. In contrast with f_T, it is the fundamental boundary between device activity and passivity.) Such activity is further reduced by the increasing loss of the metal structure due to the more severe skin depth effect. This dilemma is worsened considering that the f_{max} of mainstream CMOS technologies has reached a plateau near 300 GHz in recent years (especially when the device's metal interconnects are included).
2) Because our target frequency is close to or above f_{max}, we have to rely on super-harmonic operations. Actually, the ubiquitous usage of device nonlinearity is probably the biggest distinction between THz electronic designs and their lower-frequency counterparts. While the nonlinear modeling and optimization of some two-terminal devices, such as the diode and MOS varactor, were relatively well studied in the past and in recent years [8], [9], those for three-terminal transistors are less explored [10]–[12]. This adds significant complexity to the design. Furthermore, harmonic operation inevitably leads to lower power efficiency [13]–[27].

Due to these technical challenges, conventional circuit topologies normally fail to facilitate effective THz power generation. We present several examples in the "Harmonic Oscillators" section, to illustrate this.

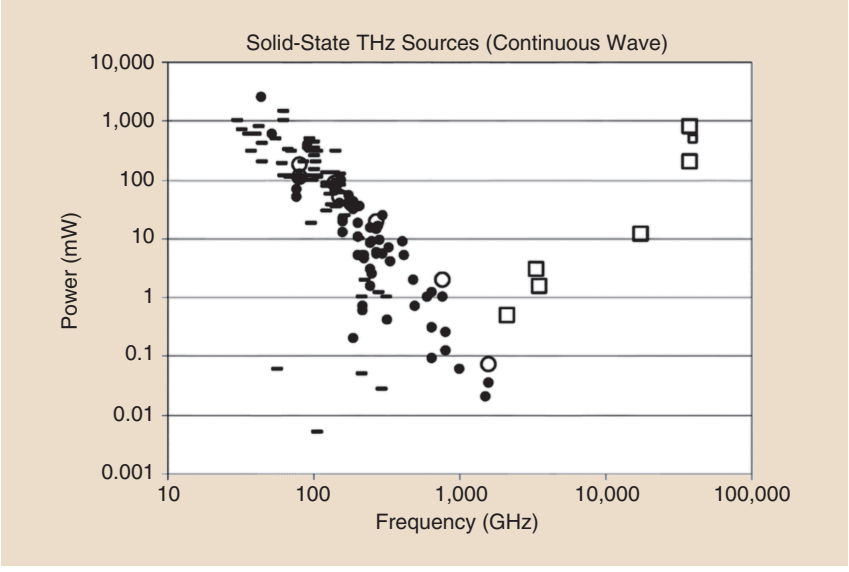

FIGURE 1: The THz gap with respect to source technology, including quantum cascade lasers (□), frequency multipliers (●), and other electronic devices (–). Hollow symbols represent cryogenic results [1].

High-Power THz Source: Circuit Works for Device

As circuit designers, we have realized that it is no longer valid to treat devices for existing circuits like LEGO bricks. Instead, to fully release their potential, new circuits should be synthesized for certain characteristics of existing devices. To be more specific, we first analyze the linear/nonlinear dynamics of a single device and find that the conditions must reach their fundamental performance limit. Then, we innovate microwave passive structures to generate wave patterns around the device to meet the derived conditions. Finally, the input and output signals, which normally are at different harmonics, are efficiently guided between the device and the external using wave features such as mode orthogonality. To illustrate such methodology, two examples, a harmonic oscillator and frequency multiplier, are presented in the "Harmonic Oscillators" and "Frequency Multiplier" sections, representing the most popular solutions to generate THz signals.

Harmonic Oscillators

For the most part, a harmonic oscillator is similar to a normal oscillator. The difference is that the output of the harmonic oscillator is the harmonic component of the oscillation signal distorted by the nonlinearity of the transistors. While the oscillation

is allowed to occur only below f_{max}, its harmonics may lie well within the THz region. A push–push second-harmonic oscillator (and its variants) is a typical topology based on such a principle. As shown in Figure 2, the two transistors oscillate in a differential pattern. The fundamental signal is therefore canceled at the output, and the second-harmonic signals are in phase and combined and extracted to the load.

Although a push–push oscillator was very popular in THz design [28]–[30], the output power was low, as explained in the following. In general, we need to optimize two processes to maximize the output power. First, at the fundamental frequency, the transistor should be configured so that the maximum power is generated to overcome the passive loss and sustain a large oscillation swing. Second, the nonlinearity of the device should be optimized to convert (part of) the fundamental power into higher harmonics. Regarding these, we find that two optimization conditions are required. Because they are derived from the analysis of a single device, they are independent of any circuit topology and hence are very general and fundamental.

The first condition is called *optimum voltage gain at fundamental oscillation frequency*, A_{opt} [31]. Note that such a gain is a complex value with both magnitude and phase. If we model the transistor using a two-port, Y-parameter network and derive the net radio-frequency (RF) power P_{out} coming out of the device, an optimum drain-to-gate voltage ratio (i.e., voltage gain) A_{opt} exists, which maximizes the power. (The net power is the sum of two parts: that generated from the drain and that dissipated by the gate.) In particular, we find that, close to f_{max}, the phase of the gain is significantly smaller than 180° (or more negative than –180°, considering the device delay).

We can better comprehend such a phenomenon from a device point of view, as shown in Figure 3 [32]. When a gate voltage is applied, the

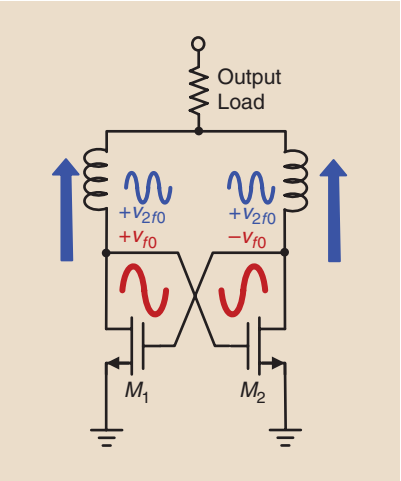

FIGURE 2: A standard push–push oscillator that generates a second-harmonic signal at the output.

drain current i_d is delayed due to the propagation along the gate R-L-C network and the finite carrier drift time. The drain current is further delayed by the feedforward path through the parasitic capacitance C_{gd}. To extract the maximum power from the drain, the drain voltage v_d should phase match i_d. Hence, an extra delay (or phase shift) of v_d is needed in addition to the conventional 180° inversion behavior. If we are off from such an optimal value, P_{out} rolls off quickly (Figure 3). This implies that any design that treats and forces the transistor to be a full-inverting device (i.e., $A = 180°$), as we did at a lower frequency, will lead to severe power degradation. Unfortunately, that is exactly what happens in the popular push–push oscillator. According to the simulation in Figure 3, the oscillation power, P_{out}, is only half the optimal.

The second condition deals with the optimum harmonic power generation efficiency [32]. This highly nonlinear problem is simplified into a harmonic feedback factor, β_{nf0}. Normally, harmonic oscillators are designed for only fundamental-frequency operation, with, at most, an output-matching network at the desired harmonic. However, an aspect that has been neglected is that, once the harmonic signal is generated from the transistor drain, it is partially sent back to the gate through the oscillator structure. Unfortunately, in most (if not all) previous THz designs, a negative feedback loop is unintentionally formed, greatly reducing the harmonic output power. Again, take the push–push oscillator as an example. As mentioned previously, the second-harmonic voltages on both sides are identical (Figure 2),

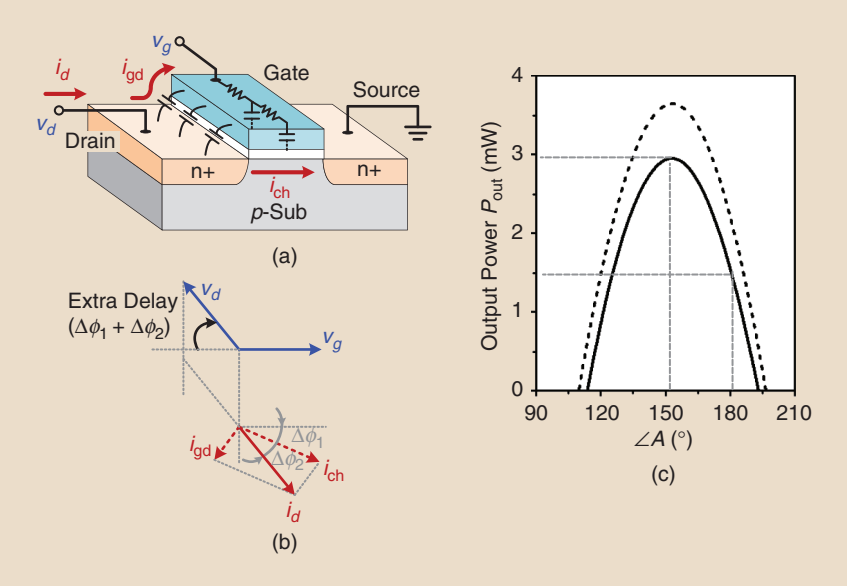

FIGURE 3: (a)–(b) The phase delays of various voltage and current components inside a transistor that lead to the optimum complex voltage gain condition. (c) The calculated (dashed line) and simulated (solid line) net output power at 130 GHz of a 65-nm NMOS transistor (f_{max} = 200 GHz) with varying phases of the gain [32].

which leads to a unity harmonic feedback factor ($\beta_{2f_0} = 1$). The harmonic voltage presented at the gate induces an extra harmonic current that is almost out of phase with the original one generated through f_0–$2f_0$ nonlinear conversion (which is supposed to be fully extracted to output). That is another reason for the low output power of push–push oscillators. Shown in Figure 4, the harmonic output power at 300 GHz is four times smaller than the optimal, which is associated with near-zero feedback (i.e., full drain-to-gate harmonic isolation).

To achieve the first optimum gain condition, in [31] a triple-push structure in 65-nm CMOS is used to match the optimum phase of near 120° at 160 GHz. The measured third-harmonic power at 480 GHz (160 μW) is approximately 8,000 times higher than its silicon predecessors were before 2010 [28], [29]. In another work [33], the optimum phase of the gain is achieved using a lower fundamental frequency (where $\angle A_{opt}$ is close to 180°) and higher harmonic order (fourth). The measured power at 290 GHz is 0.76 mW.

To simultaneously achieve the optimum gain and harmonic isolation for even higher output power, a self-feeding oscillator topology utilizing wave synthesis is proposed [34]. The basic schematic of such an oscillator is shown in Figure 5, where a transmission line (TL) supporting traveling wave is used as the transistor's oscillation feedback path. In addition, the boundaries on two sides of the TL are engineered through Y_G and Y_D to create proper reflections (hence, standing wave). It is shown that both optimum conditions can be obtained by controlling the patterns and relationship of the traveling and standing waves inside the TL [32]. For the optimum gain A_{opt} at fundamental frequency, such a wave can be synthesized when the design parameters in Figure 5 comply with the relationship

$$\frac{1}{Z_0 \sin \varphi_{TL}} = \frac{g_{11} + \mathrm{Re}(A_{opt} \cdot y_{12})}{\mathrm{Im}(A_{opt})}, \quad (1)$$

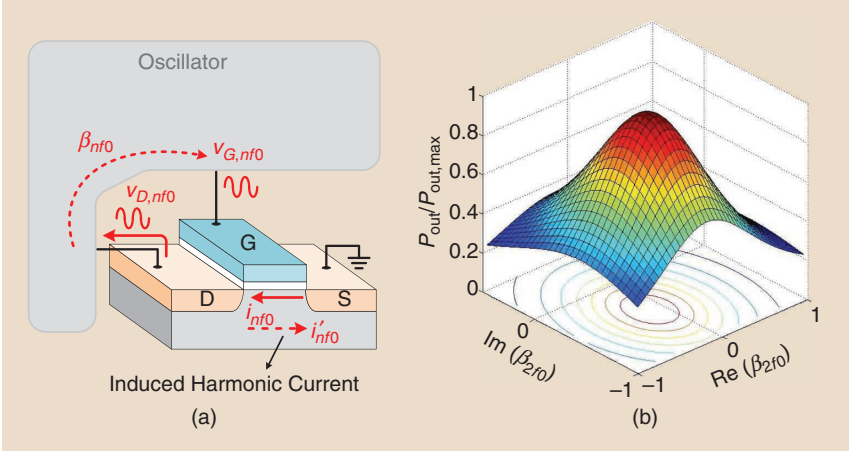

FIGURE 4: (a) The harmonic feedback factor that affects the net harmonic output power from a transistor. (b) The simulated harmonic output power at 260 GHz of a 65-nm NMOS transistor with a varying harmonic feedback factor. In a push–push oscillator, $\mathrm{Re}(\beta_{nf0})$ is 1, and $\mathrm{Im}(\beta_{nf0})$ is 0.

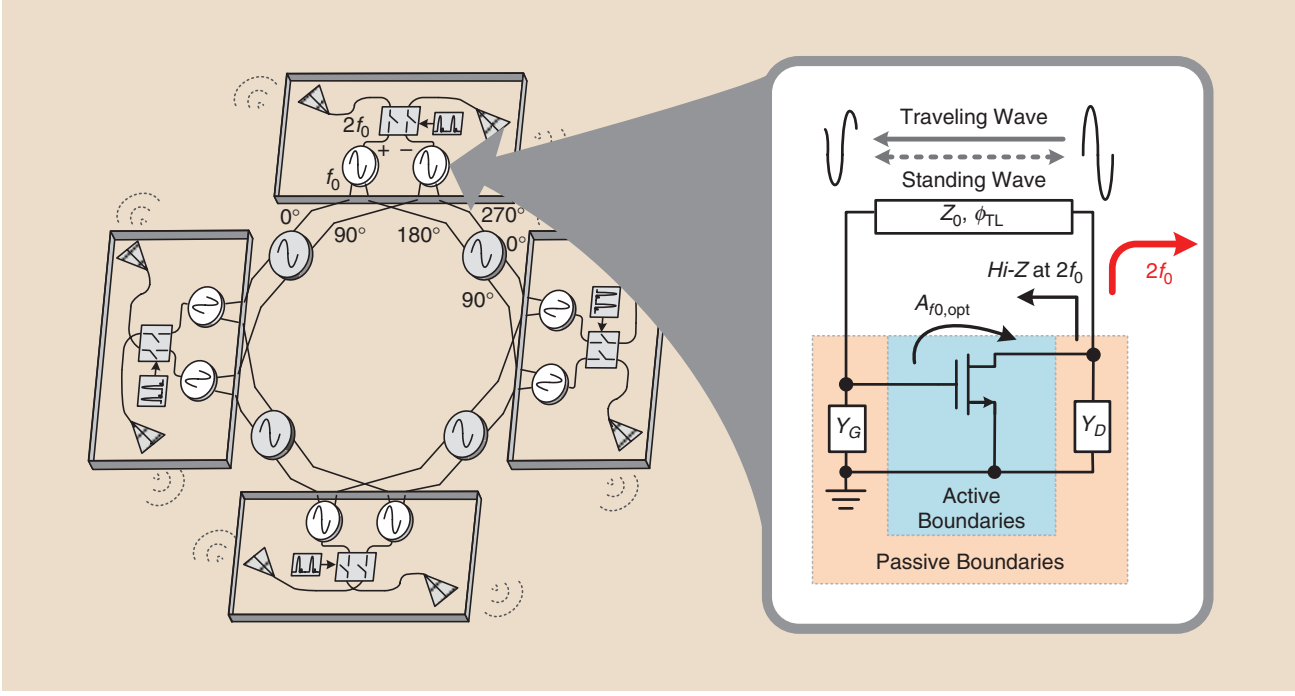

FIGURE 5: The basic schematic of a self-feeding oscillator (right) and the architecture of an eight-element radiator array at 260 GHz [32].

where Z_0 and φ_{TL} are the impedance and electrical length of the TL, respectively, and g_{11} and y_{12} are the *Y*-parameters of the transistor.

At the second-harmonic frequency, the length of the TL ($2\varphi_{TL}$) is chosen to be nearly quarter-wave. [Note that in (1), Z_0 couples with φ_{TL}, which enables the relatively free selection of φ_{TL}.] Such a quarter-wave transformer transforms the low impedance at the gate (due to large C_{gs}) into a much higher one presented on the drain side. Therefore, the high impedance keeps the generated harmonic signal from flowing back to the gate, thus creating effective isolation. In a 260-GHz, 65-nm CMOS oscillator array as shown in Figure 5 [34], eight differential self-feeding oscillators are coupled with phase synchronization, enabling the power combining of their second-harmonic radiation in free space. The radiation is through an on-chip, broadband slot-antenna array implemented using the CMOS metal layers. An external high-resistive, hemispheric silicon lens is attached to the back of the chip to further enhance the backside radiation coupling into the air. This radiator array has a measured radiated power of 1.1 mW, which is the highest among all THz/sub-THz CMOS radiators to date. The chip can also modulate the radiation with ultranarrow (~45 pS) pulses to generate broadband spectrum (~25 GHz), which is useful for THz spectroscopy.

Frequency Multiplier

Although a harmonic oscillator is a self-sustaining circuit that does not require external input, it suffers from narrow output bandwidth due to the increasingly significant transistor parasitic capacitance, which is normally part of the resonance tank. The variable part of the tank, consisting of an MOS varactor, is therefore smaller. To overcome this disadvantage, we can implement oscillators at a lower frequency (i.e., wider tuning range) and then feed the signal into a frequency multiplier to generate a broadband THz frequency.

To increase power efficiency, it is critical to prevent leakage of the fundamental signal at the output, as well as the harmonic signal at the input. As a very straightforward solution, dedicated frequency filters are often employed at the input and output. In THz design, these filters are frequently implemented using quarter- or half-wavelength transmission stubs [35], [36]. However, there are two problems related to such isolation methods. First, these filters are quite bulky in terms of wavelength and are lossy, especially the output high-pass filters at harmonic. [The output filter is designed to block the fundamental signal at f_0. Therefore, it often consists of multisectional quarter-wave resonators at f_0, which means the harmonic signal (e.g., second harmonic) experiences several long, half-wavelength lines before reaching the output.] Second, because they are resonance-type, these filters also limit the bandwidth of the multipliers, so alternative signal-filtering methods are preferred.

While Schottky diodes are widely used in waveguide-housed multipliers [1], [37], MOS or heterojunction bipolar transistors are adopted in almost all previous silicon-based THz frequency multipliers due to their process compatibility [38], [39]. However, this causes additional large dc power consumption. To solve this problem, next we introduce a design based on MOS varactors, a passive variable capacitor available in all CMOS technologies [9]. In a standard 65-nm bulk CMOS process, the dynamic cutoff frequency of the device is as high as 870 GHz, which enables us to efficiently generate a THz signal without dissipating any dc power. However, compared to transistors, the one-port MOS varactor does not provide any isolation between the input and output signals, increasing the challenge for the signal-filtering design mentioned previously in this section.

Instead of filtering the input/output signals based on their frequencies, in our design we separate them based on their wave modes. Such a concept is applied to the design of a 480-GHz CMOS doubler. Shown in Figure 6, this doubler is based on a partially coupled ring structure. Through magnetic coupling, the input signal at f_0 is injected into the ring with a differential pattern (unbalanced-wave mode). The two branches of the signal travel along the left half of the ring and are absorbed by the varactor pair. On the output node of the ring, because the two signals are out of phase, a virtual ground is created that reflects back the signals. The signal at f_0 is therefore blocked from the output.

When the fundamental signals are doubled (in terms of frequency and phase) by the nonlinear capacitors, the two second-harmonic signals in the two branches become in phase (balanced-wave mode). They travel along the right half of the ring until they are extracted and combined at the output. In the left side of the ring, the magnetic fields created by the harmonic signals cancel each other. Therefore, the isolation of the second-harmonic signal at the input is also obtained. Thanks to wave-mode filtering, this doubler structure is very compact and efficient. The chip, fabricated using 65-nm CMOS, occupies only $120 \times 250\ \mu m^2$, excluding pads. In the measurement (Figure 7), the chip is able to provide 230-μW power at 480 GHz with a conversion efficiency of 3.7%. Currently, the output power is limited only by the maximum available power of the input testing source. Given a larger input, we expect to obtain a nearly 1-mW output before the breakdown of the MOS varactors. To the best our knowledge, this doubler has the highest operational frequency among all CMOS doublers.

As mentioned previously, one advantage of frequency multipliers over harmonic oscillators is their broadband nature. Such an advantage, however, is offset if conventional topologies with dedicated filters and resonant-type matching networks are used. Fortunately, as shown in Figure 6, most of the input and output signals are in the form of traveling wave along the TLs. The simulated –3-dB bandwidth of the 480-GHz doubler is as high as 70 GHz

(20 GHz in measurement due to the limited input source bandwidth) [9].

Another example of a traveling-wave multiplier, a 250-GHz doubler [40], is shown in Figure 8. The gates of four MOS transistors probe at different locations of a metal ring. Through an output-matching network, the drains of the transistors are then combined. Upon injection, the input fundamental signal travels along the two branches of the ring until it is reflected back on the other end. The structure is designed so that the forward and backward waves add constructively at each transistor gate, thus enhancing the power efficiency. It is also shown that, with frequency (as well as phase) doubling, the second-harmonic signals from the four drain nodes are in phase, which facilitates power combining. One important

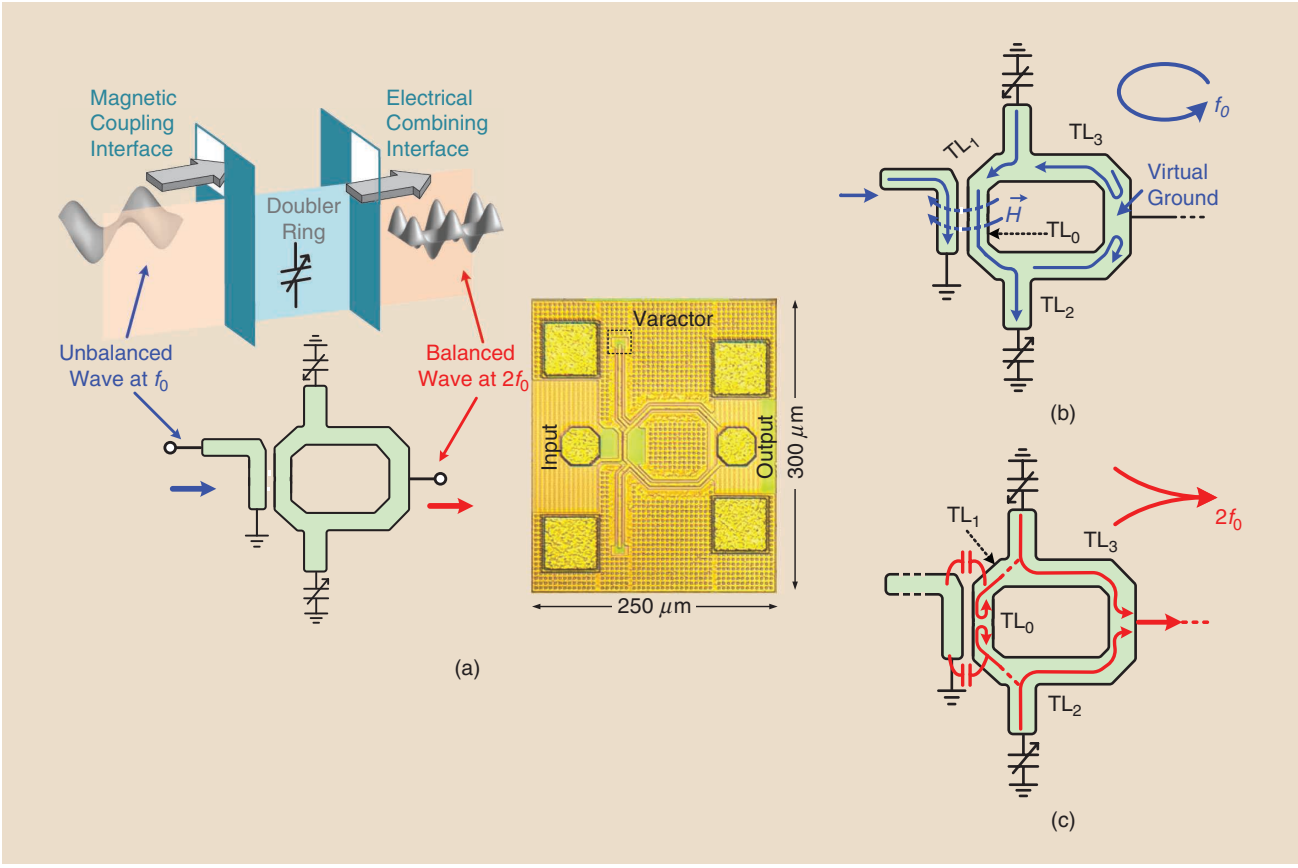

FIGURE 6: (a) The proposed partially coupled ring structure and the die photo of the 480-GHz CMOS doubler. (b) The signal flow at the fundamental frequency and (c) the signal flow at the second harmonic [9].

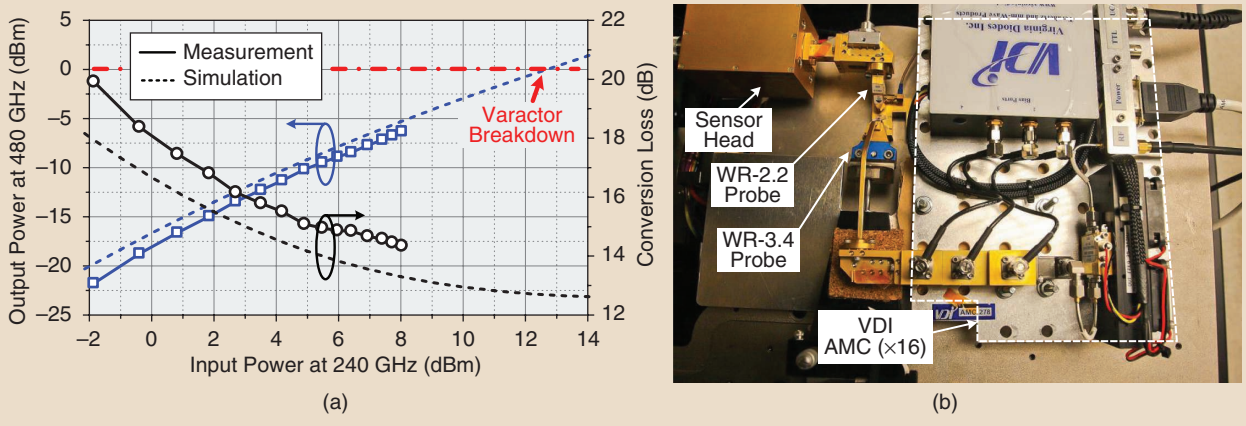

FIGURE 7: (a) The measured output power and conversion loss of the 480-GHz frequency doubler and (b) the testing setup based on on-wafer probing [9]. WR: waveguide; VDI: Virginia Diodes Inc.

feature of this traveling-wave design is that the operation is independent of frequency, although the actual bandwidth is still limited by the input/output matching. The chip has a measured bandwidth of 9 GHz and output power of 230 μW.

Coherent Radiation System: A Scalable Phased-Array Architecture

Given a highly optimized electronic source, how can we arrange multiple replicas of that source in the best way possible to scale the performance? The beauty of this problem is that it transcends specifications such as the operating frequency of the oscillators, specific transistor technology, and required power level or phase noise. However, until recently, a solution to this problem did not appear to be necessary. For many applications, a single electronic source or set of a few electronic sources can be organized in an architecture that serves the purpose for single or multiphase signal generation. In fact, a well-known oscillator figure of merit demonstrates a fundamental tradeoff that exists between an oscillator's three main specifications: center frequency, phase noise, and power consumption. For instance, in RF voltage-controlled oscillators, one can trade more power for better spectral purity.

However, as one pushes an oscillator to its fundamental, these conventional tradeoffs start to break down. Specifically, for a CMOS THz source where the oscillator output is close to or above the f_{max} regardless of the applied dc power, the generated output power and phase noise cannot be improved above a certain level. At such high frequencies, this achievable power level is insufficient for many transceiver-based imaging or sensing applications. As a result, in an integrated THz source, it is imperative to use a large number of devices to achieve a reasonable level of output power or spectral purity.

Indeed, incorporating a large number of small radiators is fundamentally more efficient than increasing the power of a single source. The spatial diversity of a distributed source can focus the beam at the desired point in space. In other words, by distributing a single source into N smaller sources with the same total dc power, the effective radiated power targeted to a certain point can increase by a factor of N. Nevertheless, the main challenge with scaling is to maintain control over the individual elements in the same way that one accesses a single module. In fact, this challenge has shaped the conventional idea for phased-array radiation. As shown in Figure 9, the way multiple sources radiate in a phased array is not by means of individual sources across the grid but by means of a single source distributed across the grid through a global network. The complexity of this global routing becomes noticeable as the number of rows and columns in the array increases or the interconnection coupling and loss begin to affect the performance. For a scalable THz source, both issues are significant, and pursuing the conventional phased-array implementation is not quite fruitful. The saying that "necessity is the mother of invention" is proven, as the only way to have a high-power THz electronic source is to build a scalable source that can uniformly increase the limited performance of individual

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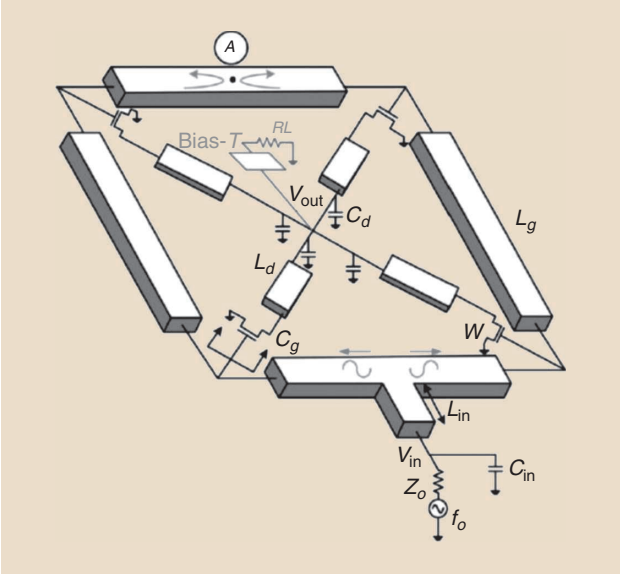

FIGURE 8: The wave propagation inside a 250-GHz CMOS active doubler [31].

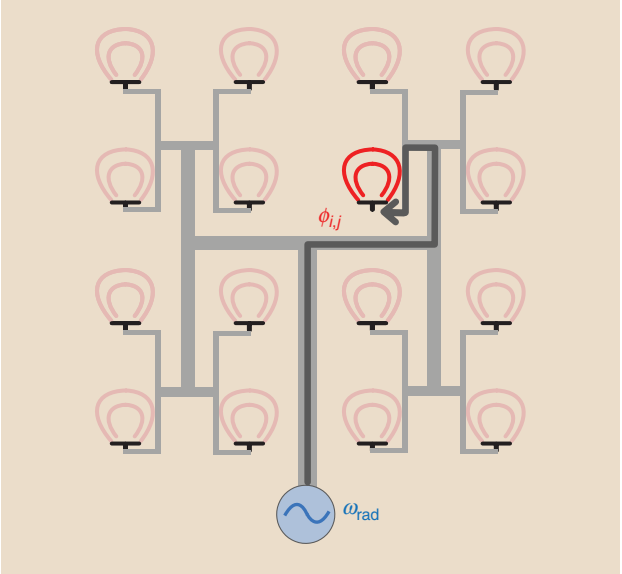

FIGURE 9: The conventional implementation of the phased-array concept.

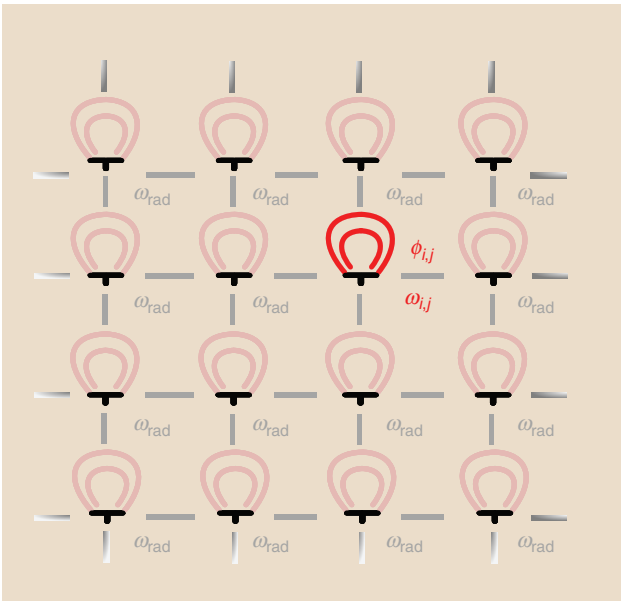

FIGURE 10: An ideal scalable phased-array radiator with local coupling between adjacent cores.

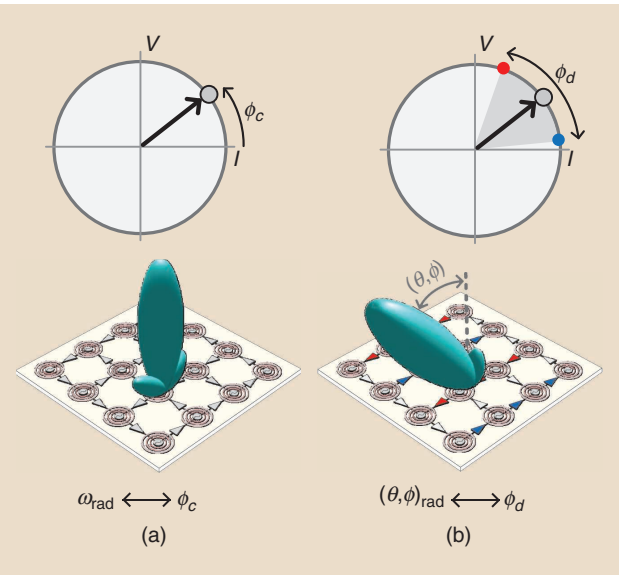

FIGURE 11: (a) The frequency tuning of the phased array by changing the common phase. (b) Phase tuning and beam steering in the array through the performance of differential phase adjustments.

devices without mounting structural complexity. To address this challenge, we have presented a 2D scalable and tunable THz source based on delay-coupled oscillators.

Let us use the orchestra as a metaphor to illustrate the concept of the scalable phased array. In an orchestra, each member in the musical ensemble has access to an instrument that he or she can play independently. However, during a symphony, the musicians synchronize to a single rhythm by observing the conductor and listening to each other. In other words, all the instruments collectively create a symphony composed of independently controlled sources that can adapt their pace to neighboring performers. Similarly, as shown in Figure 10, the THz source consists of an array of independent THz radiators separated from their neighbors by half the wavelength. In this arrangement, instead of a single control unit, the oscillators synchronize to each other as a result of the local coupling between adjacent neighbors. There is no lengthy interconnect and, with the absence of uncertainties due to error and loss of propagation, the scaling of the structure is not bound to a small number of elements.

Interestingly, the method used to adjust the phase and frequency of this structure proves to be quite intuitive. In a ring of oscillators directionally coupled by phase shifters, we show that the synchronized frequency can be controlled by adjusting the coupler phase shifts [41]. We call this common phase shift ϕ_c, which is changed across all couplers. In the 2D array, the same adjustment to the common phase shift will change the synchronized frequency of the radiators. In Figure 11, we illustrate the coupling phase shifts of the network by a bundle of phasors in the array phase space. The common phase shift is, in effect, a superposition of all the phasors. When all phasors are aligned, the radiators are in phase. Now, if the phase shifts of the couplers surrounding one of the radiators change in opposite directions, ϕ_c remains unchanged. However, the phase of that particular node changes according to this differential change, ϕ_d. We demonstrate that a particular mapping exists between all possible changes in the ϕ_ds and all of the angles of the radiated beam of the phase array. This 2D phased-array concept is based on the theory of a coupled

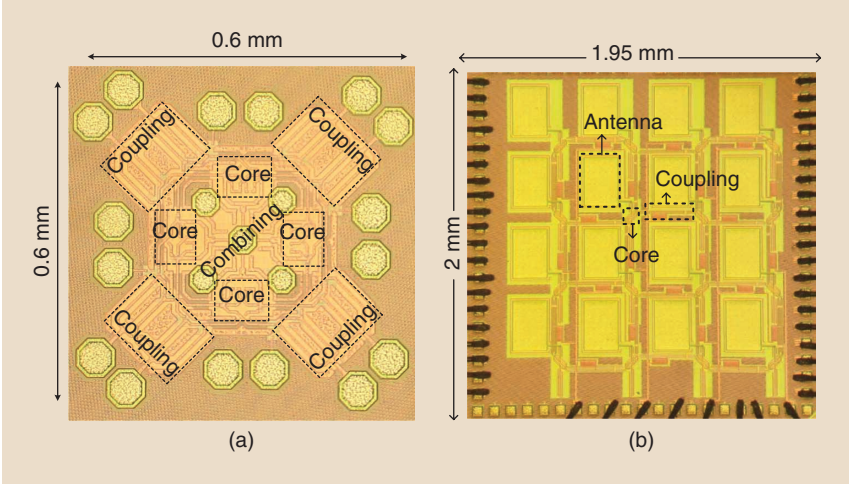

FIGURE 12: Die photos of (a) a 290-GHz delay-coupled tunable oscillator and (b) a 340-GHz tunable phased-array radiator based on delay-coupled oscillators.

oscillator and provides a method to independently control the phase and frequency properties of a scalable structure in a fully distributed fashion. This gives a suitable solution for a THz source that can be scaled without the limitations of previous controlling methods.

To prove the concept, we implement a 4 × 4 phased array at 340 GHz using a standard CMOS process with a sub-THz cutoff frequency (Figure 12). The measured results show that approximately 1 mW in total radiates power from the chip, which translates to more than 50 mW of effective isotropic radiated power. The measured phase noise is also the lowest among any electronic radiating source above 100 GHz [42]. This chip is the first fully integrated THz phased array on CMOS. Furthermore, this concept can be applied to achieve higher radiated power at even higher frequencies, where a larger number of sources can coherently radiate within the same chip area due to shorter wavelengths.

Conclusions

In this article, we showed several examples of smaller circuit blocks as well as a larger scale system. In conclusion, the CMOS and bipolar CMOS processes are very capable at sub-mm-wave and THz frequencies below 1 THz. However, as circuit designers, we need to combine device physics, circuit theory, RF systems, and electromagnetic theory into a coherent design methodology to be able to tackle the challenges of circuit design above 100 GHz.

References

[1] T. W. Crowe, W. L. Bishop, D. W. Porterfield, J. L. Hesler, and R. M. Weikle, "Opening the terahertz window with integrated diode circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 10, pp. 2104–2110, Oct. 2005. doi: 10.1109/JSSC.2005.854599.

[2] M. Arbab, D. Winebrenner, T. Dickey, A. Chen, M. Klein, and P. Mourad, "Terahertz spectroscopy for the assessment of burn injuries in vivo," *J. Biomed. Opt.*, vol. 18, no. 7, pp. 1–8, July 2013. doi: 10.1117/1.JBO.18.7.077004.

[3] E. Pickwell and V. P. Wallace, "Biomedical applications of terahertz technology," *J. Phys. D: Appl. Phys.*, vol. 39, no. 17, pp. R301–R310, Aug. 2006. doi: 10.1088/0022-3727/39/17/r01.

[4] I. Kallfass et al., "All active MMIC-based wireless communication at 220 GHz," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 2, pp. 477–487, Nov. 2011. doi: 10.1109/TTHZ.2011.2160021.

[5] H. Song and T. Nagatsuma, "Present and future of terahertz communications," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 256–263, Sept. 2011. doi: 10.1109/TTHZ.2011.2159552.

[6] B. S. Williams, "Terahertz quantum-cascade lasers," *Nature Photon.*, vol. 1, pp. 517–525, Sept. 2007. doi: 10.1038/nphoton.2007.166.

[7] A. Fosnight, B. Moran, and I. Medvedev, "Chemical analysis of exhaled human breath using a terahertz spectroscopic approach," *Appl. Phys. Lett.*, vol. 103, no. 13, Sept. 2013. doi: 10.1063/1.4823544.

[8] P. Penfield and R. Rafuse, *Varactor Applications*. Cambridge, MA: MIT Press, 1962.

[9] R. Han and E. Afshari, "A high-power broadband passive terahertz frequency doubler in CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1150–1160, Mar. 2013. doi: 10.1109/TMTT.2013.2243465.

[10] H. Aghasi and E. Afshari, "A 0.92-THz SiGe power radiator based on a nonlinear theory for harmonic generation," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 406–422, 2017. doi: 10.1109/JSSC.2016.2627547.

[11] H. Aghasi and E. Afshari, "Design of broadband mm-wave and THz frequency doublers," in *Proc. IEEE 42nd Eur. Solid-State Circuits Conf.*, Lausanne, Switzerland, Sept. 2016, pp. 367–372. doi: 0.1109/ESSCIRC.2016.7598318.

[12] R. Kananizadeh and O. Momeni, "Second-harmonic power generation limits in harmonic oscillators," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3217–3231, Nov. 2018. doi: 10.1109/JSSC.2018.2868283.

[13] M. Adnan and E. Afshari, "A 247-to-263.5 GHz VCO with 2.6 mW peak output power and 1.14% DC-to-RF efficiency in 65 nm bulk CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2014, p. 262. doi: 10.1109/ISSCC.2014.6757427.

[14] H. Khatibi, S. Khiyabani, and E. Afshari, "An efficient high-power fundamental oscillator above $f_{max}/2$: A systematic design," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4176–4189, Nov. 2017. doi: 10.1109/TMTT.2017.2702116.

[15] H. Khatibi, S. Khiyabani, A. Cathelin, and E. Afshari, "A 195 GHz single-transistor fundamental VCO with 15.3% DC-to-RF efficiency, 4.5 mw output power, phase noise FoM of –197 dBc/Hz and 1.1% tuning range in a 55 nm SiGe process," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, Honolulu, HI, 2017, pp., 152–155. doi: 10.1109/RFIC.2017.7969040.

[16] H. Aghasi and E. Afshari, "An 88-GHz compact fundamental oscillator with 19.4% DC-to-RF efficiency and 7.5-dBm output power in 130-nm SiGe BiCMOS," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 5, pp. 106–109, May 2018. doi: 10.1109/LSSC.2018.2875832.

[17] C. Jiang, A. Cathelin, and E. Afshari, "An efficient 210-GHz compact harmonic oscillator with 1.4 dBm peak output power and 10.6% tuning range in 130-nm BiCMOS," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, San Francisco, CA, 2016, pp., 194–197. doi: 10.1109/RFIC.2016.7508284.

[18] S. Shopov, A. Balteanu, J. Hasch, P. Chevalier, A. Cathelin, and S. P. Voinigescu, "A 234–261-GHz 55-nm SiGe BiCMOS signal source with 5.4–7.2 dBm output power, 1.3% DC-to-RF efficiency, and 1-GHz divided-down output," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2054–2065, Sept. 2016. doi: 10.1109/JSSC.2016.2560198.

[19] C. Jiang, A. Cathelin, and E. Afshari, "A 301.7-to-331.8 GHz source with entirely on-chip feedback loop for frequency stabilization in 0.µm BiCMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2018, pp. 372–374. doi: 10.1109/ISSCC.2018.8310339.

[20] Y. Tousi, O. Momeni, and E. Afshari, "A 283-to-296 GHz VCO with 0.76 mw peak output power in 65-nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2012, pp., 258–260. doi: 10.1109/ISSCC.2012.6177000.

[21] Z. Wang, P. Chiang, P. Nazari, C. Wang, Z. Chen, and P. Heydari, "A CMOS 210-GHz fundamental transceiver with OOK modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564–580, Mar. 2014. doi: 10.1109/JSSC.2013.2297415.

[22] K. Sengupta and A. Hajimiri, "A 0.28 THz power-generation and beam-steering array in CMOS based on distributed active radiators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3013–3031, Dec. 2012. doi: 10.1109/JSSC.2012.2217831.

[23] R. Han et al., "A SiGe terahertz heterodyne imaging transmitter with 3.3 mw radiated power and fully-integrated phase-locked loop," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2935–2947, Dec. 2015. doi: 10.1109/JSSC.2015.2471847.

[24] C. Jiang et al., "A fully integrated 320-GHz coherent imaging transceiver in 130 nm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2596–2609, Nov. 2016. doi: 10.1109/JSSC.2016.2599533.

[25] S. Kang, S. V. Thyagarajan, and A. M. Niknejad, "A 240 GHz fully integrated wideband QPSK transmitter in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2256–2267, Oct. 2015. doi: 10.1109/JSSC.2015.2467179.

[26] C. Jiang, A. Cathelin, and E. Afshari, "A high-speed efficient 220-GHz spatial-orthogonal ask transmitter in 130-nm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2321–2334, Sept. 2017. doi: 10.1109/JSSC.2017.2702007.

[27] A. Mostajeran, A. Cathelin, and E. Afshari, "A 170-GHz fully integrated single-chip FMCW imaging radar with 3-D imaging capability," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2721–2734, Oct. 2017. doi: 10.1109/JSSC.2017.2725963.

[28] E. Seok et al., "A 410-GHz CMOS push-push oscillator with an on-chip patch antenna," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2008, pp. 472–473, 629. doi: 10.1109/ISSCC.2008.4523262.

[29] D. Huang, T. R. LaRocca, L. Samoska, A. Fung, and M.-C. F. Chang, "324-GHz CMOS frequency generator using linear superposition technique," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2008, pp. 476–477, 629. doi: 10.1109/ISSCC.2008.4523264.

[30] K. Sengupta and A. Hajimiri, "Distributed active radiation for THz signal generation," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2011, pp. 288–289. doi: 10.1109/ISSCC.2011.5746322.

[31] O. Momeni and E. Afshari, "High power terahertz and submillimeter-wave oscillator design: A systematic approach," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 583–597, Mar. 2011. doi: 10.1109/JSSC.2011.2104553.

[32] R. Han and E. Afshari, "A CMOS high-power broadband 260-GHz radiator array for spectroscopy," *IEEE J. Solid-State Circuits*,

vol. 48, no. 12, pp. 3090–3104, Dec. 2013. doi: 10.1109/JSSC.2013.2272864.
[33] Y. Tousi, O. Momeni, and E. Afshari, "A novel CMOS high-power terahertz VCO based on coupled oscillators: Theory and implementation," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3032–3042, Dec. 2012. doi: 10.1109/JSSC.2012.2217853.
[34] R. Han and E. Afshari, "A 260-GHz broadband source with 1.1mW continuous-wave radiated power and EIRP of 15.7dBm in 65nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2013, pp. 138–139. doi: 10.1109/ISSCC.2013.6487671.
[35] U. R. Pferiffer, C. Mishra, R. M. Rassel, S. Pinkett, and S. K. Reynolds, "Schottky barrier diode circuits in silicon for future millimeter-wave and terahertz applications," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 2, pp. 364–371, Feb. 2008. doi: 10.1109/TMTT.2007.914656.
[36] C. Mao, C. Nallani, S. Sankaran, E. Seok, and K. K. O. "125-GHz diode frequency doubler in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1531–1538, May 2009. doi: 10.1109/JSSC.2009.2016995.
[37] A. Maestrini et al., "A 540–640-GHz high-efficiency four-anode frequency tripler," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 9, pp. 2835–2843, Sept. 2005. doi: 10.1109/TMTT.2005.854174.
[38] E. Ojefors, B. Heinemann, and U. Pfeiffer, "Active 220- and 325-GHz frequency multiplier chains in an SiGe HBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 5, pp. 1311–1318, May 2011. doi: 10.1109/TMTT.2011.2114364.
[39] B. Cetinoneri, Y. Atesal, A. Fung, and G. Rebeiz. "Band amplifiers with 6-dB noise figure and milliwatt-level 170–200-GHz doublers in 45-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 692–701, Mar. 2012. doi: 10.1109/TMTT.2011.2165964.
[40] O. Momeni and E. Afshari, "A broadband mm-wave and terahertz traveling-wave frequency multiplier on CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2966–2976, Dec. 2011. doi: 10.1109/JSSC.2011.2162469.
[41] Y. Tousi, V. Pourahmad, and E. Afshari, "Delay coupled oscillators for frequency tuning of solid-state terahertz sources," *Phys. Rev. Lett.*, vol. 23, no. 108, p. 234101, June 2012.
[42] Y. Tousi and E. Afshari, "A scalable THz 2D phased array with 17dBm of EIRP at 338 GHz in 65nm bulk CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2014, pp. 258–259.

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