29.5 Sub-THz CMOS Molecular Clock with 43ppt Long-Term Stability Using High-Order Rotational Transition Probing and Slot-Array Couplers

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Future ultra-broadband and low-latency radio access networks pose stringent specifications for time synchronizations. For 5G base stations, inter-site timing error should be <130ns for carrier aggregation and <10ns for high-accuracy positioning [1], requiring a 10^{-10}-level relative drift for a 1min clock holdover. Meanwhile, massive deployments of compact access nodes also make small size, power, and cost indispensable for clocks. Oven-controlled crystal/MEMS oscillators (OCXO/OCMO) with moderate cost are currently used. But, their resonators exhibit long-term aging and high-temperature sensitivity (-31ppm/K for MEMS resonators), hence requiring up to a watt-level heater power for temperature stabilization. Referencing clocks to invariant physical constants well solves the drifting issue. To this end, chip-scale atomic (Cs or Rb) clocks (CSACs) [2-4] have achieved outstanding stability, low power (120mW in [3]) and miniaturization. However, the highly complicated optical-electrical components (e.g., VCSEL laser with high wavelength accuracy), integration, and packaging (e.g. heater with mK-accuracy temperature control, magnetic shield, buffer gas) lead to very high cost (>$1k [3]). Recently, molecular clock referenced to sub-THz rotational transitions of carbonyl sulfide (OCS) gas emerged as a fully electronic solution with high stability [5]. In particular, chip-scale molecular clock (CSMC), built using a CMOS chip coupled with a waveguide OCS molecular cell, appeared as highly attractive for miniaturization and significant cost reduction. In [5], the long-term stability (3.8×10^{-10}@ averaging time $\tau=10^3$s) of the CSMC was limited by the non-ideal measured OCS transition curve, which is susceptible to environmental disturbance. This paper presents a 70mW CSMC chip design that enables high-order dispersion-curve locking and enhances the long-term stability by 9×. Additional testing results also reveal its advantages in temperature stability over OCXO/OCMO and magnetic sensitivity over CSAC, respectively.

Figure 29.5.1 shows the clock architecture. Two cascaded PLLs (3.21GHz $\Delta\Sigma$ and 57.77GHz integer-*N*) and a quadrupler form the spectroscopy transmitter (TX). A subthreshold MOSFET square-law detector, a variable-gain amplifier (VGA), and a harmonic-rejection lock-in detector (HRLKD) form the spectroscopy receiver (RX). The TX is referenced to an on-chip 60MHz voltage-controlled crystal oscillator (VCXO) with an off-chip quartz crystal (XTAL). The TX signal is coupled into/out of a single-mode WR4.3-waveguide molecular cell to probe the transition line of OCS molecules at $f_0\approx$231.06GHz. The TX probing signal $f_p(t)$ with an average frequency of f_{p0} is wavelength modulated (WM) at a rate of f_m=100kHz. While sweeping the transition line, the gas absorption introduces an envelope fluctuation $V_{env}(t)$ with the period of $1/f_m$. The N^{th}-order odd harmonics ($V_{LK,N}$ in Fig. 29.5.1) of $V_{env}(t)$ are recorded as dispersion curves shown in Fig. 29.5.2. Ideally, for symmetric OCS line profile, $V_{LK,N}$=0 at $f_{p0}=f_0$. Then, a negative frequency-feedback loop is established, shown in Fig. 29.5.1, which dynamically adjusts the f_{XO}=60MHz output. In practice, the gas-free transmission baseline of the CSMC is not leveled, due to the standing wave inside the gas cell and the non-flat TX-RX frequency response. Thus, an offset voltage (V_{Offset} in Fig. 29.5.2) appears on the 1st-order dispersion curve ($V_{LK,1}$ as a function of f_{p0}), which can be comprehended as the 1st-order derivative of the asymmetric OCS line profile. Consequently, with the OCS absorption changing with temperature, the zero-crossing point of the dispersion curve at $f_{p0}=f_0$ and hence f_{XO} drift (Fig. 29.5.2). That happens in the CSMC in [5].

Stability enhancement can be achieved by using a higher-order dispersion curve (N=3, 5…), where the baseline tilting becomes negligible with an equivalent high-order derivative [5]. However, two challenges remain. First, instead of the discrete FSK modulation in [5], a continuous sinusoidal WM with high accuracy is required. Second, the *SNR* drops rapidly with the probing of higher-order dispersion curves, which increases the clock short-term instability ($\propto SNR^{-1}$). For the first challenge, the 57.77GHz VCO in TX PLL2 is chirped by a high-accuracy differential sine signal at f_m=100kHz, which is generated by a pair of 8b DACs and then fed to a pair of small varactors in the VCO (Fig. 29.5.2). Since an ultra-small frequency deviation ($\Delta f\approx$2MHz or 9×10^{-6} of 231.06GHz) is required for optimal line probing, resistive source degeneration is adopted to reduce the VCO sensitivity. The modulator also has a 3b attenuator for fine tuning of Δf. The loop bandwidth (~10kHz) of the 57.77GHz PLL is designed to be much smaller than f_m=100kHz to prevent disturbing WM. The presented dual-PLL architecture also realizes better trade-off between modulation accuracy and phase noise. Lastly, a quadrupler with a 115.5GHz slot balun [6] multiplies the VCO output to 231.06GHz. In this work, the 3rd-order dispersion curve is used instead of 5th-order, considering a trade-off between long-term stability enhancement and the *SNR* degradation. To enable 3rd-order locking, a reference clock of $f_{LKREF}=3f_m$ is generated by WM and fed into the RX HRLKD. The HRLKD is passive and presents >80dB harmonic rejection ratio and <10μV DC offset voltage at its differential output. To ensure correct polarity and maximize the slope at zero-crossing point of the dispersion curve, a phase alignment between the 3rd-harmonic component in the RX baseband and the f_{LKREF} signal is achieved by a 10b phase shifter in WM. At the start-up of the CSMC, before the PLL and HRLKD initialize, the gain of the off-chip DC amplifier, GDC, (Fig. 29.5.1) is reduced to unity first to avoid disturbing the clock loop. After the initialization, the gain of GDC is increased to 10^4, so that the CSMC is locked to the spectral-line center with sufficiently small error.

Next, to boost the spectroscopic *SNR*, our chip adopts a pair of slot array couplers (SAC) for low-loss chip-gas-cell waveguide connection. The 2×2 double-slot radiators of the SAC collimate the beam and radiate downward into the waveguide aperture ($1.09\times0.55mm^2$) through the unthinned (T=305μm) silicon substrate of the chip (Fig. 29.5.3). For efficient coupling, the array geometry is also shaped so that the electrical-field distribution at the silicon-waveguide interface matches the TE_{10} mode of the waveguide. The simulated loss and 3dB fractional bandwidth of the SAC are 5.2dB and 22%, respectively. 60dB isolation is simulated between the TX and RX SACs. Compared to prior THz chip couplers, this design does not require any external component. In addition, since the wave is confined inside the substrate, it also allows for robust clock operation against variation of the chip surroundings.

The chip adopts a 65nm bulk CMOS process with a DC power consumption of 70mW. The peak output power of the 231GHz TX (Fig. 29.5.4), measured by PM5 power meter, is -9.4dBm (-4.2dBm excluding the SAC loss), which approaches the molecular power saturation threshold [5]. Measured by VDI frequency extender, the TX also shows a 27GHz (12%) of the PLL locking range. The matching between the simulated and measured TX power in Fig. 29.5.4 indicates the effectiveness of the SACs. Next, note that TX phase noise leads to PM-to-AM noise conversion in the clock and lowers its stability. At 231.06GHz, the measured phase noise of the unmodulated TX (including the on-chip VCXO) output is -60.7dBc/Hz @100kHz offset and -81.5dBc/Hz @1MHz offset, respectively. Figure 29.5.4 also shows the spectrum of the modulated TX, with the desired deviation frequency of Δf=2.5MHz. The measured noise equivalent power (NEP) of the RX is $62.8pW/Hz^{0.5}$ ($19.0pW/Hz^{0.5}$ excluding the SAC loss) at 100kHz baseband frequency. When probing the OCS transition, the measured 3rd-order dispersion curve (Fig. 29.5.5) exhibits 256× smaller offset (V_{Offset}=4.3μV) than that of the 1st-order curve (V_{Offset}=1.1mV). With 3rd-order locking (SNR_{1Hz}=65.7dB) and a 0.09Hz clock open-loop unity-gain bandwidth, the measured overlapping Allan Deviation (ADEV) are 3.2×10^{-10} @τ=1s and 4.3×10^{-11} @$\tau=10^3$s, respectively, which further bridges the performance gap between CSMCs and CSACs. Furthermore, as predicted in [5], the measured magnetic sensitivity of the unshielded clock, being 4×10^{-10} at 75Gauss or $\pm2.9\times10^{-12}$/Gauss, is 31× better than that of the CSAC with magnetic shielding [3]. Lastly, through an on-chip temperature sensor and a simple 2nd-order polynomial compensation, the frequency drift is $\pm3.0\times10^{-9}$ over a temperature range of 27 to 65°C. Compared with TCXOs and OCXOs in Fig. 29.5.6, this work achieves higher combined temperature-stability-power performance, while keeping the size and cost low.

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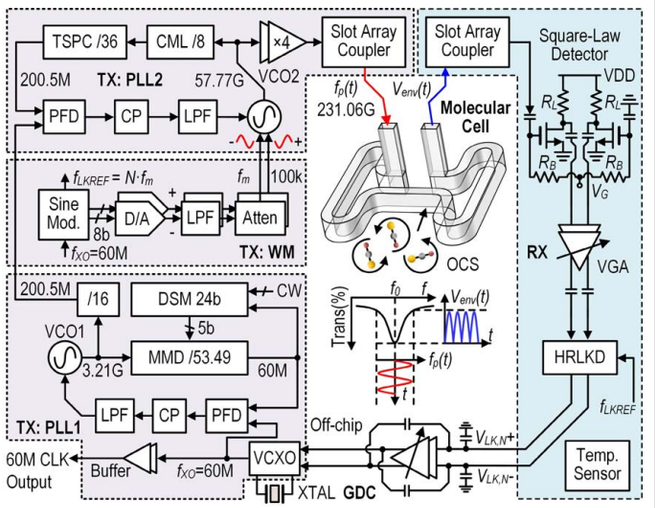

Figure 29.5.1: System architecture of molecular clock with off-chip molecular cell, XTAL, and DC gain stages.

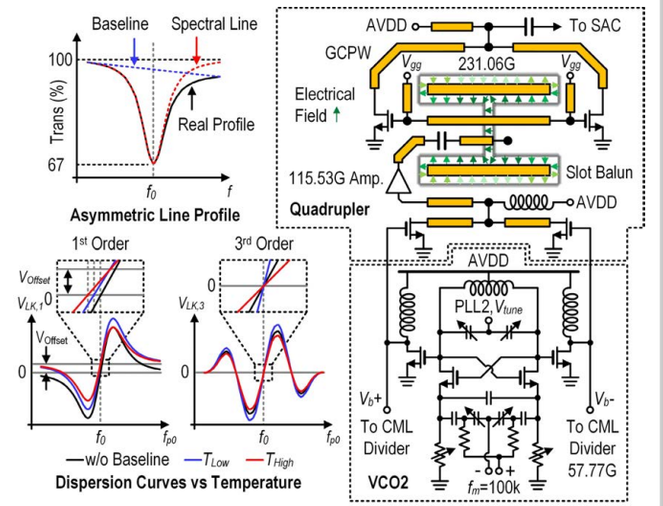

Figure 29.5.2: Locking to high-order dispersion curve center: theorem and schematic.

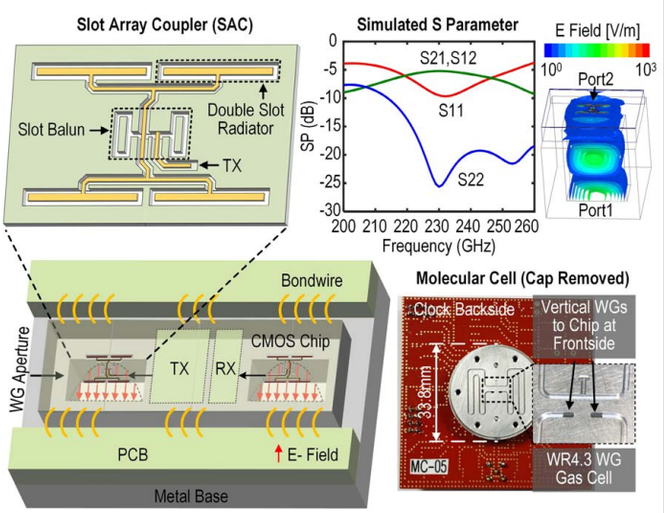

Figure 29.5.3: Slot-array coupler (SAC) and OCS molecular cell.

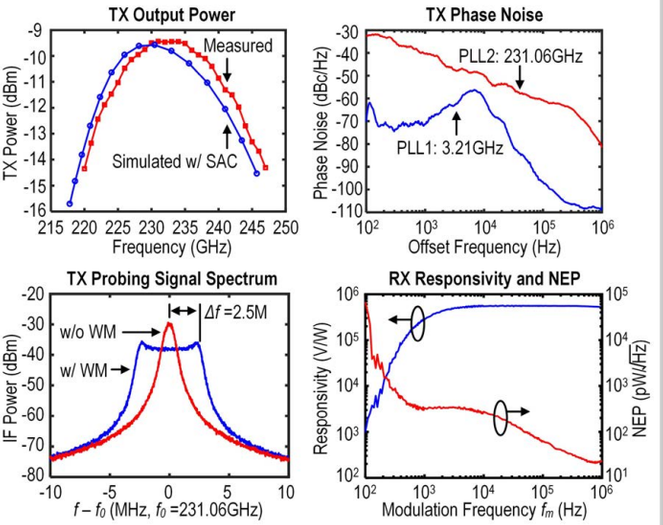

Figure 29.5.4: Measured CMOS TRX performance for spectral line probing.

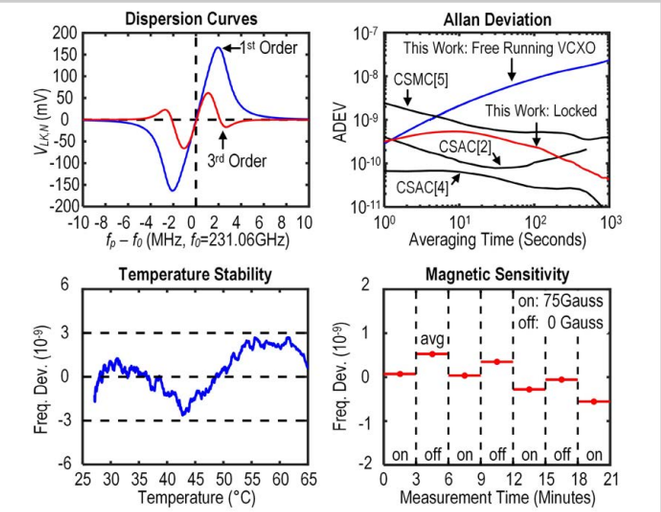

Figure 29.5.5: Measured dispersion curves, Allan deviation, temperature stability, and magnetic sensitivity.

Comparison of Molecular Clocks

	[5]	This Work
Frequency Reference	231.061GHz Rotational Transition of $^{16}O^{12}C^{32}S$	
Implementation	65nm CMOS IC + Gas Cell + Crystal Oscillator	
Gas Cell Coupler	External Quartz Probe	On-Chip Integrated
Order of Disp. Curve Locking	1st	3rd
ADEV (τ=10⁰s)	2.4×10^{-9}	3.2×10^{-10}
ADEV (τ=10³s)	3.8×10^{-10}	4.3×10^{-11}
Temp. Stability †	N/A	±3.0ppb (w/ T.C.) ±54ppb (w/o T.C.)
Mag. Sens. (G^{-1})	N/A	$\pm2.9\times10^{-12}$
DC Power (mW)	66	70

†: Measured temperature range: 27 to 65°C.

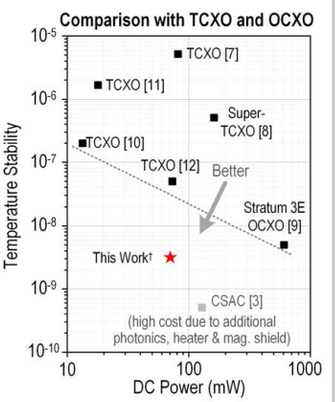

Figure 29.5.6: Performance-comparison table.

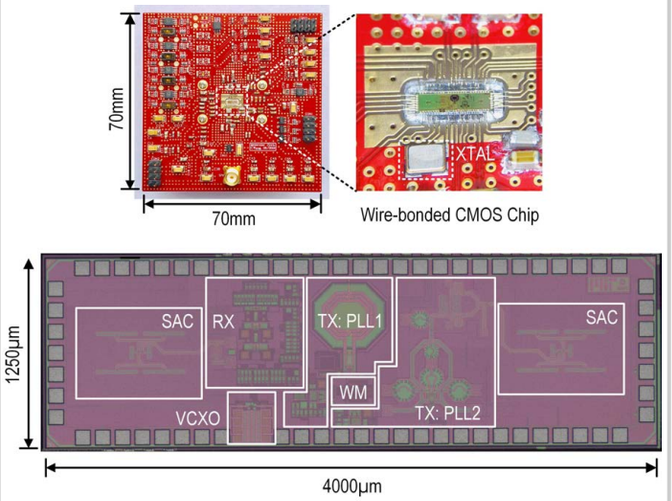

Figure 29.5.7: Die micrograph and packaging.

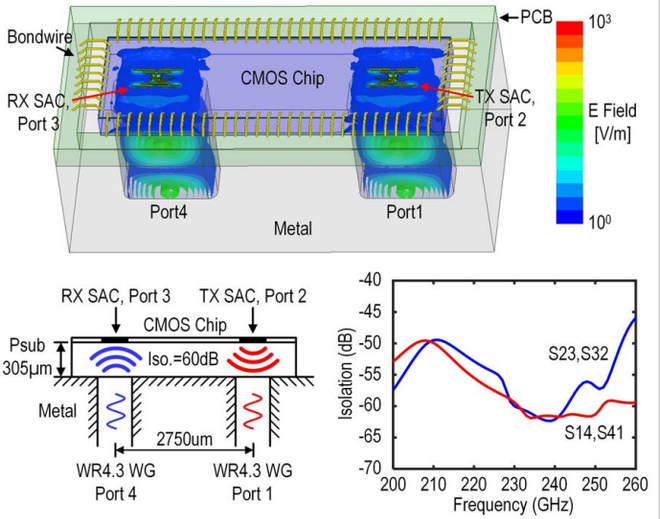

Figure 29.5.S1: Simulated E-field distribution and isolation of TX and RX SACs.

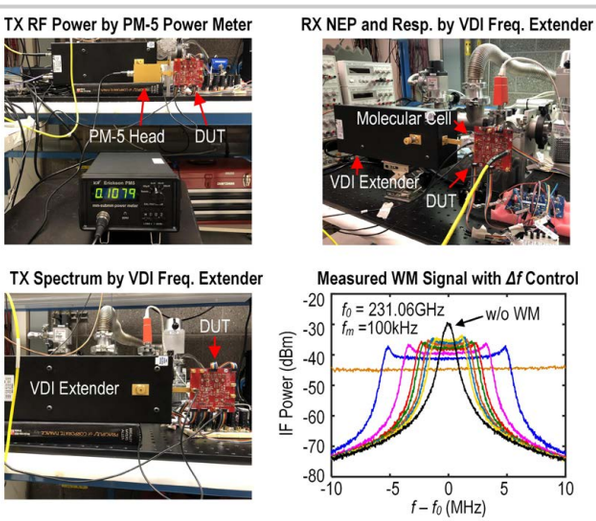

Figure 29.5.S2: RF performance characterization using a test sample with independent TX and RX access.

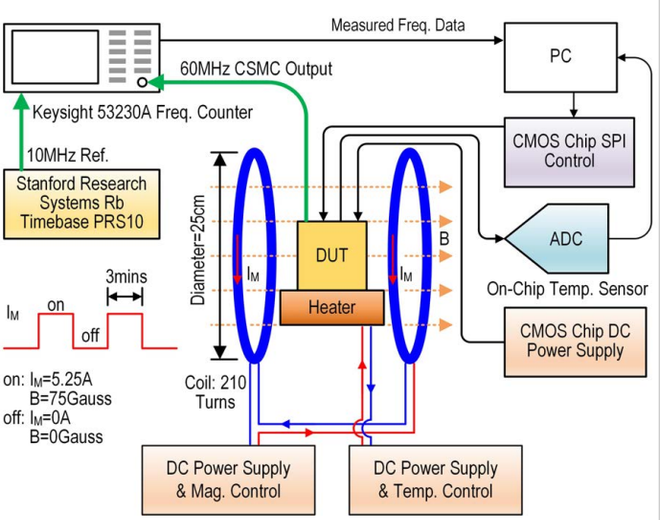

Figure 29.5.S3: Schematic for clock stability measurement.

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