Sub-THz CMOS Molecular Clock with 43*ppt* Long-Term Stability Using High-Order Rotational Transition Probing and Slot-Array Couplers

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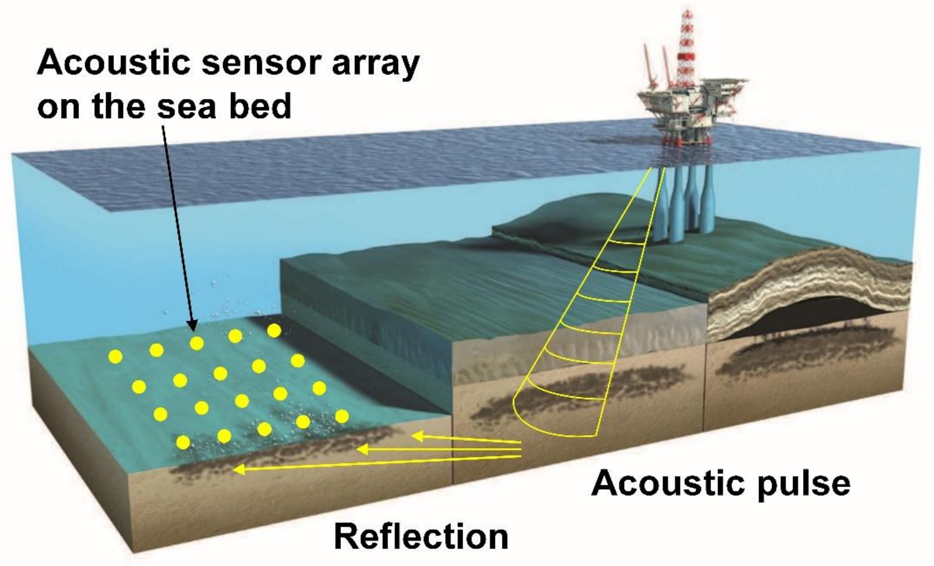
Massachusetts Institute of Technology

Outline

- Background
- High-order locking for long-term stabilization
- Architecture and circuit design
- Measurement results
- Conclusions

Ultra-Stable, Miniaturized Clocks

[researchsnipers.com]



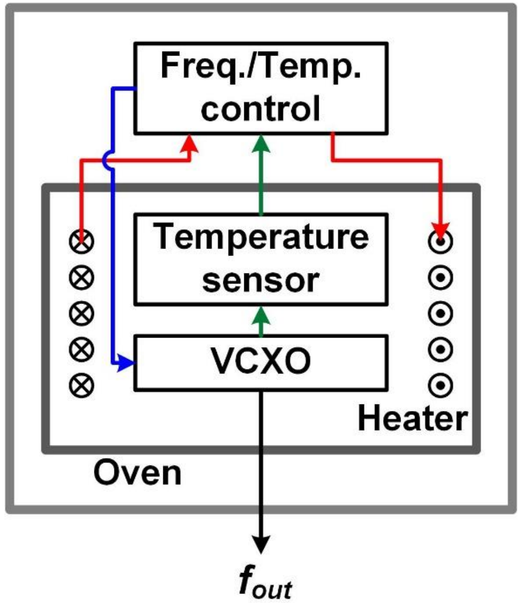
Synchronization of high-speed radio access networks

- 5G massive MIMO → σ_t < 65ns
- Precise positioning → σ_t < 10ns
- 1-min holdover → $\Delta f < 10^{-10}$

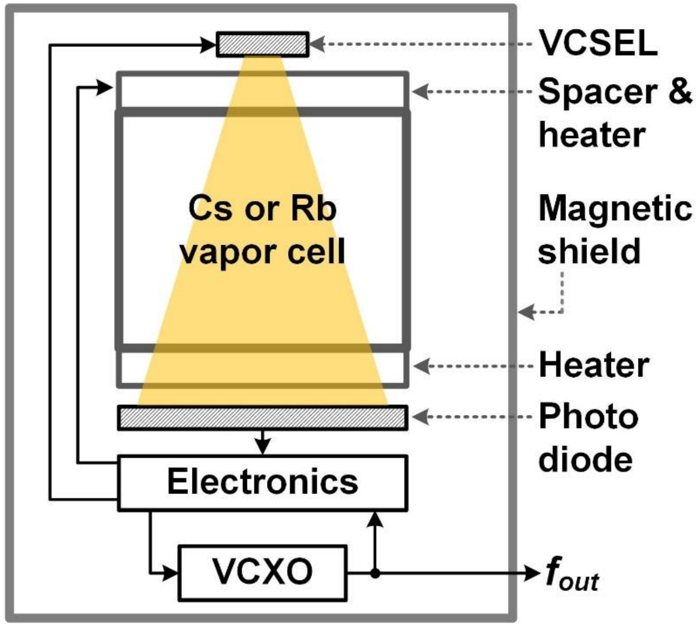
Precise timing for underwater oil exploration

- Temp. variation → $\Delta f < 10^{-9}$
- Deployment time → *Weeks*
- DC Power → *~100mW*

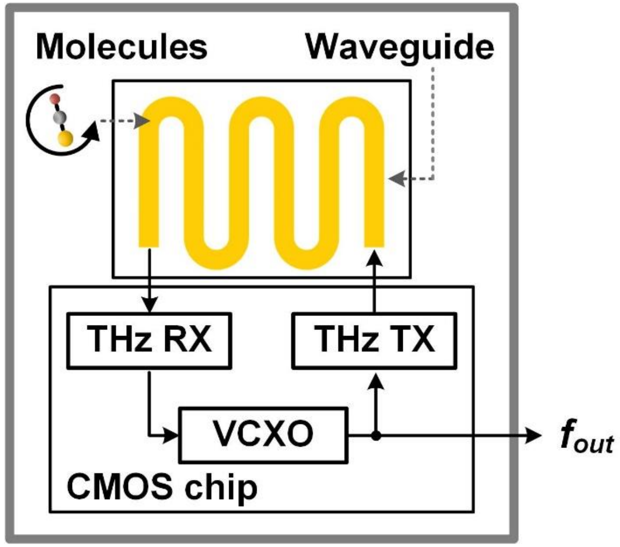
Comparison of Portable Clocks



Oven compensated crystal oscillator (OCXO)



Chip-scale atomic clock (CSAC)



Chip-scale molecular clock (CSMC) (This work)

	OCXO	CSAC	CSMC
Stability	~10^{-10}@10^3s	~10^{-11}@10^3s	~10^{-11}@10^3s
Power	~1W	~100mW	~100mW
Cost	~$100	~$1000	~$10

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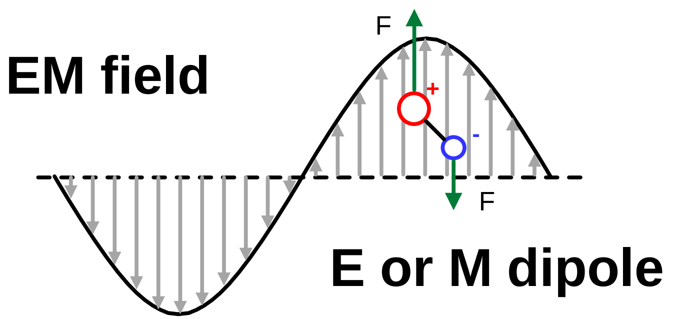
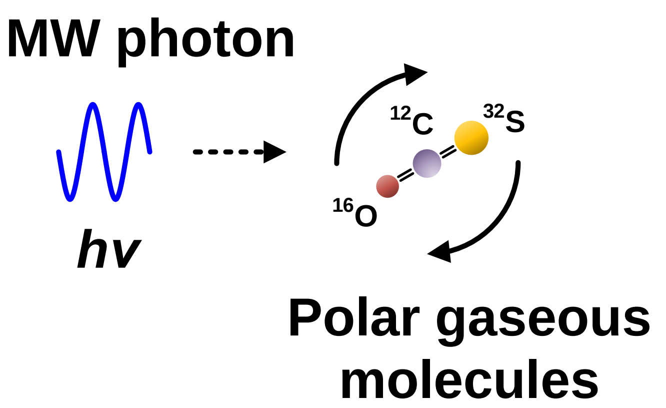
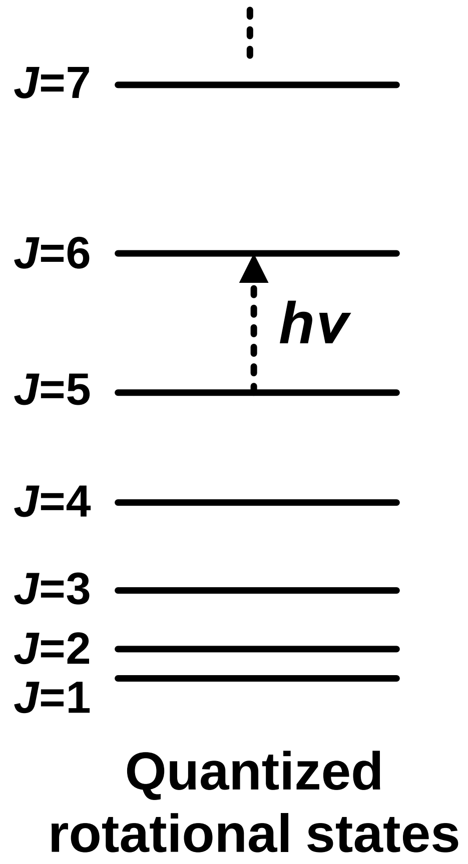
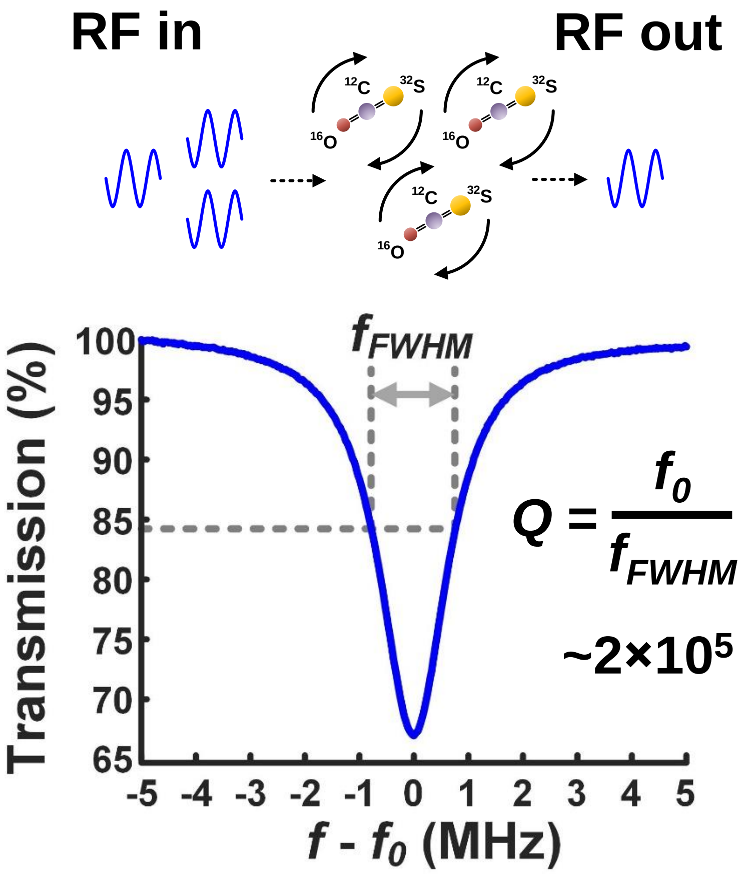
Rotational Spectra of Polar Gaseous Molecules







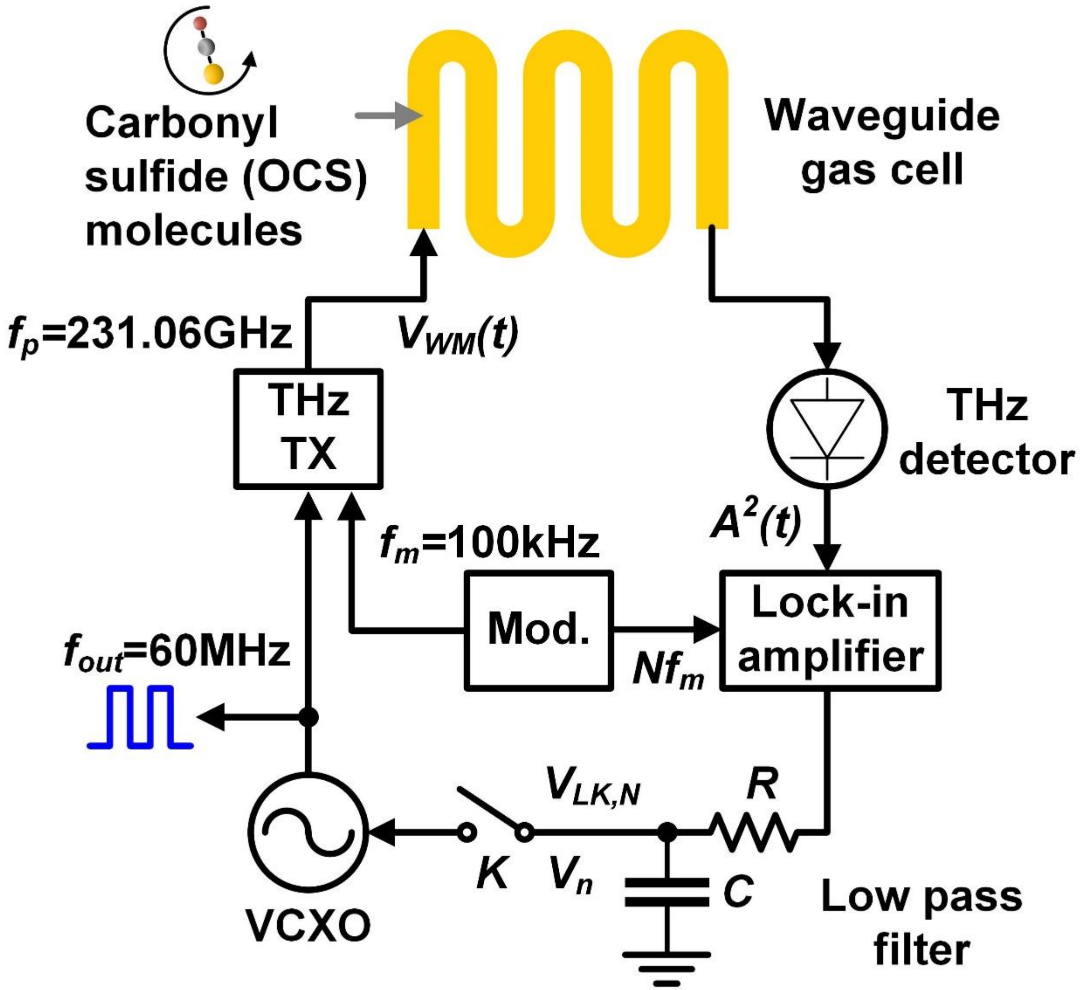


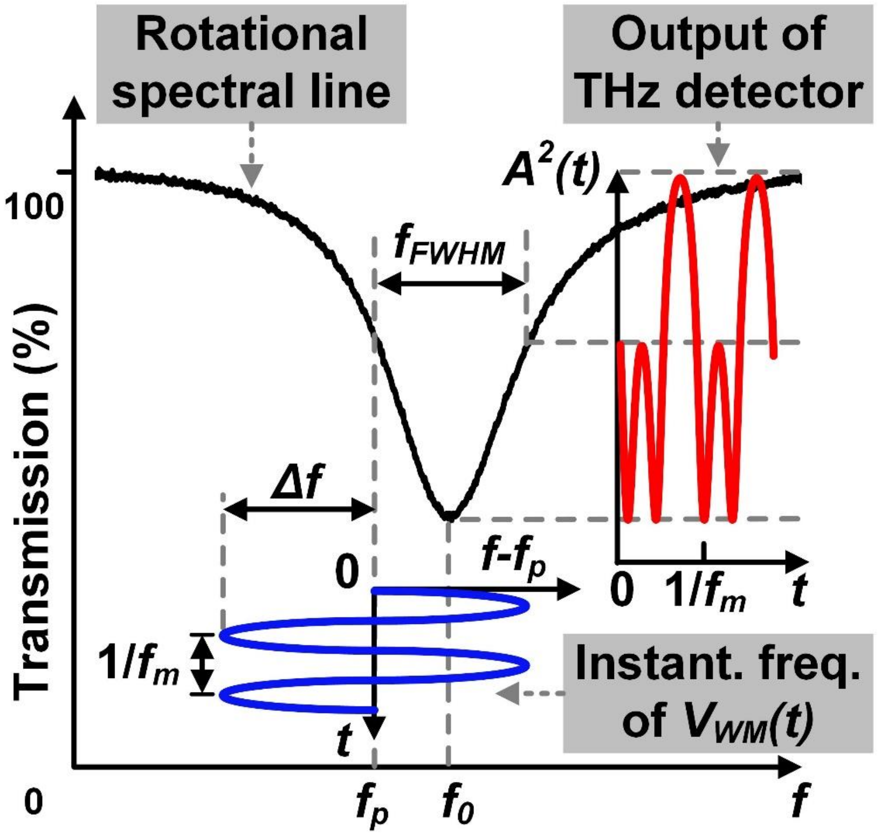
E/M torque → molecular rotation

Photon absorption → state transition (*J*→*J+1*)

Rotational spectra observed in WG gas cell

Wavelength Modulation Spectroscopy (WMS)



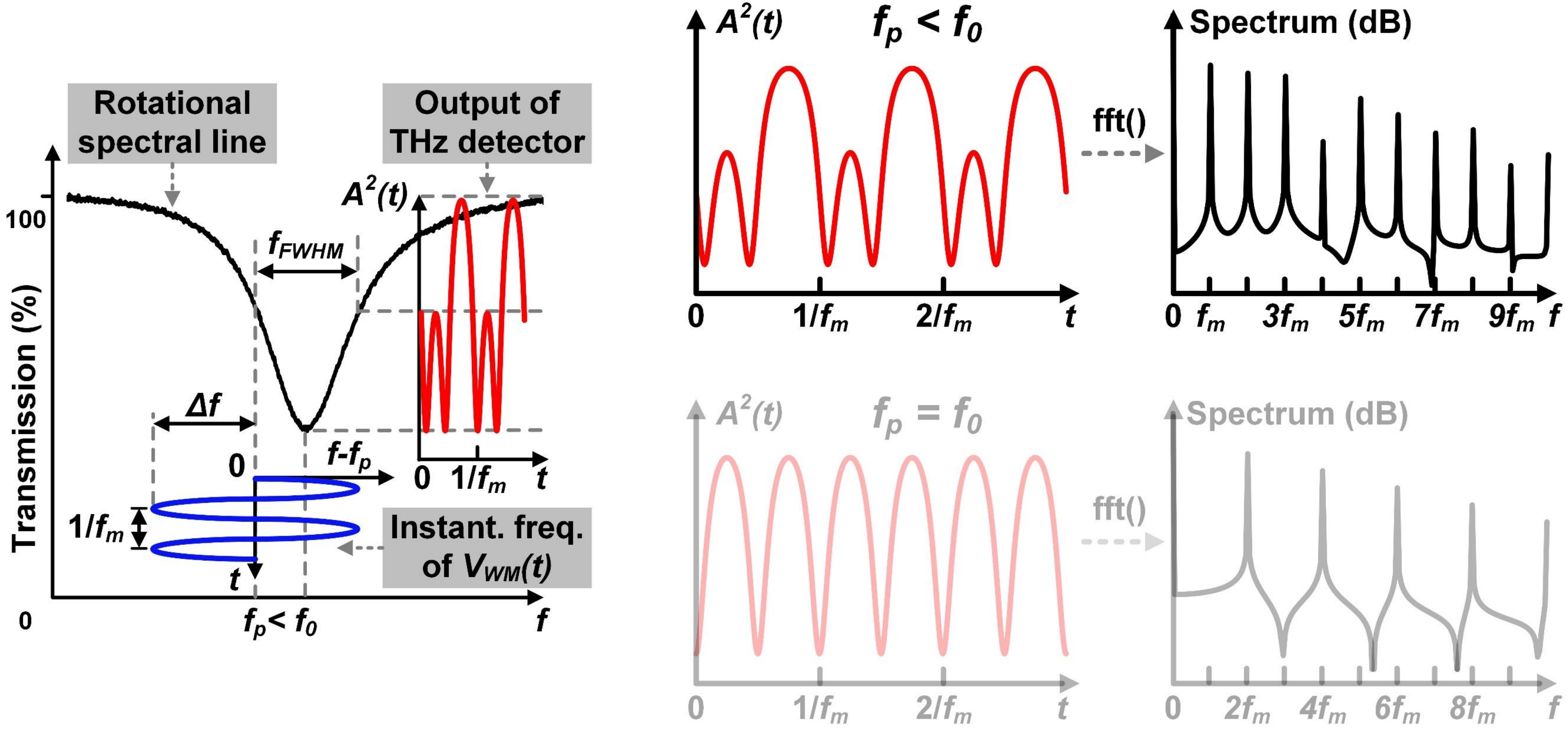


$$V_{WM}(t) = A(t) \cdot \sin[2\pi f_p t + \Delta f \cdot \sin(2\pi f_m t + \theta_0)]$$

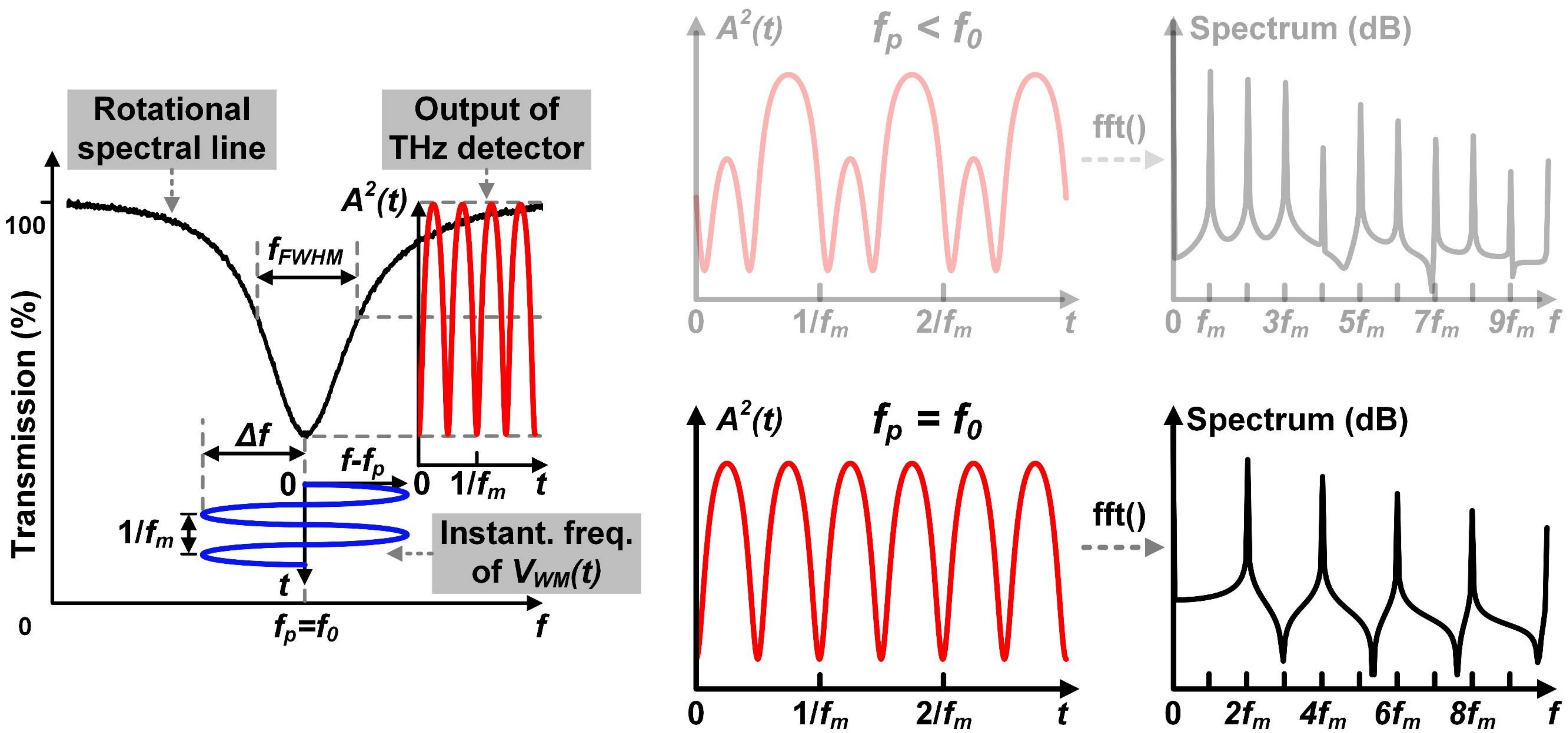
f_m - Modulation freq. Δf - Freq. deviation

- *K*: "open" → rotational spectrometer

High Order Harmonics of f_m

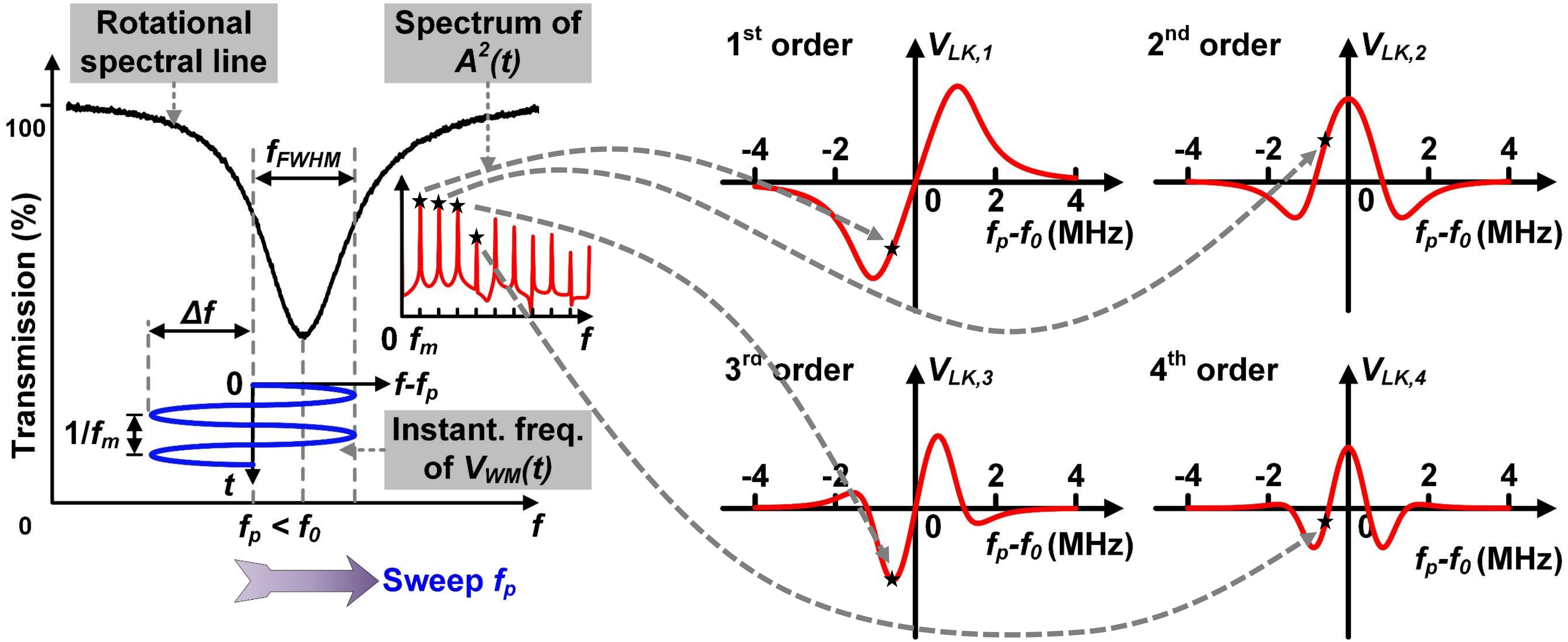


High Order Harmonics of f_m



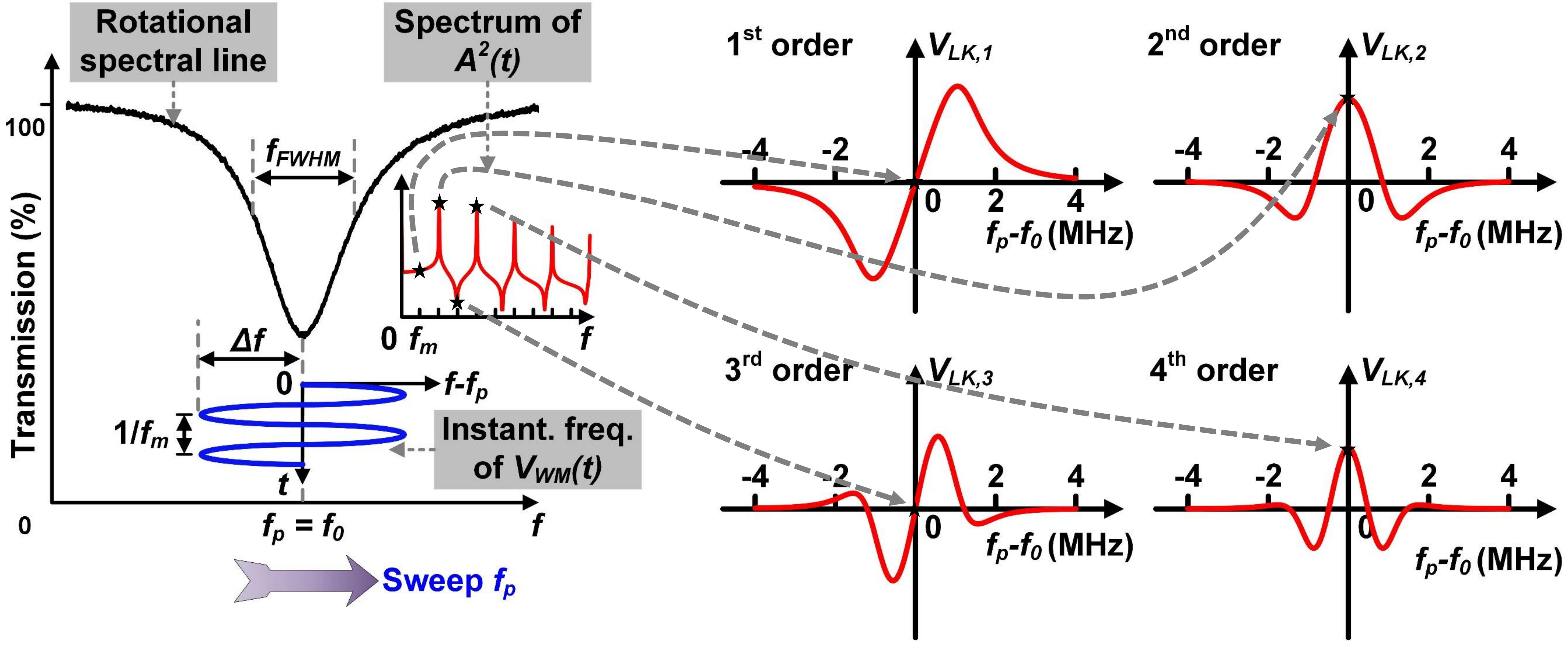
Multi-Order Dispersion Curves

N^{th} order dispersion curve ≈ N^{th} order derivative

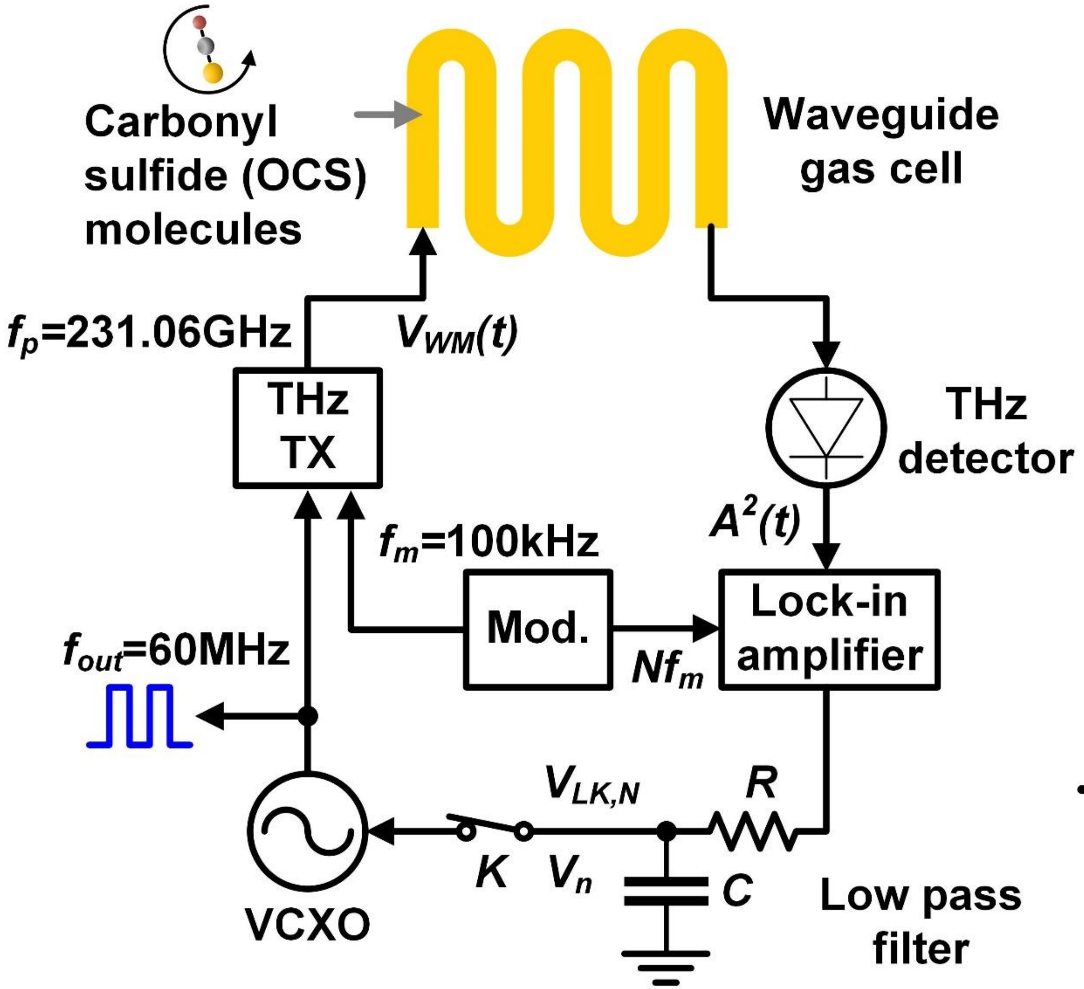


Multi-Order Dispersion Curves

Odd order curves → zero-crossing point



Molecular Clock Locking to Spectral Line Center



Allan deviation:

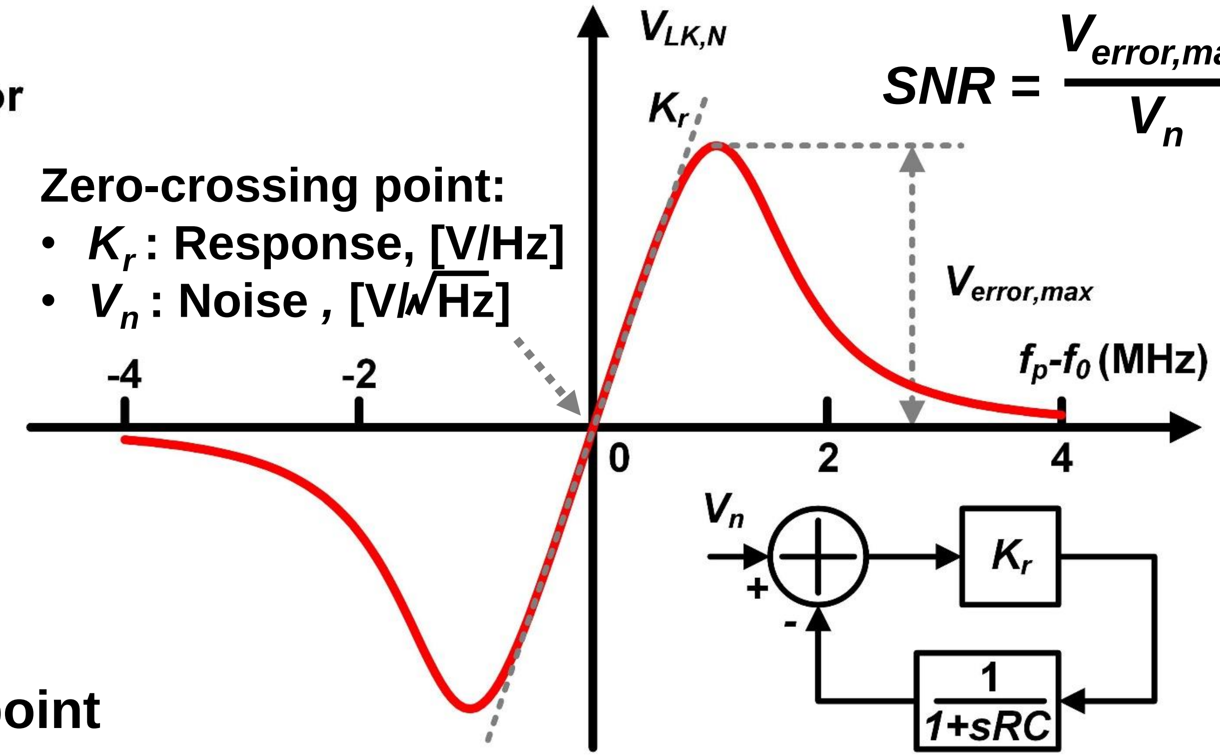
$$\sigma_y = \frac{V_n}{\sqrt{2\tau} \cdot K_r \cdot f_0} \approx \frac{N_0}{\sqrt{\tau} \cdot Q \cdot SNR}$$

τ - Avg. time

$$SNR = \frac{V_{error,max}}{V_n}$$

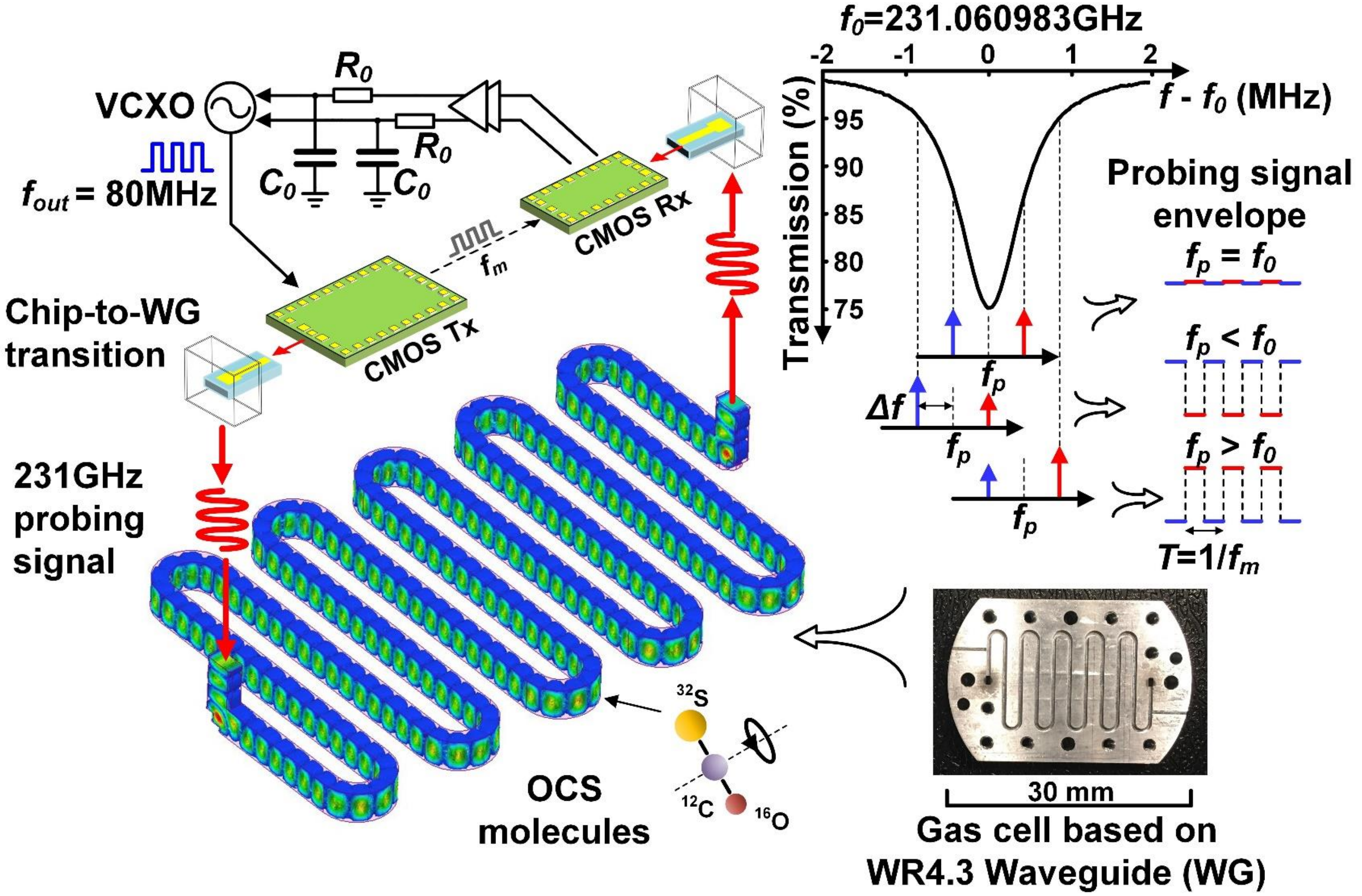
Zero-crossing point:

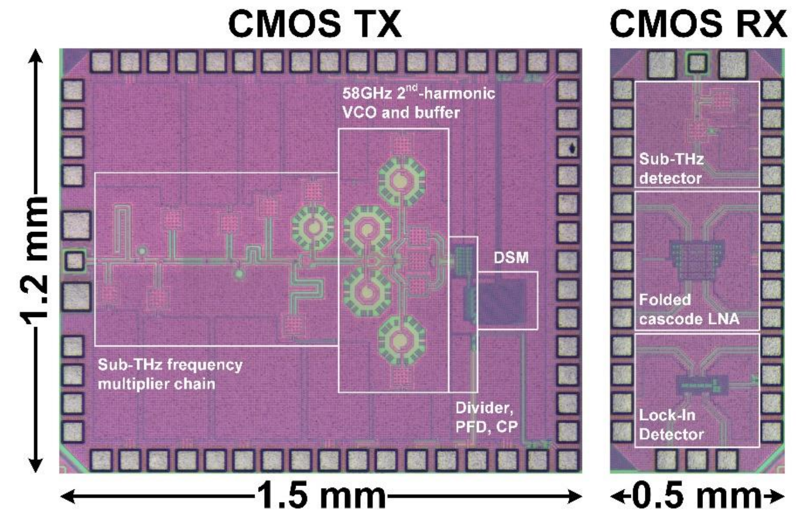
- K_r : Response, [V/Hz]
- V_n : Noise , [V/$\sqrt{\text{Hz}}$]



- K: "closed" → Lock to zero-crossing point

Proof-of-Concept: The 1st CSMC Prototype



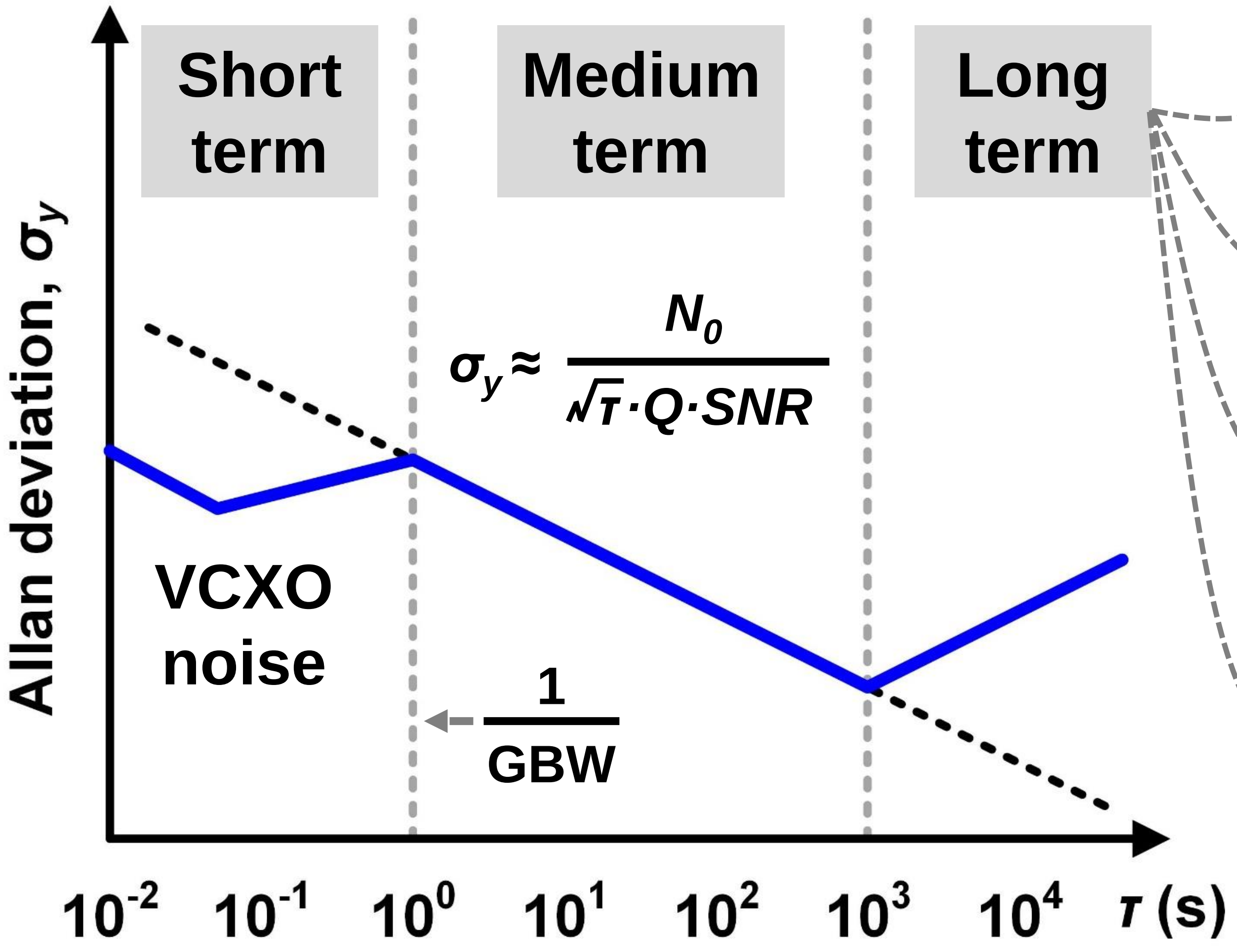


- 231.061GHz line of OCS
- 1st order dispersion curve
- Frequency stability:

  $\sigma_y = 3.8\times10^{-10} @ \tau = 10^3 s$
- 66mW DC power.

[C. Wang, et al., *Nature Electronics*, 2018]

Frequency Stability of Molecular Clock



Drift due to baseline tilting

- **This work: High order locking**

Temperature dependency

Drift due to Magnetic field

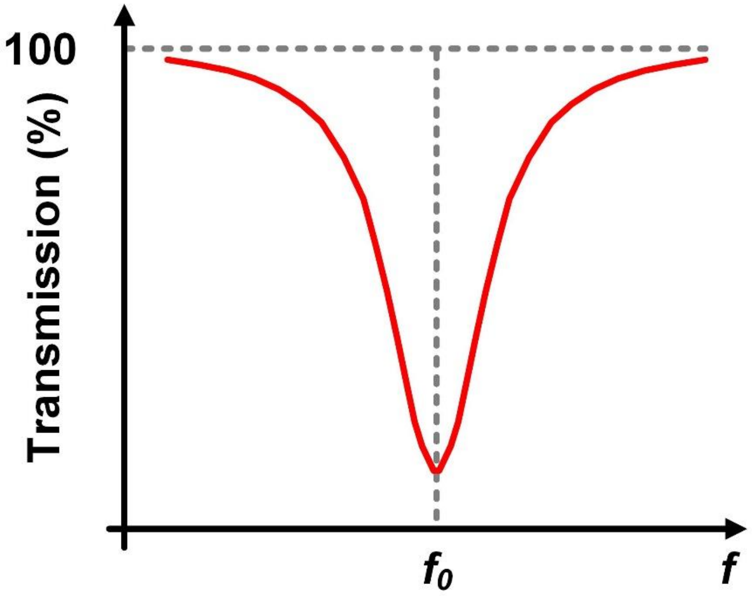
Drift due to Electrical field

Asymmetric Line Profile due to Baseline Tilting

Rotational spectral line

Baseline tilting

Asymmetric line profile



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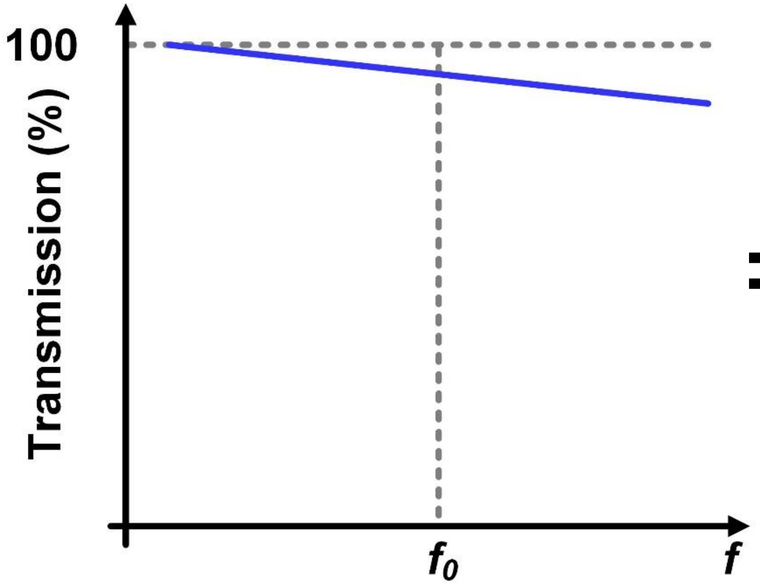

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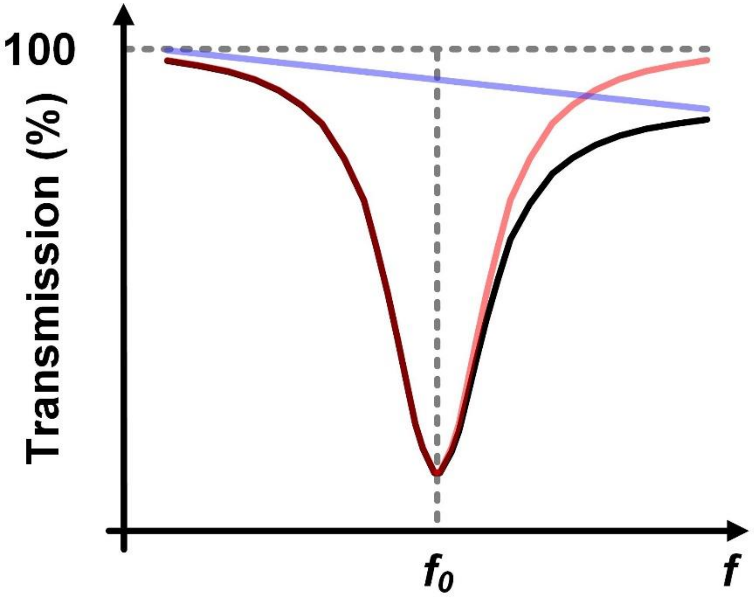


- Symmetric in theory

- THz transceiver response
- Gas cell response

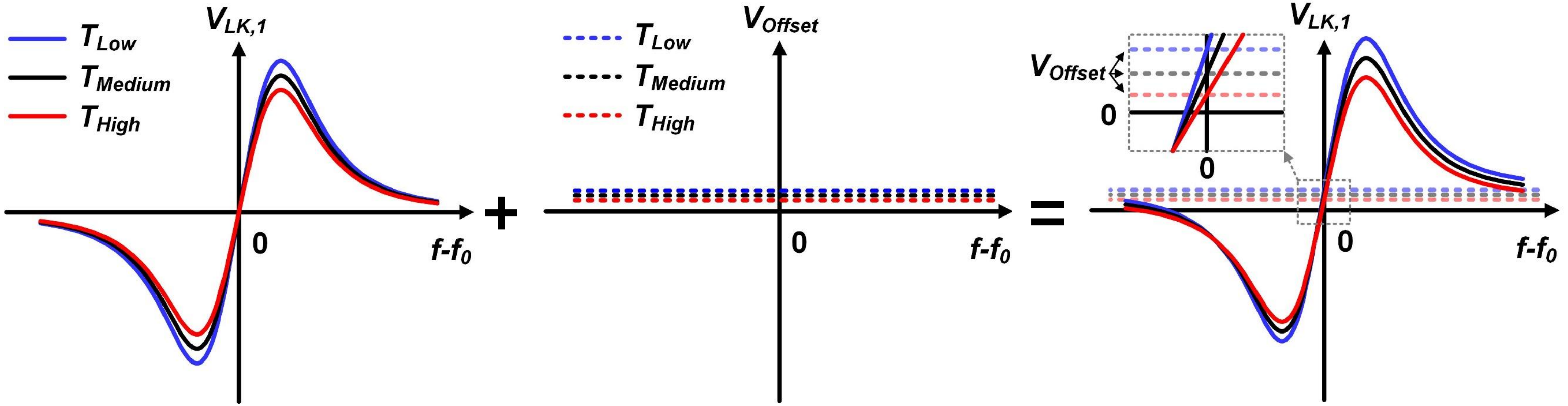
- Measured in reality

1st Order Dispersion Curve w/ Baseline Tilting

1st order dispersion curve

Offset voltage V_{Offset}

Long-term clock drift



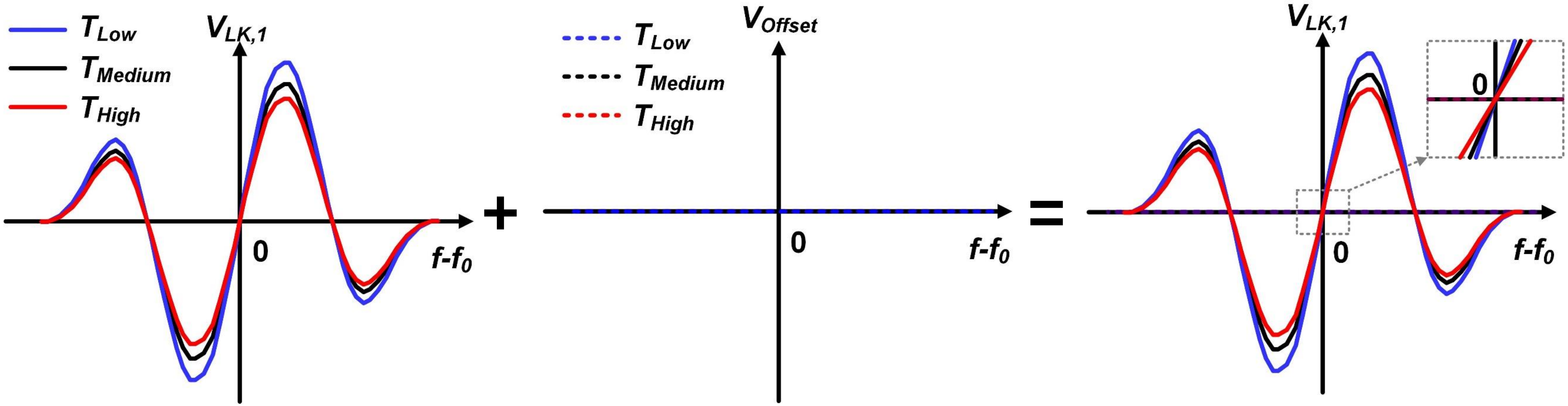
- **Invariant zero-crossing point under PVT**
- **V_{offset} is PVT dependent**
- **How to deal with varying zero-crossing point?**

High Order Dispersion Curve w/ Baseline Tilting

High order dispersion curve

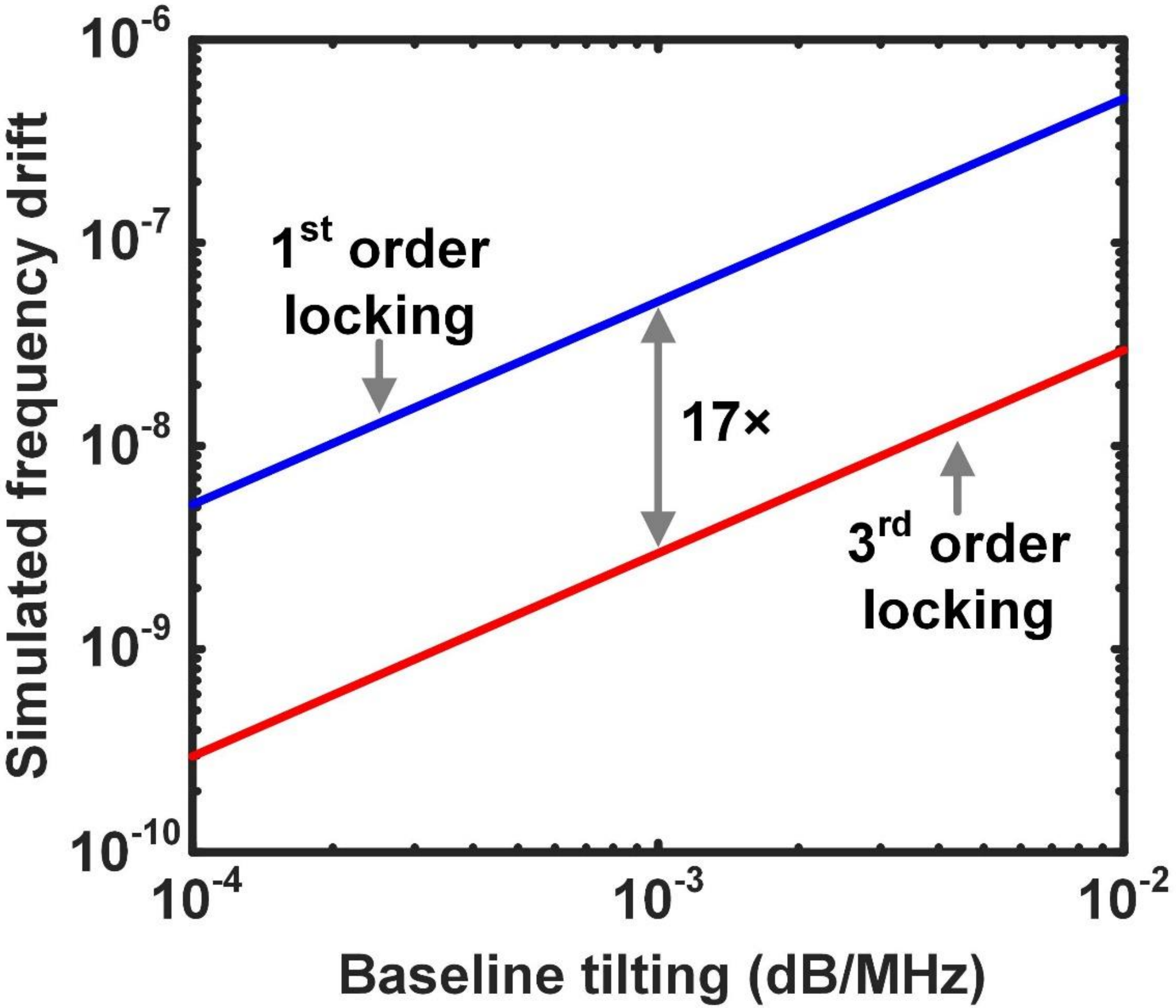
Offset voltage V_{Offset}

Stability enhanced



- **Invariant zero-crossing point under PVT**
- **Eliminated by high order derivative, $V_{offset} \approx 0$**
- **Invariant zero-crossing point under PVT**

Idea: CSMC with High-Order Locking



- Simulation: 0.1dB/GHz baseline tilting → a frequency drift of:
  - 5×10^{-9} for 1st order locking
  - 3×10^{-10} for 3rd order locking
- This work: a chip-scale molecular clock (CSMC) locking to high order dispersion curve

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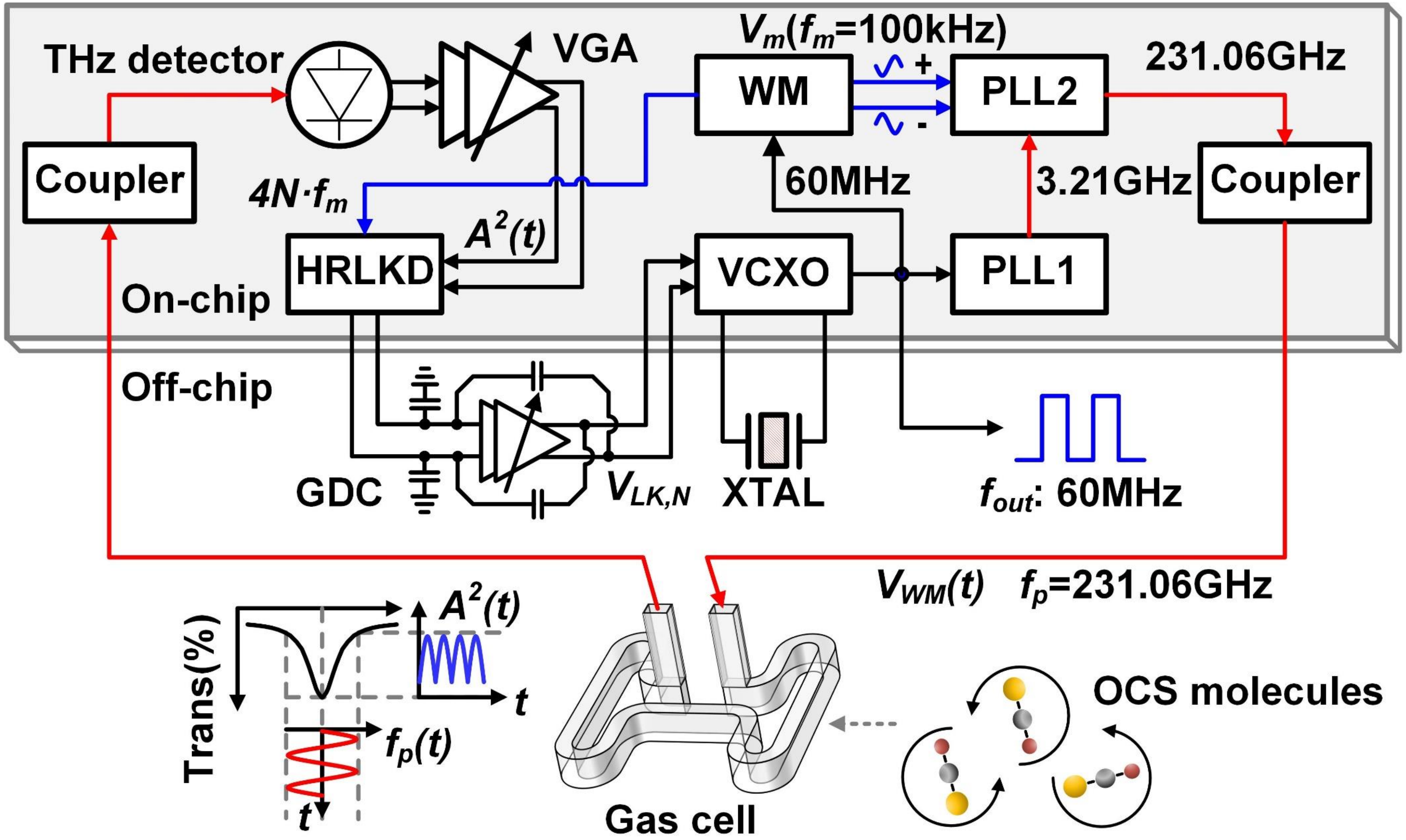
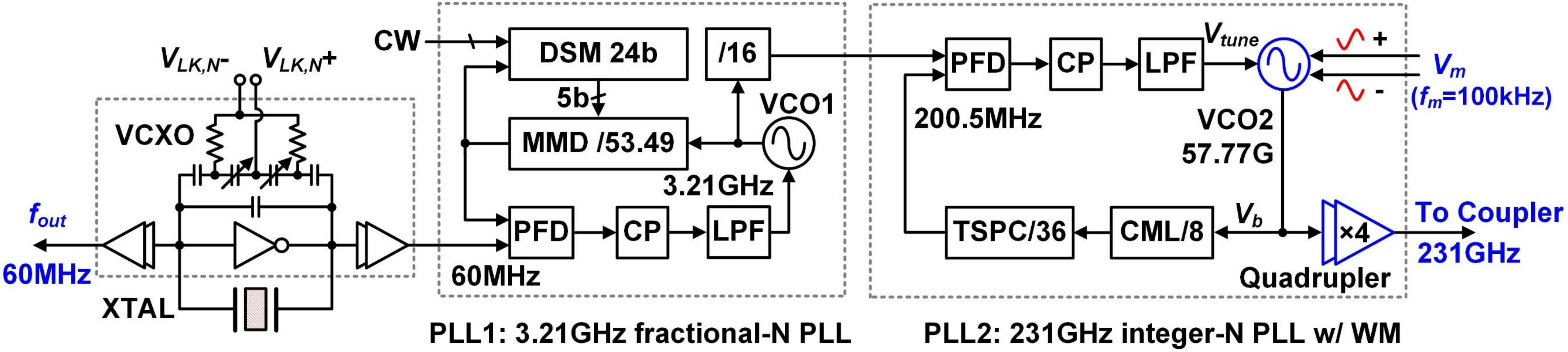
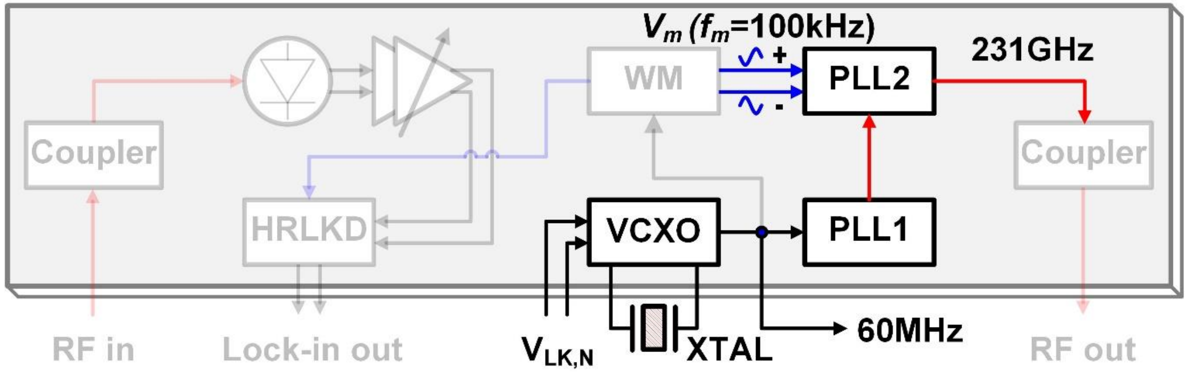
System Architecture



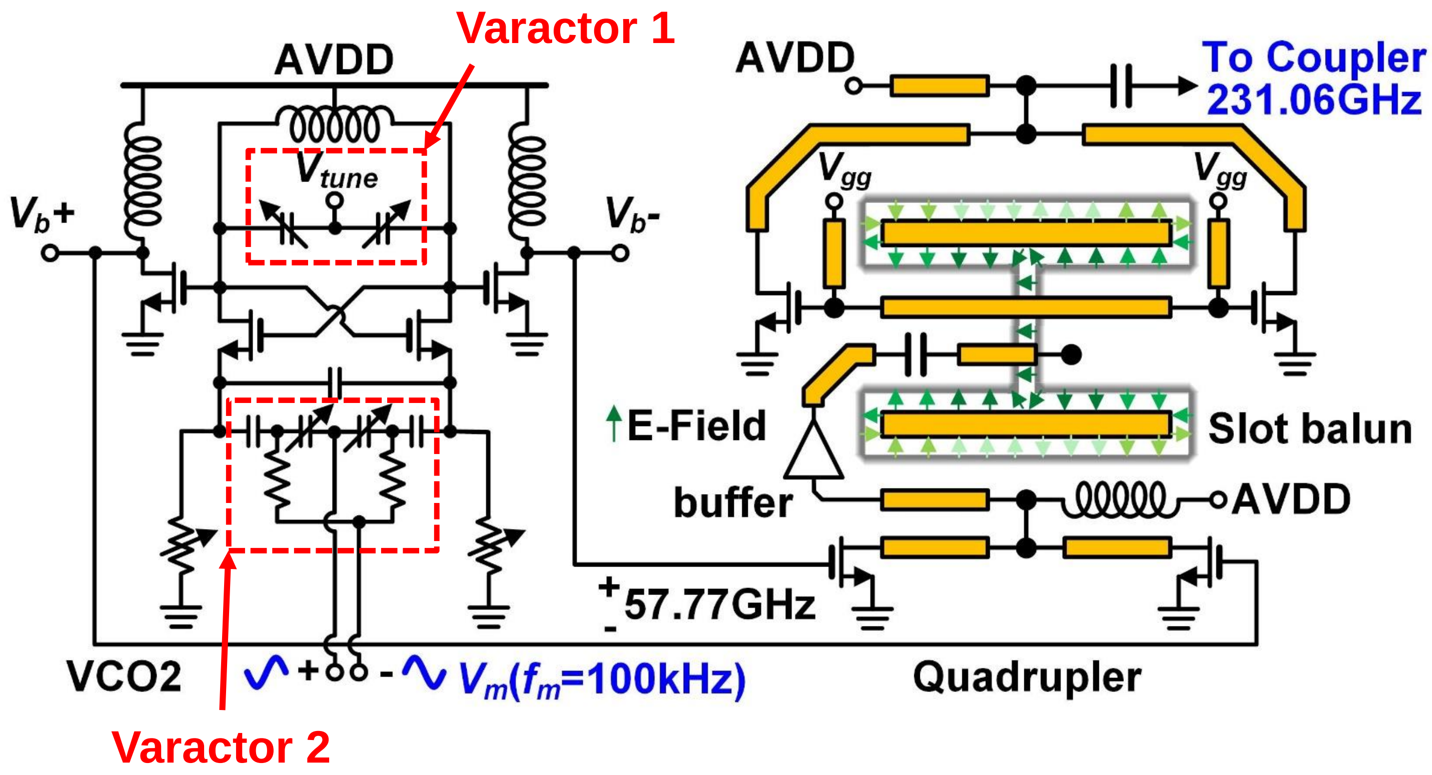
TX: 231GHz Cascaded Two-Stage PLL

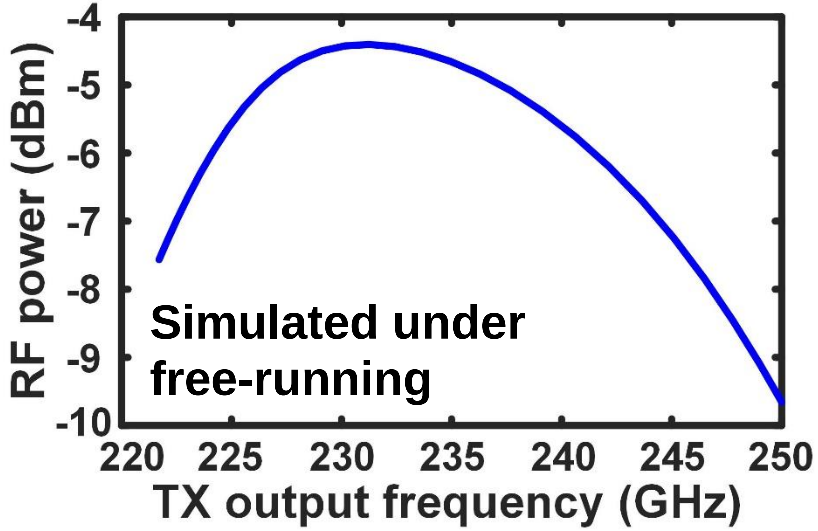


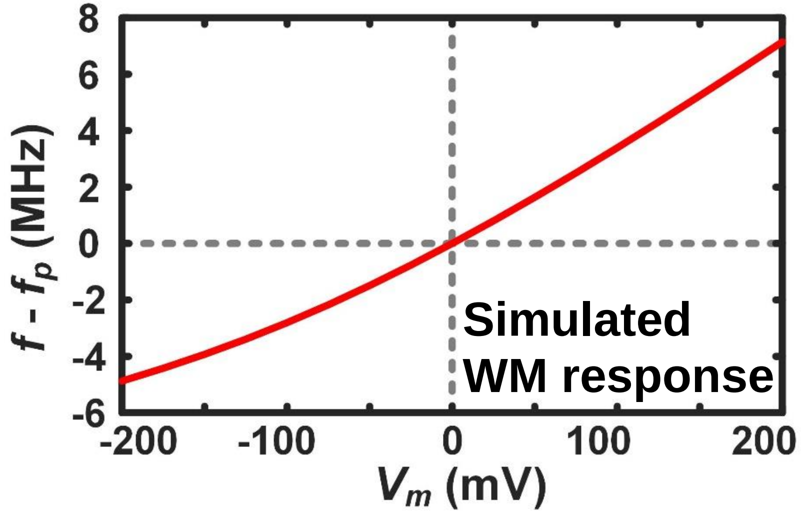


- **Freq. tunability: ~1% of line width f_{FWHM}**
- **27GHz (12%) bandwidth for line coverage**
- **Precise wavelength modulation (WM)**
  - **$\Delta f/f_p \approx 10^{-5}$ ($\Delta f \approx$2.5MHz, f_p=231.06GHz)**

TX PLL2: 57.77GHz VCO and 231GHz Quadrupler

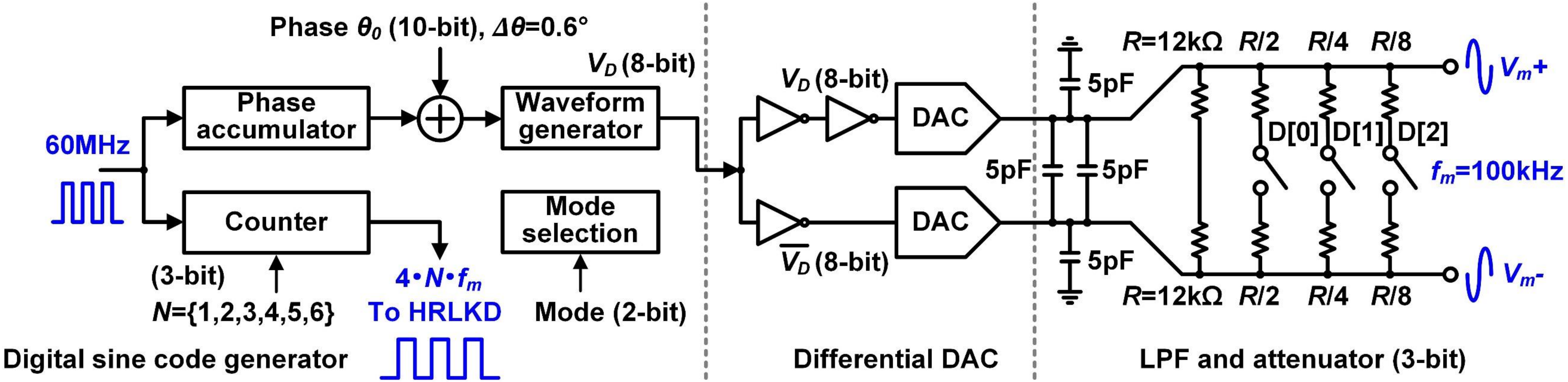


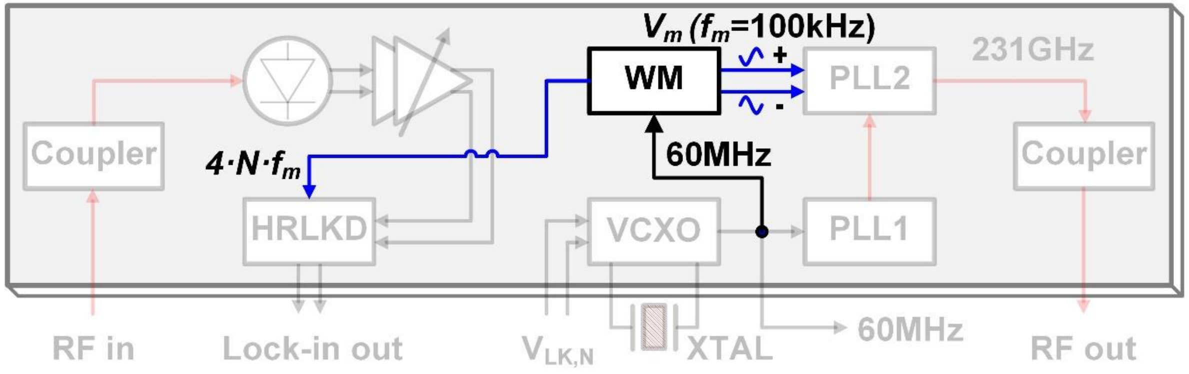


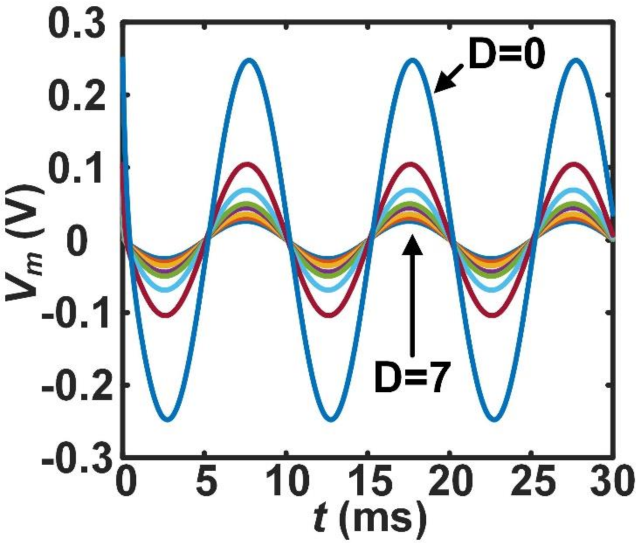


- Varactor 1: highly-sensitive for large PLL bandwidth
- Varactor 2: low sensitivity for wavelength modulation
  - $KVCO_{Varactor\ 1} / KVCO_{Varactor\ 2} \approx 10^3$

TX: Wavelength Modulator (WM)

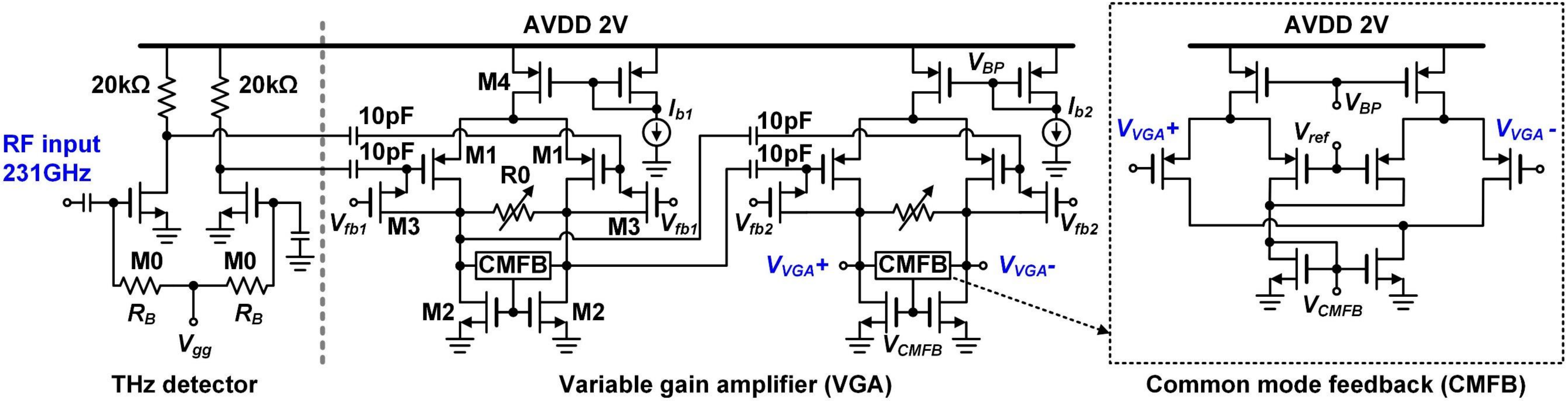


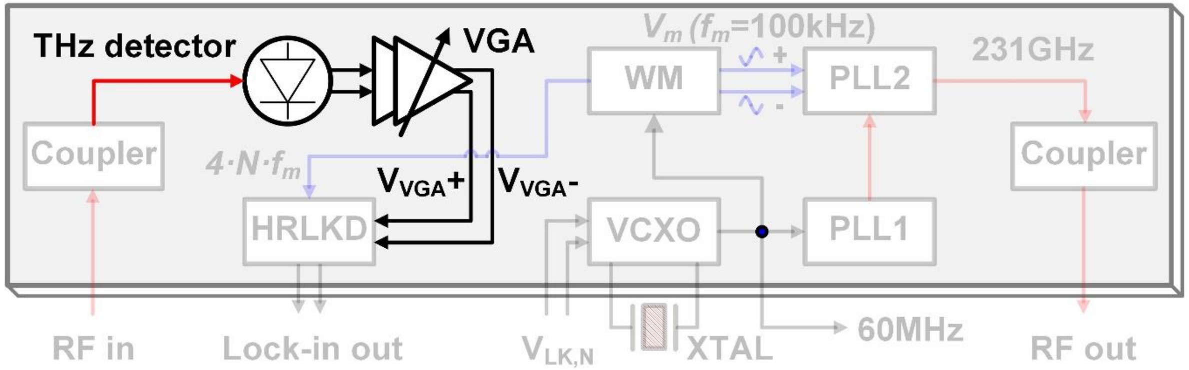




- **100kHz differential output voltage**
- **3-bit Δf control**
- **0.6° phase control**
- **Low distortion: spur < -55dB**

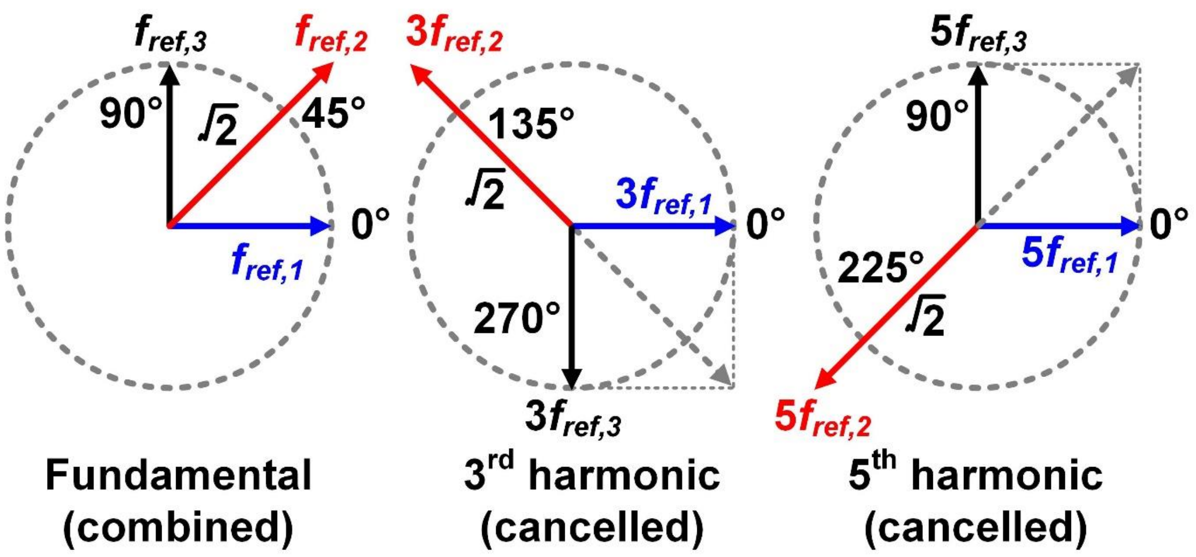
RX: THz Detector and VGA



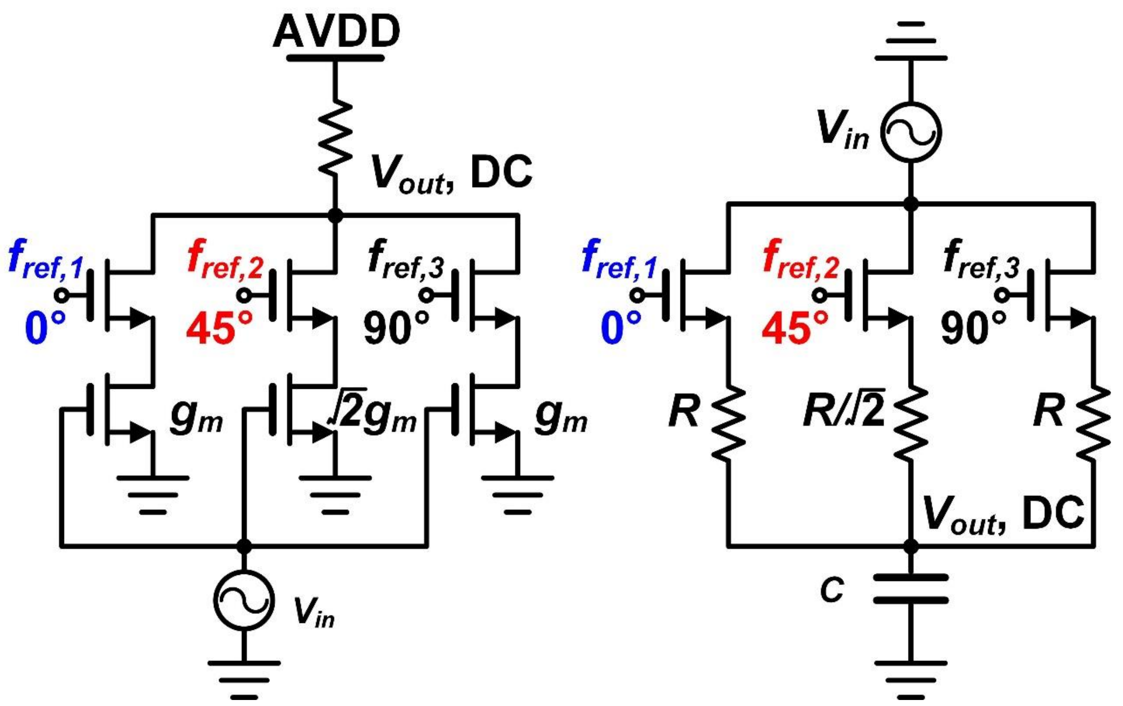


- **Sub-threshold NMOS pair → low noise THz square-law detector**
- **2-stage variable gain amplifier**
  - **65dB max gain / 10-bit control**
  - **AC coupled / monolithic integrated**

RX: Harmonic Rejection Lock-in Detector (HRLKD)

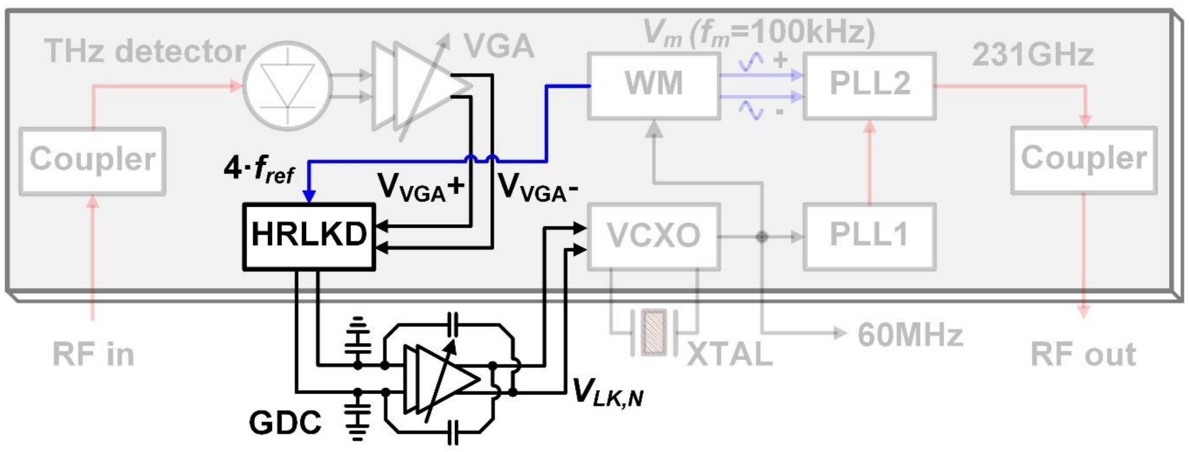


Phasor diagram of harmonic rejection mixer



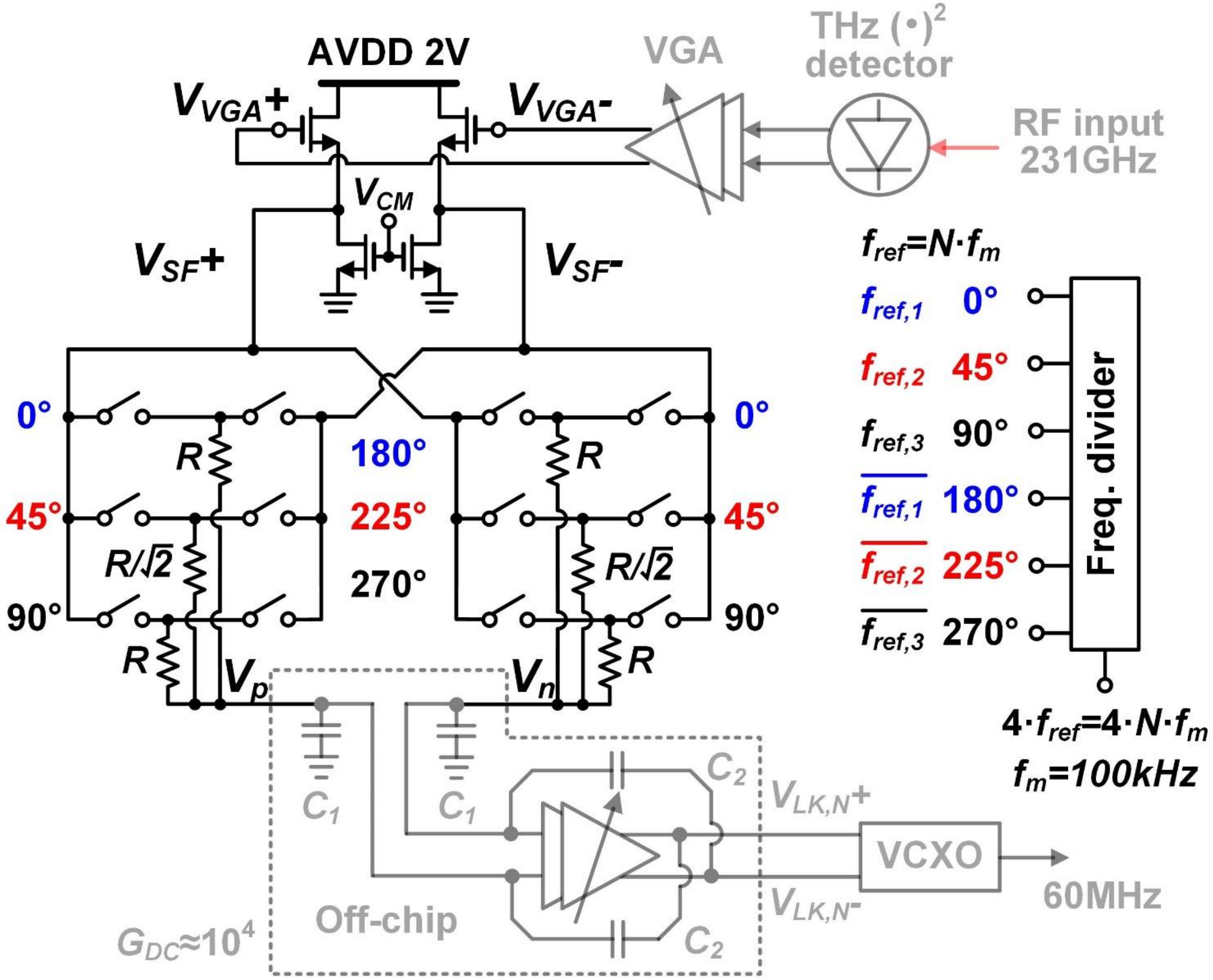
Conventional

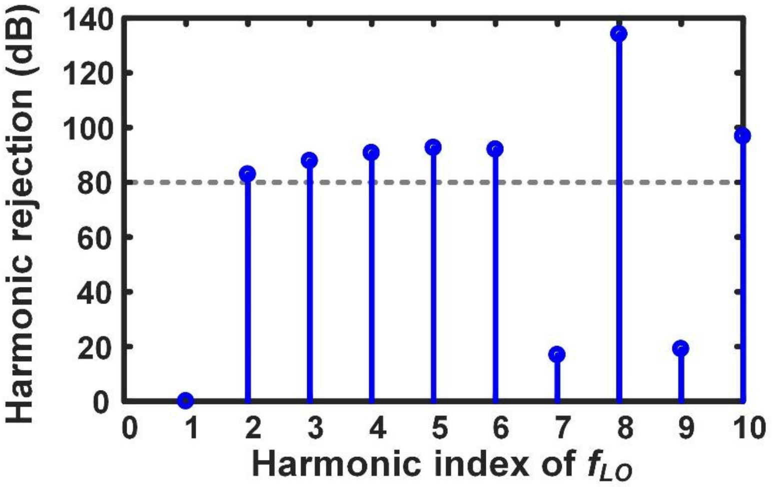
Proposed



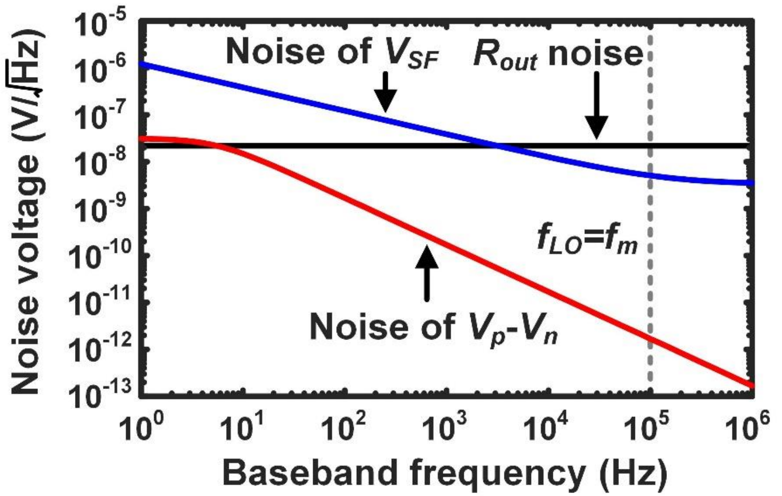
- Convert N^{th} harmonic of f_m to DC
- Harmonic rejection of ref. clock f_{ref} for low interference and noise-folding
- Reduce flicker noise at DC output

RX: Harmonic Rejection Lock-in Detector (HRLKD)



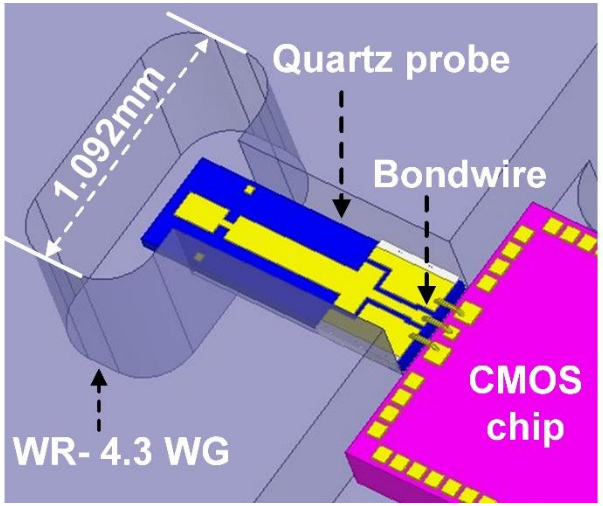


- Harmonic rejection > 80dB



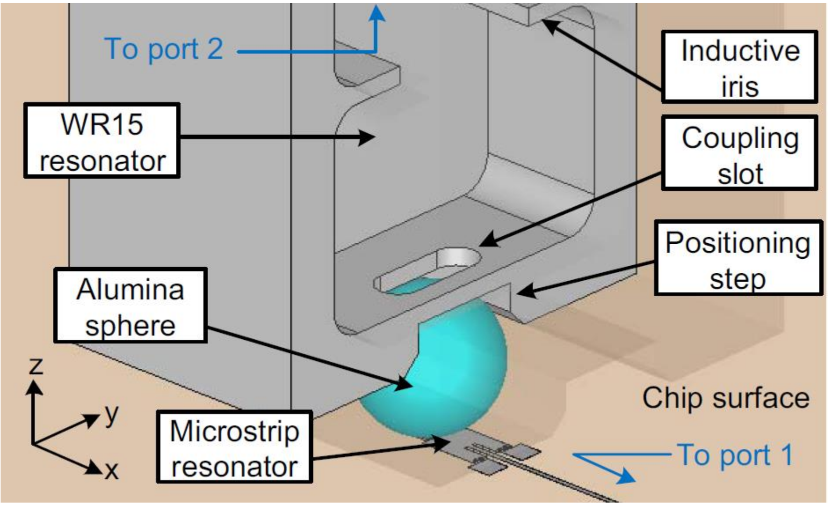
- DC offset V_p-V_n ≈10μV (1μV change → 10^{-10} drift)
- Reduced DC flicker noise

Chip-to-Waveguide Coupler



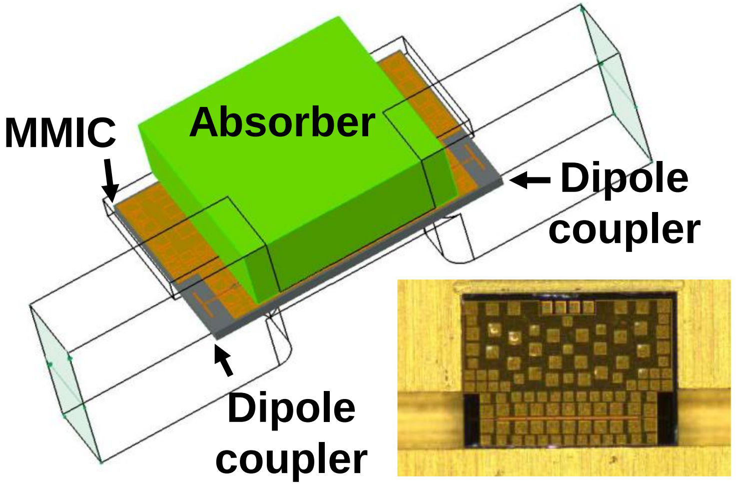
E-plane quartz probe

[C. Wang, et al., *JSSC*, 2018]



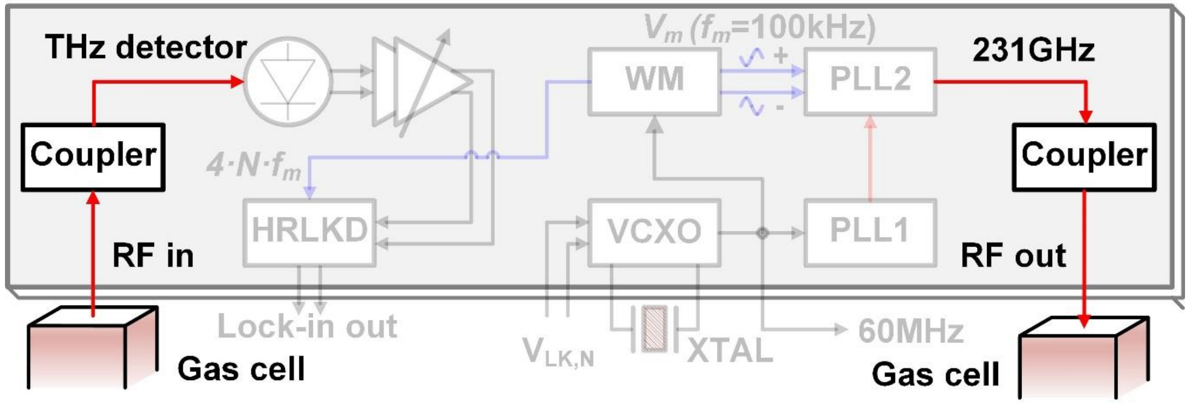
Dielectric resonator

[D. L. Cuenca, et al., *EuMIC*, 2017]



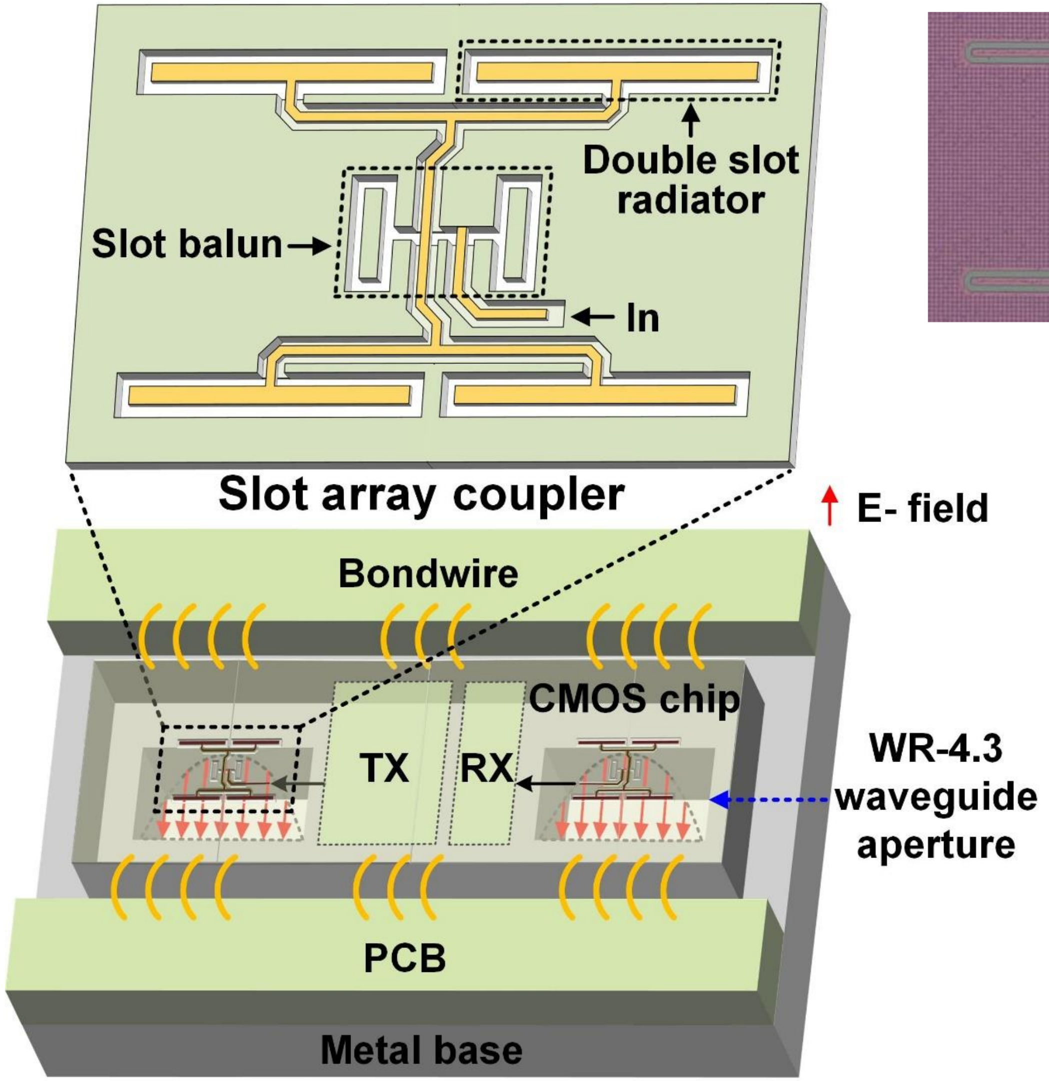
Integrated dipole coupler

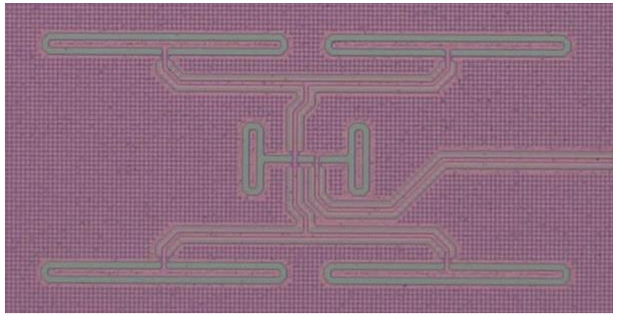
[H. Song, et al., *MWCL*, 2016]



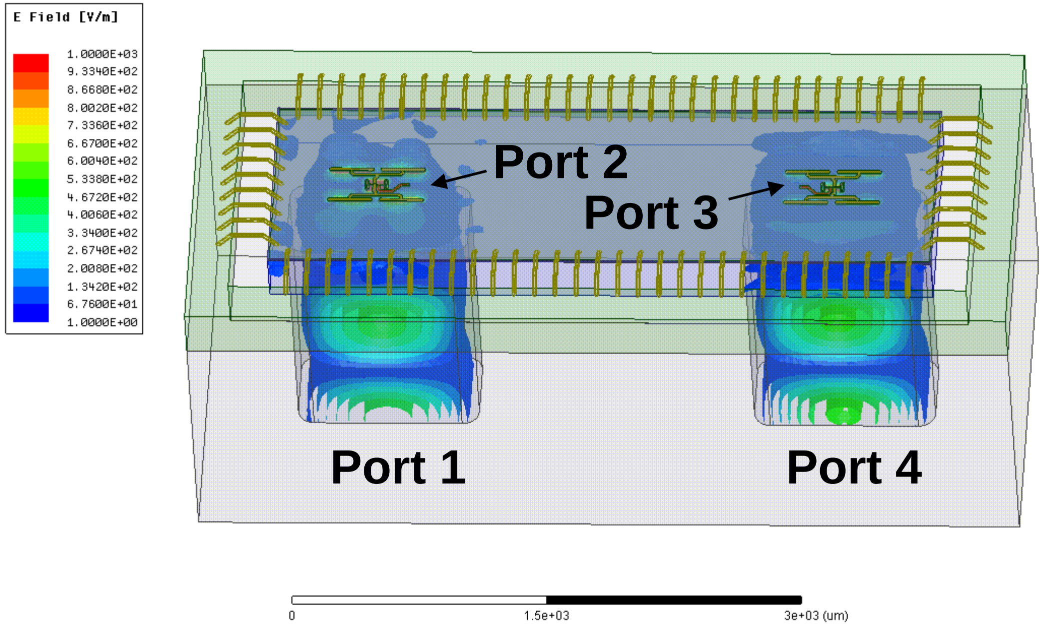
- **Conventional designs**
  - **Costly external components**
  - **Special process/wafer thinning**
  - **Insufficient TRX isolation**

Slot Array Coupler: Architecture



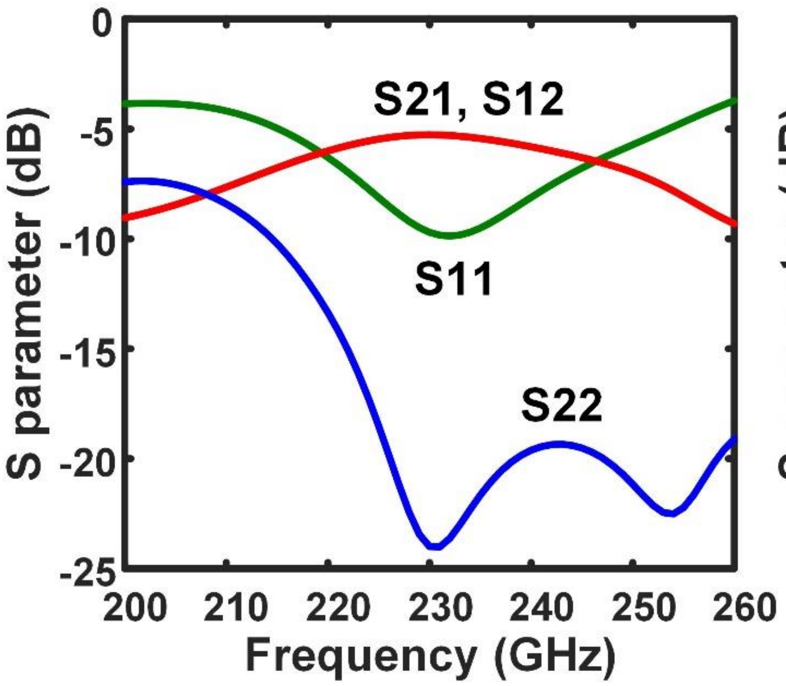


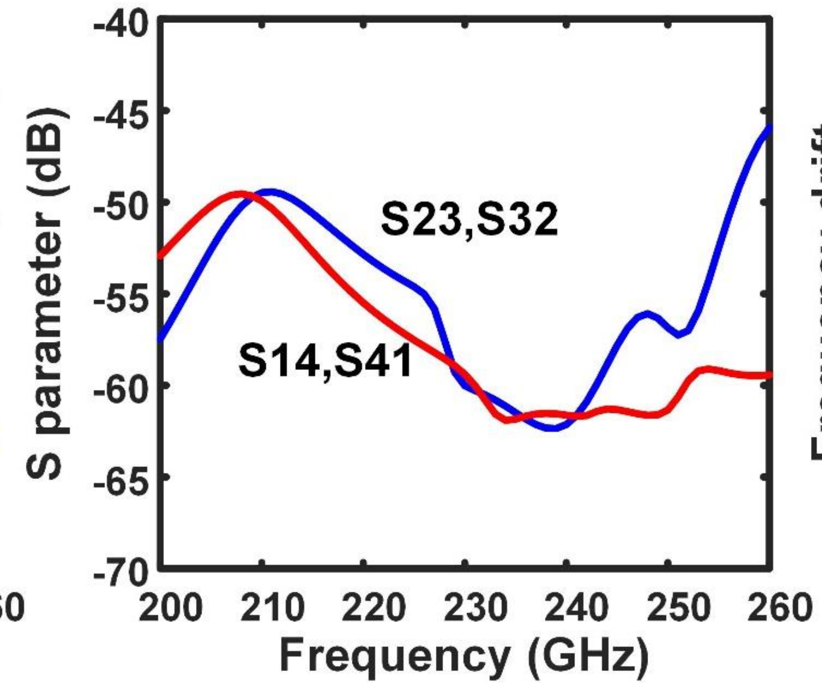
- Radiates downward into waveguide aperture through Si-substrate
- No external components
- No wafer thinning

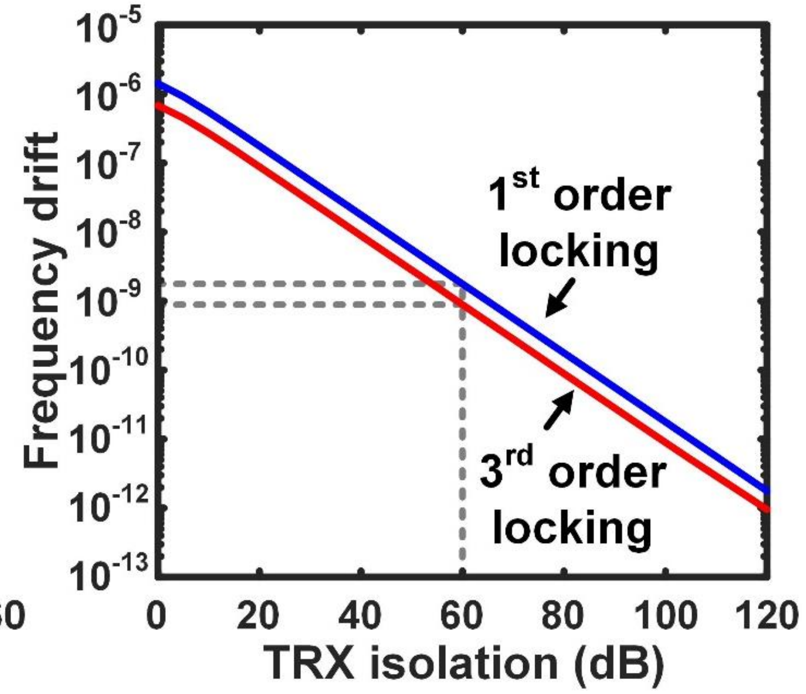


Simulated E-field distribution

Slot Array Coupler: Simulated Results







- **Simulated loss = 5.2dB**
- **BW_{3dB} = 21%**

- **60dB simulated TX/RX isolation**

- **10^{-9} drift by 60dB isolation (removable w/ calibration)**

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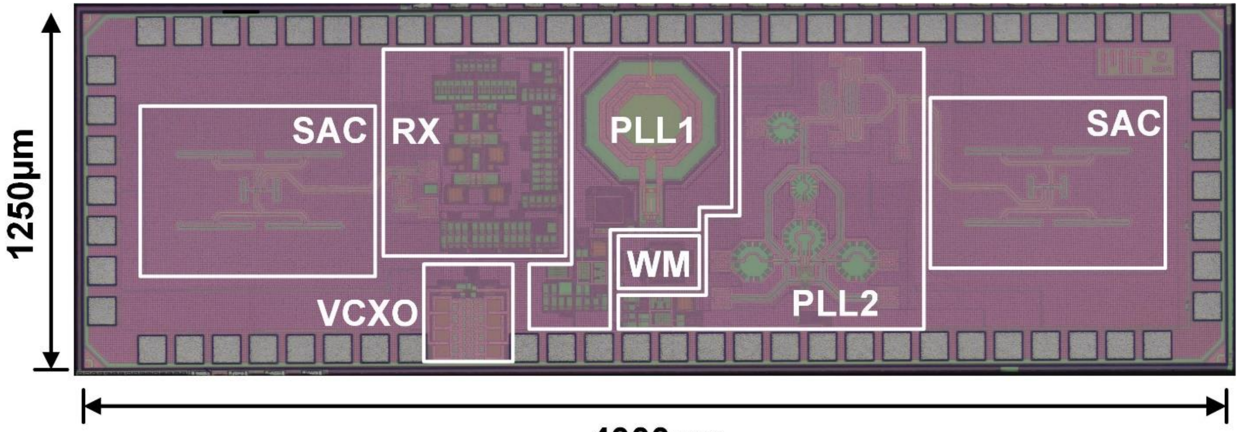
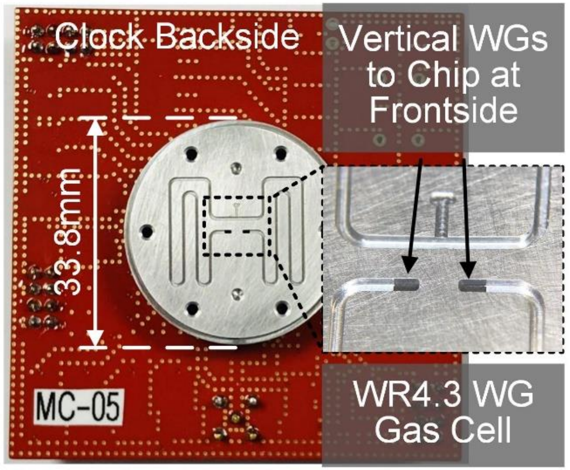
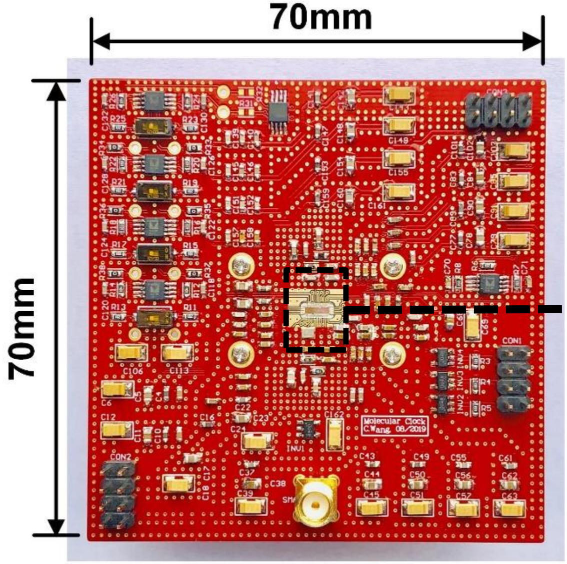
Chip Photo and Packaging



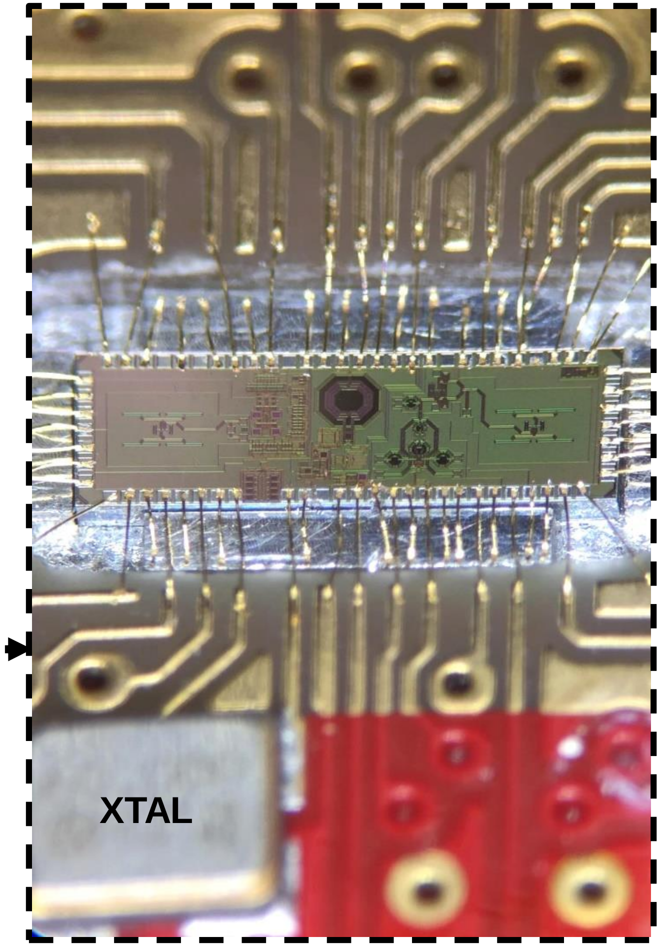
- **TSMC 65nm CMOS process.**



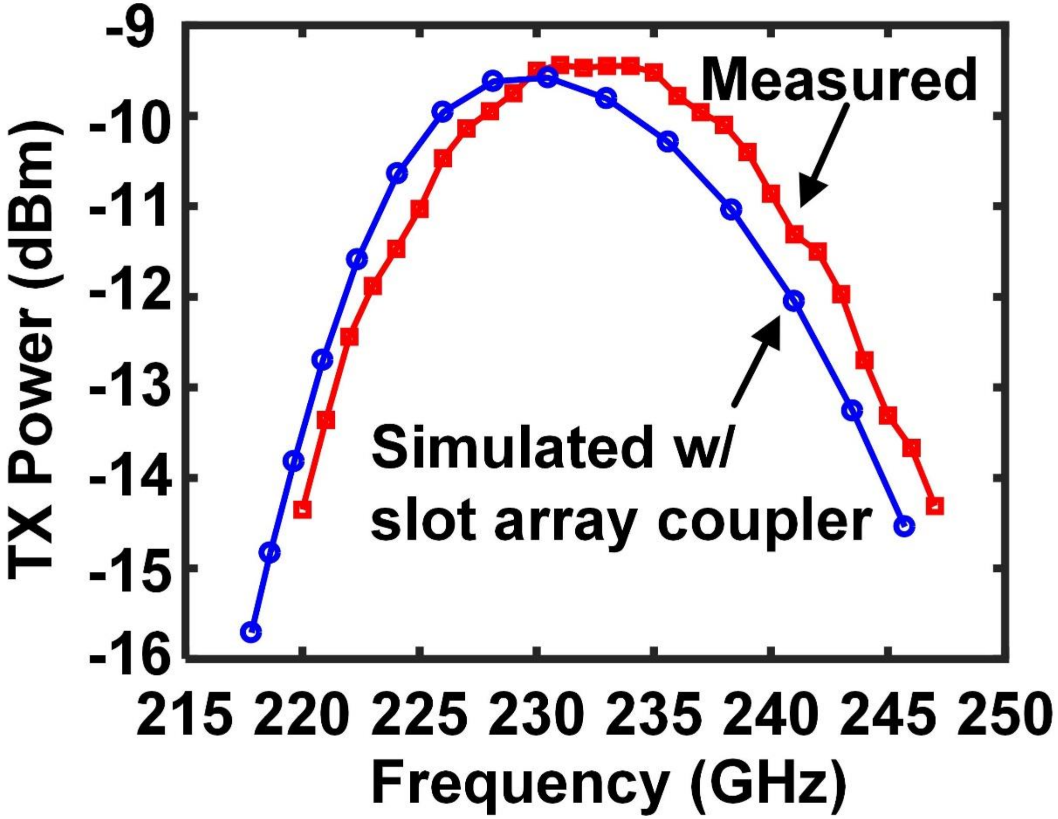
Molecular Cell (Cap Removed)

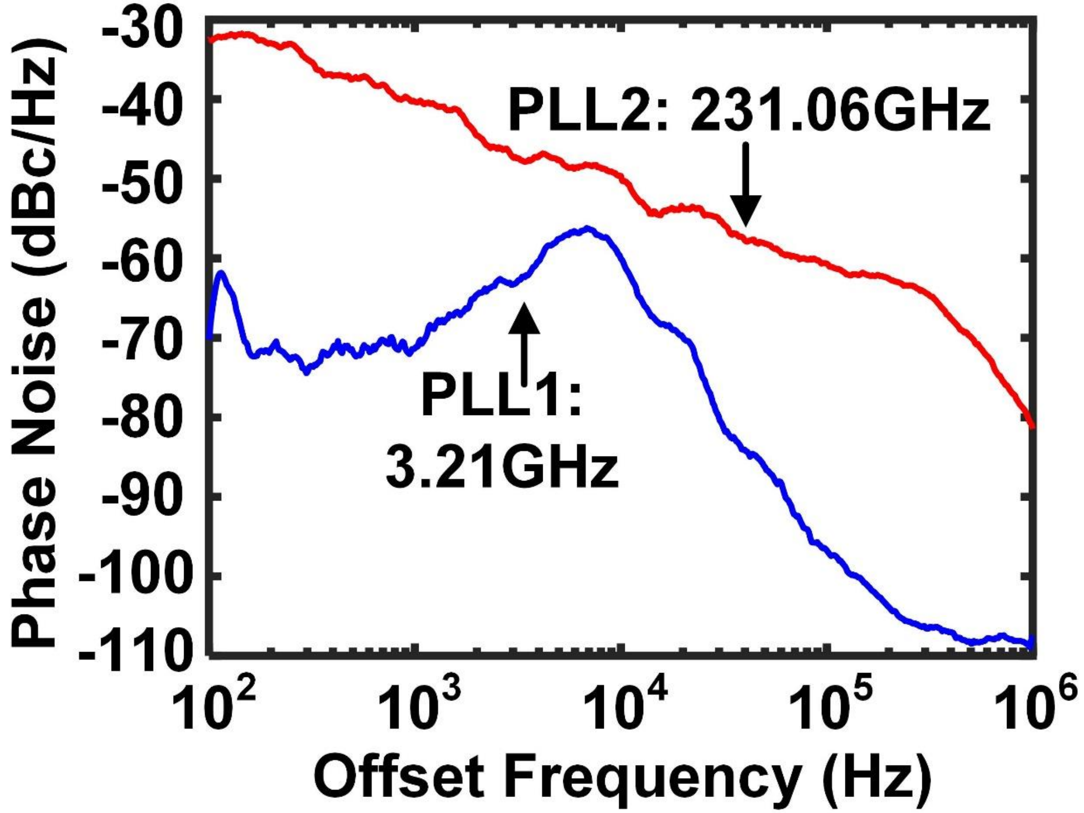


CMOS chip on PCB



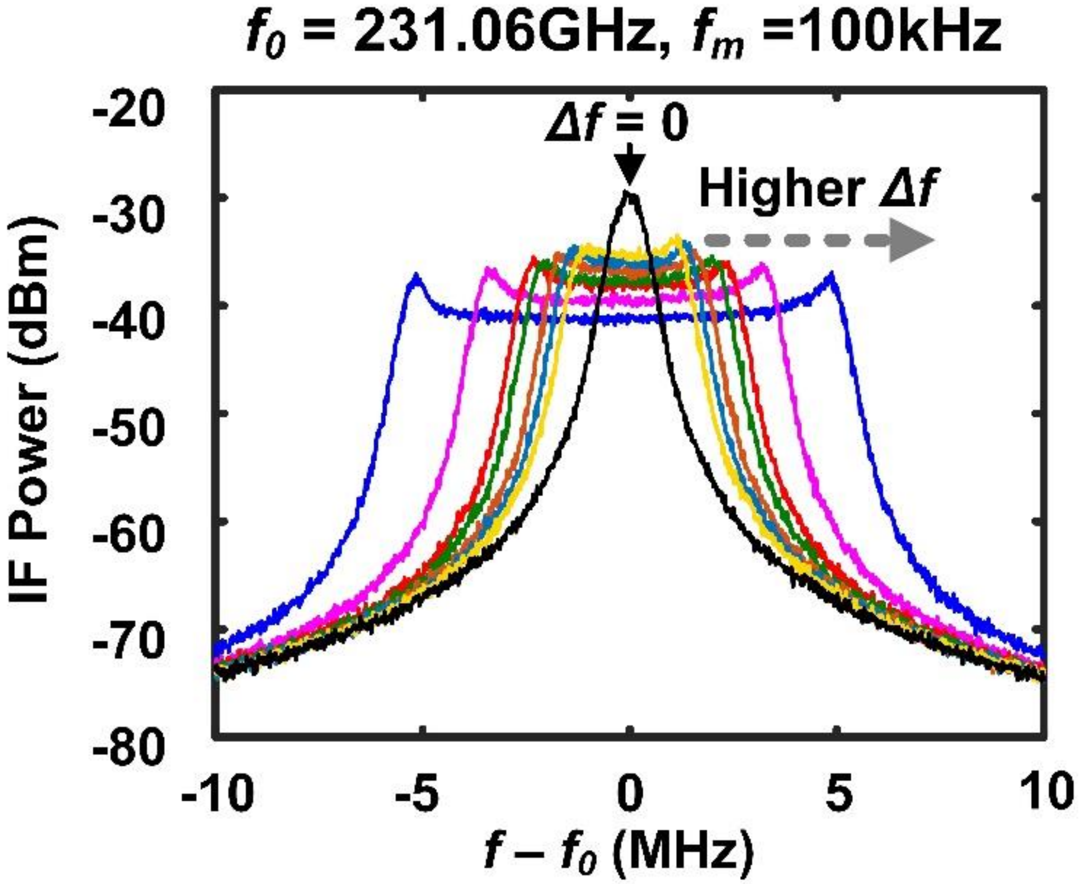
Measured RF Power and Phase Noise of TX

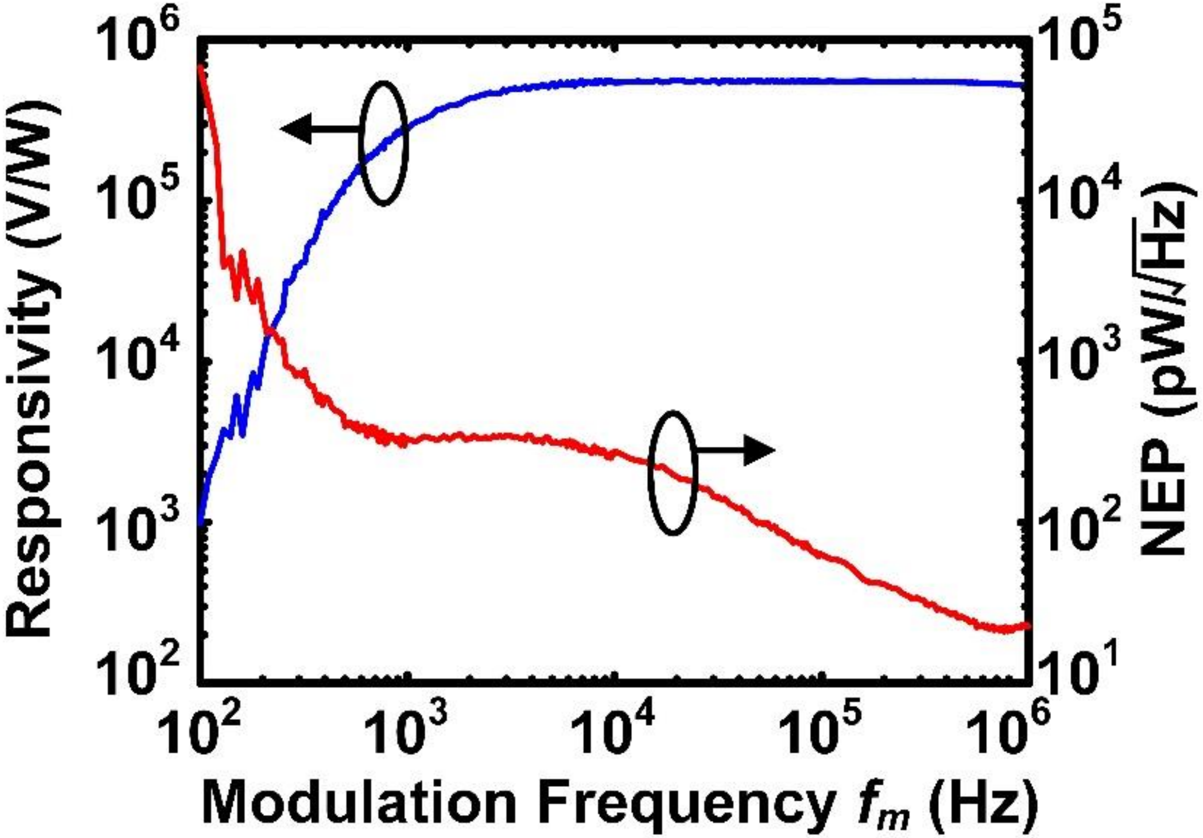




- P_{RF} = -9.4dBm w/ slot array coupler
- PLL bandwidth: 27GHz (12%)
- Phase noise : -81.5dBc/Hz@1MHz
- PM-to-AM noise → SNR_{PN}= 84dB

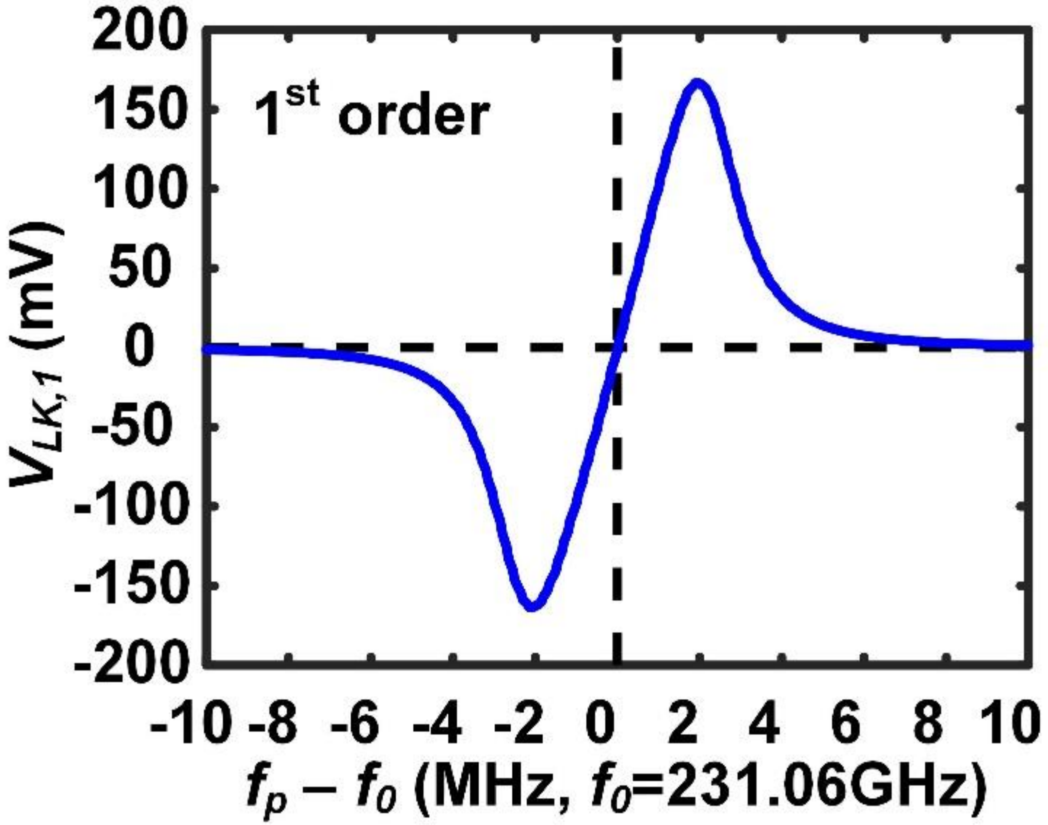
Measured WMS Spectrum and RX Performance

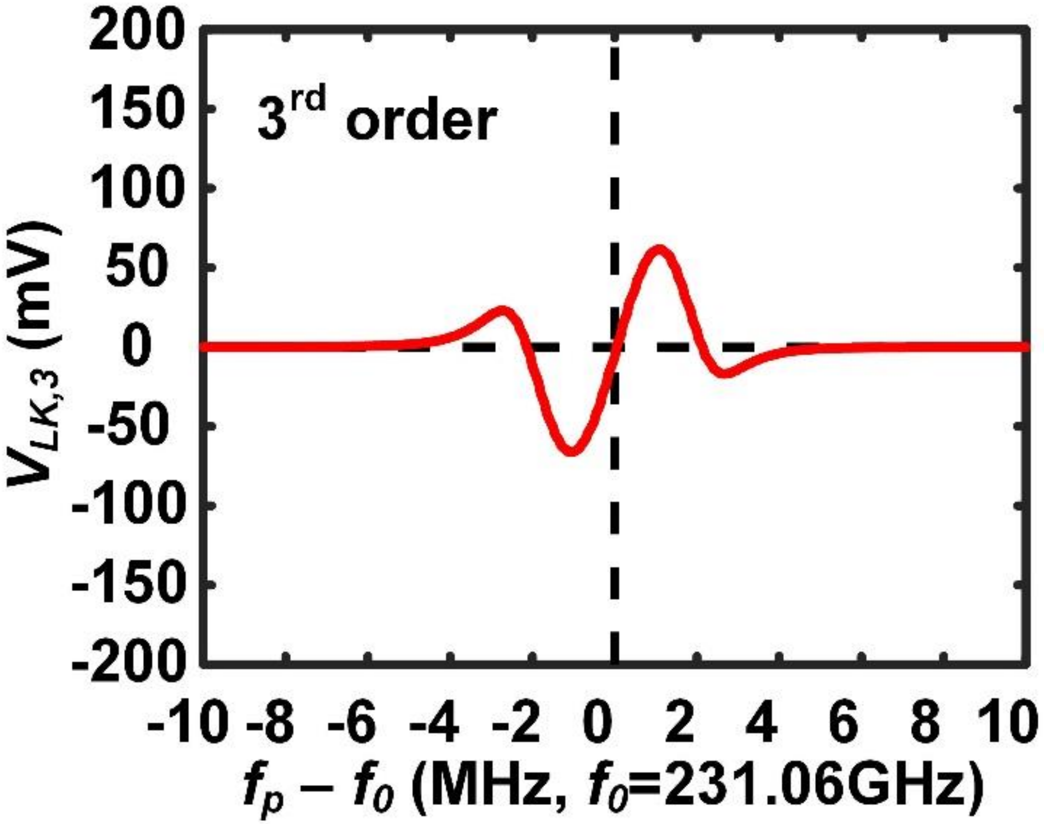




- Spectrum of TX probing signal with wavelength modulation
- NEP of RX w/ slot array coupler: 62.8 pW/$\sqrt{Hz}$ at f_m=100kHz

Measured Dispersion Curves and Allan Deviation

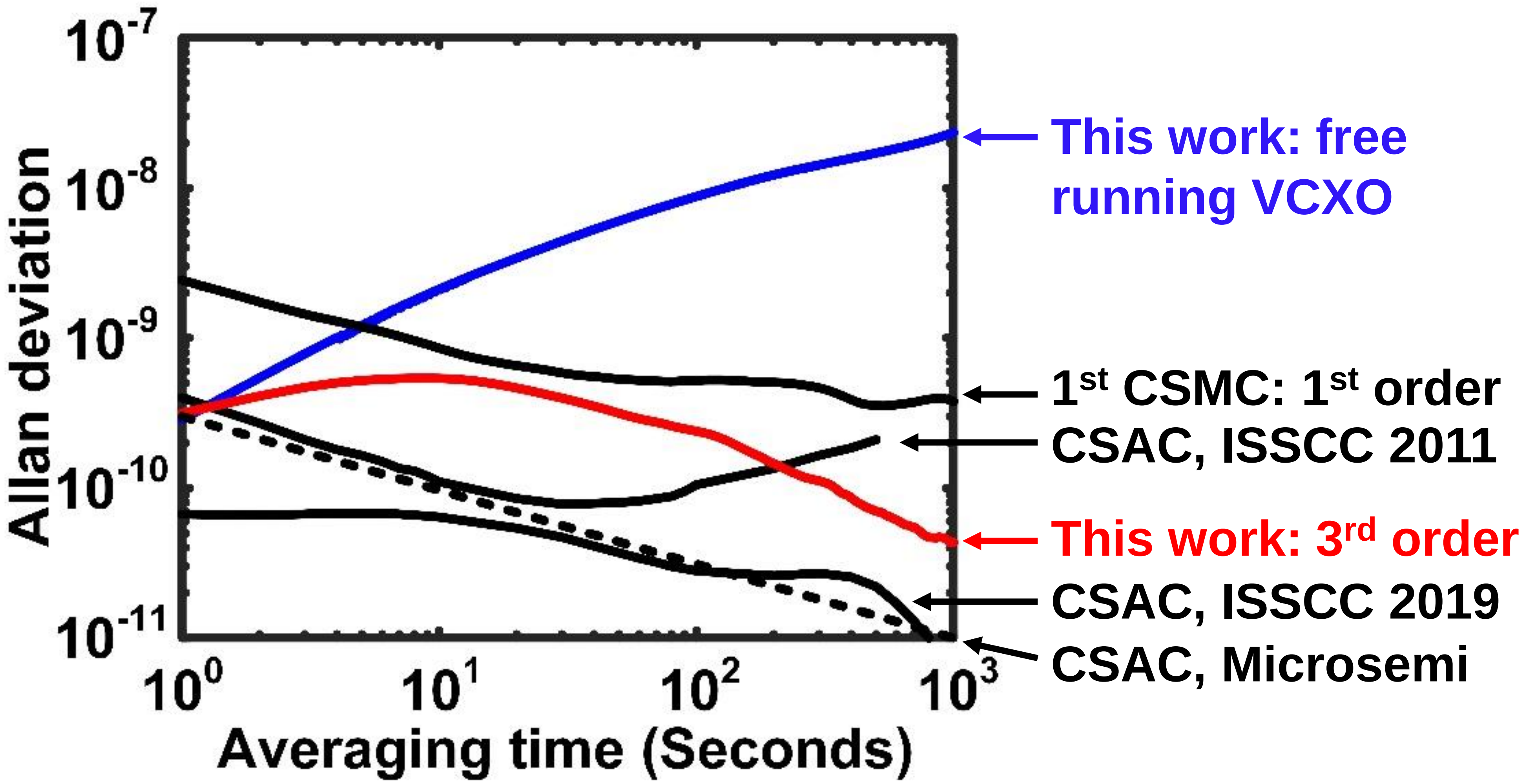




- **1st order curve: SNR = 84dB**
- **V_{Offset} = 1.1mV**

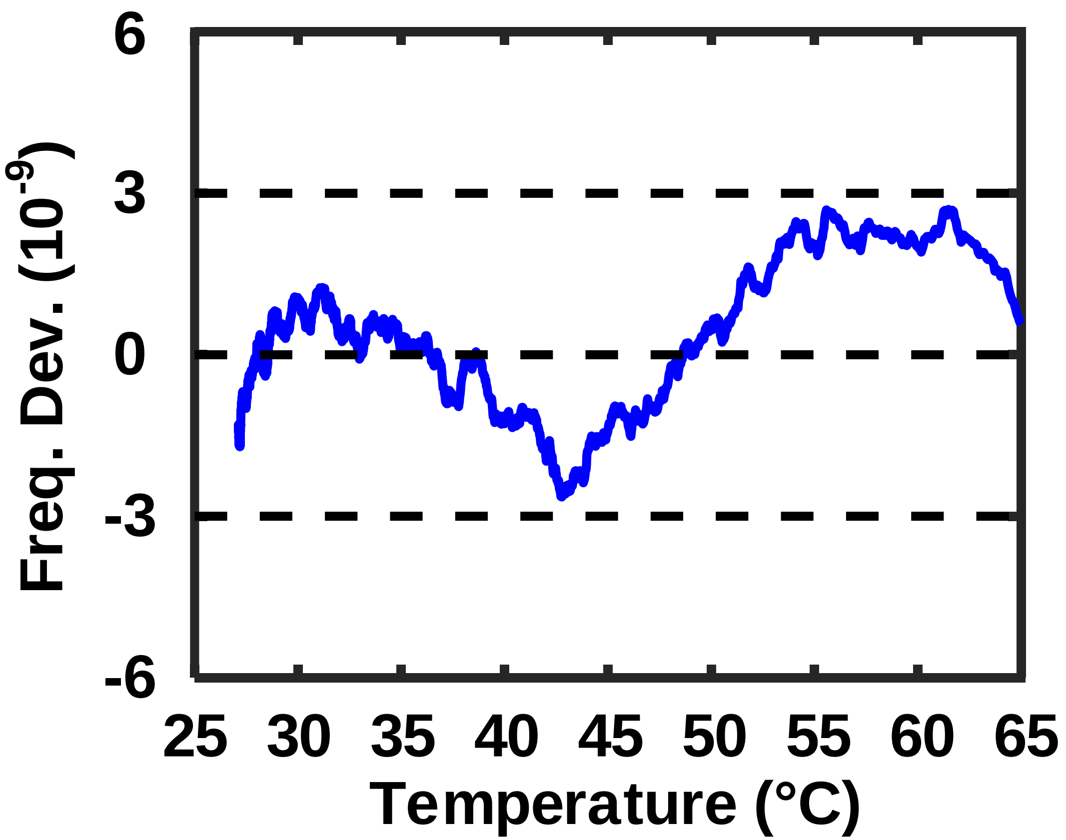
- **3rd order curve: SNR = 66dB**
- **V_{Offset} = 4.3µV (256× smaller)**

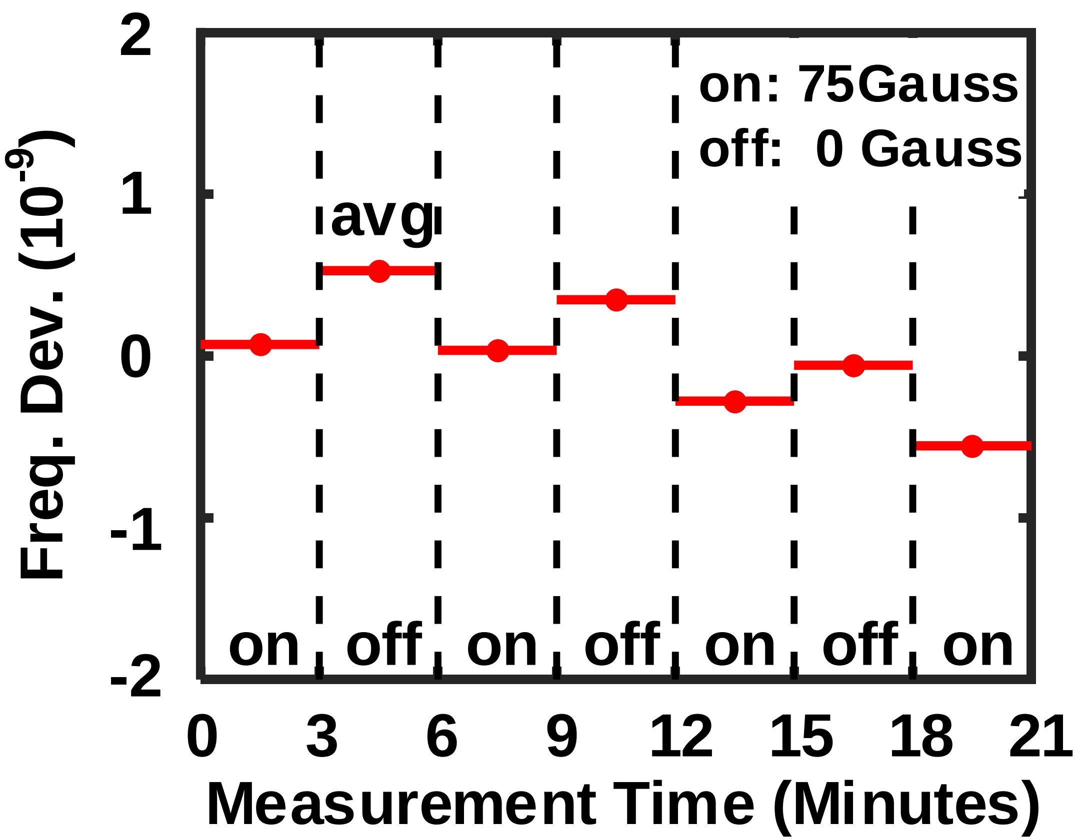
Measured Allan Deviation by 3rd Order Locking



- **Allan deviation: σ_y = 3.2×10^{-10}@ τ =1s, 4.3×10^{-11}@ τ=10^{3}s**

Measured Temperature and Magnetic Sensitivity





- Drift < ± 3×10^{-9} in 27~65 ºC w/ 2nd order temperature compensation
- Drift < ± 2.9×10^{-12}/Gauss w/o magnetic shield in CSAC

Outline

- Background
- High-order locking for long-term stabilization
- Architecture and circuit design
- Measurement results
- **Conclusions**

Performance Comparison Table

Parameters	SiTime [1]	Microsemi [3]	ISSCC2019 [4]	VLSI2018 [5]	This work
Mechanism	OCXO	^{133}Cs CSAC	^{133}Cs CSAC	$^{16}O^{12}C^{32}S$ MC	$^{16}O^{12}C^{32}S$ MC
Cost	Medium	High	High	Low	Low
Freq. (GHz)	0.06	4.6	4.6	231.061	231.061
Harmonics	N/A	1st order	1st order	1st order	3rd order
σ_y (τ =10^0s)	3.0×10^{-11}	3.0×10^{-10}	8.4×10^{-11}	2.4×10^{-9}	3.2×10^{-10}
σ_y (τ =10^3s)	4.0×10^{-11}	1.0×10^{-11}	0.8×10^{-11}	3.8×10^{-10}	4.3×10^{-11}
Temp. Drift [a]	$\pm5.0\times10^{-9}$	$\pm5.0\times10^{-10}$	$<\pm1.0\times10^{-9}$	N/A	$\pm3.0\times10^{-9}$
Mag. Sens. [b]	N/A	$\pm9.0\times10^{-11}$	N/A	N/A	$\pm2.9\times10^{-12}$
$T_{start\text{-}up}$ (s)	120	180	N/A	<1	<1
P_{DC} (mW)	600	120	60	66	70

a. Measured temp. range: [1]: -20~70°C; [2], [3]: -10~70°C; This Work: 27~65°C;

b. Unit: $Gauss^{-1}$.

[1] SiTime, *SiT5711*, 2019;
[2] D. Ruffieux, *ISSCC*, 2011;
[3] Microsemi, *SA.45s*, 2019;
[4] H. Zhang, *ISSCC*, 2019;
[5] C. Wang, *VLSI*, 2018.

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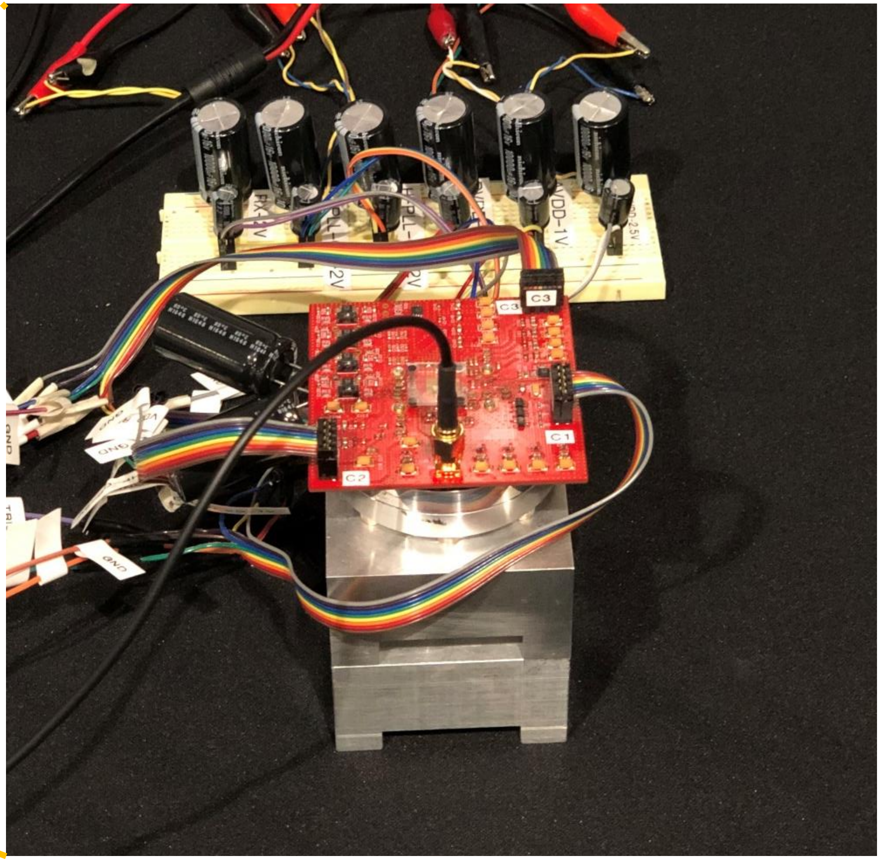
Demo Session 1



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