A 3.4–4.6GHz In-Band Full-Duplex Front-End in CMOS Using a Bi-Directional Frequency Converter

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***Abstract*— Magnetic-free circulators using phase nonreciprocity of spatial-temporal modulated structures have enabled in-band full-duplex systems on CMOS chips. In this paper, we present an alternative and simple integrated circuit scheme based on a bi-directional frequency converter, which not only realizes nonreciprocal signal flow for in-band full-duplex systems but also improves the isolation performance by completely eliminating any chip-level TX-to-RX coupling. These functions are implemented through a direction/frequency-independent single-sideband down-conversion process, which well splits the on-chip TX and RX frequencies. That principle also leads to extension of isolation bandwidth and integrated receiver down-mixing function. Implemented in a 65-nm bulk CMOS technology, a circuit prototype operates from 3.4 to 4.6 GHz (30% fractional bandwidth) and achieves >25.5-dB measured TX-RX isolation. The measured TX-ANT and ANT-RX insertion loss are 3.0 and 3.2 dB, respectively, and the TX-ANT and ANT-RX IIP3 are 29.5 and 27.6 dBm, respectively. This full-duplex front-end component occupies 0.27mm^2 area and has 48 mW of power consumption.**

***Keywords*— in-band full-duplex, magnetic-free circulator, nonreciprocal, bi-directional frequency converter (BDFC), isolation, coupling, wideband.**

I. Introduction

The ever-increasing demands of wireless communication capacity and sensing capability call for RF systems with more efficient utilization of the congested electromagnetic spectrum. Compared with half-duplex modes, such as time-division duplex and frequency-division duplex, the in-band full-duplex mode potentially doubles the spectral capacity and simplifies transmission protocols [1]. Nonreciprocal electronic devices, such as isolator, gyrator, and circulator, are critical for full-duplex operations in wireless data transmission, radar detection, and quantum signal processing [2]. In the example shown in Fig. 1(a), the circulator enables a full-duplex system with one shared antenna.

Conventional ferrite circulators based on Faraday rotation are bulky and cannot be integrated on a chip. Recently, magnetic-free circulators become attractive due to their compact size and compatibility with CMOS integrated circuit technologies [2]–[7]. Using time-variant devices, typically realized with clock-modulated switches in a N-path filter [3], [4], such a component applies nonreciprocal phases to various signals at the same frequency, and then through a set of delay

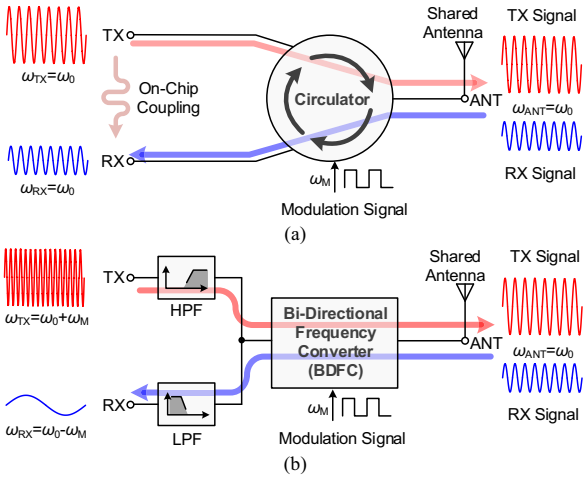

Fig. 1. Propagation and frequency allocation of TX, RX and ANT signals in (a) circulator-based full-duplex and (b) BDFC-based full-duplex systems.

lines, it creates constructive addition of the desired signal at a certain port and cancellation of other undesired signals. If the antenna impedance mismatch is addressed by the impedance tuner, another factor that limits the isolation performance of CMOS circulator relates to the identical transmitter (TX) and receiver (RX) frequencies, and hence the inevitable TX-to-RX coupling through the silicon substrate (especially in bulk CMOS processes with low substrate resistivity), power lines, inter-inductor magnetic crosstalk, etc. (Fig. 1(a)). Meanwhile, the isolation of these circulators relies on the aforementioned signal cancellation among separated transmission-line paths with desired phase shifting, which is narrowband in nature and is susceptible to non-ideal clocking and amplitude/phase mismatches among those paths.

In this paper, we present a fully-integrated nonreciprocal frond-end based on a bi-directional frequency converter (BDFC) to replace the circulator in full-duplex system, while addressing the above problems. As shown in Fig. 1(b), the two-port BDFC is also driven by a modulation signal ω_M. Its one port is connected to the shared antenna (ANT), while the other port coexists both the TX and RX signals. The key difference from previous circulators is, although the TX and RX frequencies are identical at the antenna interface ($\omega_{ANT}=\omega_0$), they are far split by $2\omega_M$ inside the chip. This is realized through a *direction-independent downconversion* of

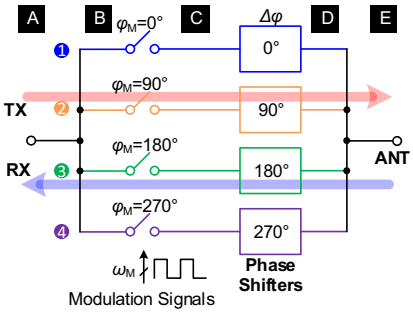

Fig. 2. Simplified schematic of the bi-directional frequency converter (BDFC).

the BDFC. The TX and RX signals can be then physically separated by a high-pass filter (HPF) and a low-pass filter (LPF). One clear advantage of this scheme is that, due to such a frequency split, the aforementioned chip-level TX-to-RX coupling is eliminated. Our later analysis will also show that the high TX-RX isolation is wideband in nature and is robust against device mismatch, non-ideal clocking, etc.

A 4-GHz prototype is demonstrated in a 65-nm bulk CMOS technology to verify the proposed concept. Measurement results show that the isolation of the proposed circuit is >25.5 dB across 30% fractional bandwidth, while taking only 0.27mm^2 core area.

II. Bi-Directional Frequency Converter: Concept

The simplified schematic of the two-port BDFC is shown in Fig. 2. It consists of four parallel paths, and each path is a series connection of one switch and one phase shifter. The switches are driven by modulation signals with quadrature phases, and are used for shifting the frequency and phase of signals.

Albeit the resemblance to a passive single-side mixer, one important property of the presented topology that was unexplored before is its *irreversible* frequency conversion process, namely, the BDFC always performs frequency downconversion regardless of the signal flow direction. To understand this, we examine the phasor diagram of signals at various stages (i.e. A∼E) of the schematic in Fig. 2. Fig. 3(a) shows the signal flowing from TX to ANT. For simplicity, only the positive frequency components are described in the following. At Stage A and B, the TX signal (ω_{TX}) is modulated with quadrature phase $\varphi_{M,\,i=1,2,3,4}$ of 0°, 90°, 180°, and 270° in Path ①, ②, ③, and ④, respectively. Thus, at Stage C, the two sideband frequency components (ω_{TX}-ω_M and ω_{TX}+ω_M) in Path i (i=1,2,3,4) carry phases:

$$\begin{cases} \varphi_{C,\,i} = \varphi_{M,\,i} & \text{for the upper sideband component} \\ \varphi_{C,\,i} = -\varphi_{M,\,i} & \text{for the lower sideband component} \end{cases}. \quad (1)$$

Next, these signals flow through the phase shifters. The values of the shifters ($\Delta\varphi_i$=$\varphi_{M,\,i}$) are selected to compensate the phase differences of the lower sideband (ω_{TX}-ω_M=ω_{ANT}) signals among the paths, so that after the signal summation, only such lower sideband component is preserved at the ANT port. In sum, the TX signal is shifted down by ω_M when flowing to ANT.

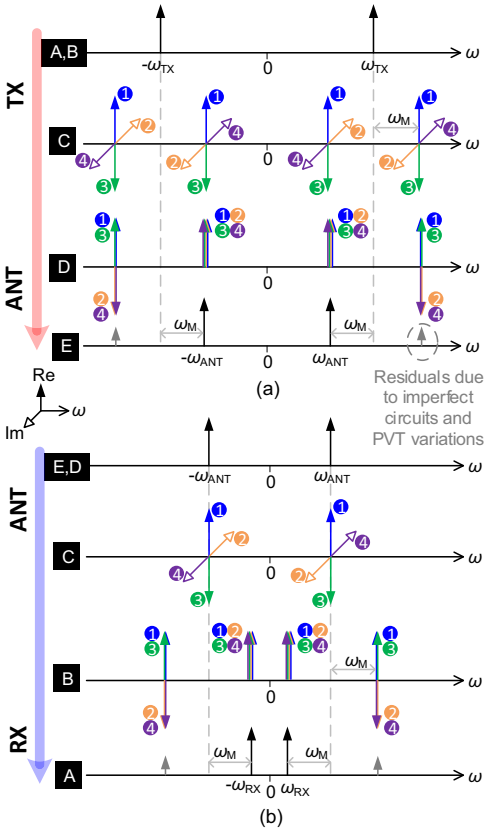

Fig. 3. Phasor diagrams of the signals flowing from (a) TX to ANT, and (b) ANT to RX.

For a signal flowing backward (i.e. ANT to RX), similar phasor-diagram analysis can be applied. As shown in Fig. 3(b), again only the lower sideband signal (ω_{ANT}-ω_M=ω_{RX}) presents at Node A on the left. A key observation to straightforwardly explain such an irreversible frequency conversion is that the condition listed in (1) is always valid, regardless of the signal frequency and its flow direction through the switches. Therefore, the additional, reciprocal phase $\Delta\varphi$ applied by the phase shifters always leads to the in-phase summation of the lower-sideband component and out-of-phase cancellation of the upper-sideband component. As a result, the RX signal is lower than ω_{ANT} by ω_M and lower than ω_{TX} by $2\omega_M$.

With an additional HPF at the TX port and a LPF at the RX port, our circuit presents identical TX and RX frequencies on a shared antenna interface, while separating them inside the chip. The former preserves all the benefits of conventional in-band full-duplex systems, and the latter eliminates the potential coupling between the TX and RX blocks on the same die.

To analyze the robustness of the TX-to-RX isolation, in Fig. 3 we also show the residual signals due to the presence of PVT variations and non-ideal circuits such as phase mismatch of clocks. For the TX-to-ANT direction, the residual is located at ω_{TX}+ω_M, and for the ANT to RX direction, the residual is located at ω_{ANT}+ω_M, so the leakage in both cases are located at irrelevant frequencies. It also indicates that, although phase shifters only apply precise $\Delta\varphi$ across a narrow band (hence

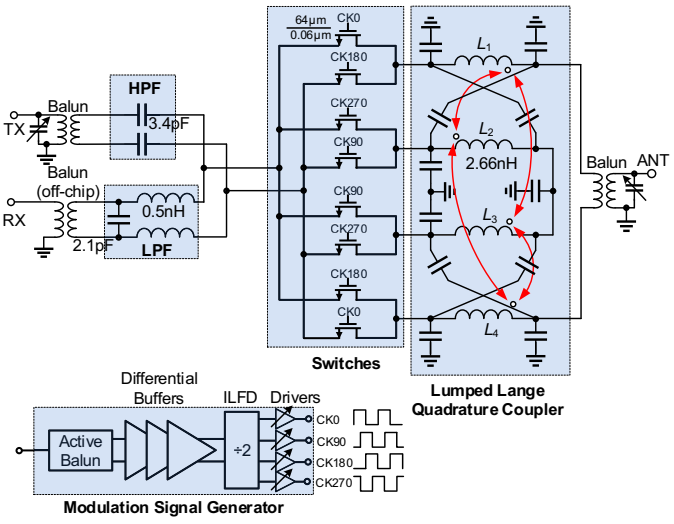

Fig. 4. Full schematic of the BDFC-based frond-end.

the above residuals exist at large frequency offset), effective TX-to-RX isolation can still be achieved across a broad band.

The presented circuit has a few more advantages in addition to the improved isolation and bandwidth. Firstly, the presented circuit uses only one set of switches (as opposed to two in [2]–[7]) in the signal paths, thus the linearity is improved. Secondly, by choosing ω_M to be close to ω_0, the circuit can also perform additional function of receiver down-mixing; so that the down-conversion mixer succeeding the RX port is omitted. Similarly, the BDFC can also be designed to perform frequency up-conversion, and the up-mixer in the transmitter side can be omitted.

III. Circuit Implementation

The full schematic of the BDFC-based frond-end with f_{ANT} around 4 GHz is shown in Fig. 4. For the aforementioned integrated down-mixing function, f_M is chosen to be ~4 GHz (i.e. homodyne receiver), hence f_{TX} is ~8 GHz. A lumped Lange quadrature coupler is adopted to realize the functions of phase shifters with compact area [8]. The differential switch pairs are used in each path for better impedance matching. A pair of MIM capacitors are used as the HPF at the TX port, and an *LC* LPF is employed at the RX port. To facilitate testing with G-S-G pad probing, two on-chip tunable baluns are implemented at the TX and ANT ports, and one off-chip balun is used at the RX port.

Fig. 5 shows the layout and simulated performance of the quadrature coupler. This lumped-element, differential version of Lange coupler consists of four coupled inductors and MOM capacitors (placed under the inductors). The inductors are laid out symmetrically and each one has about 2.5 turns, so there are quadrature ports at one side and differential ports at another side. The quadrature coupler is designed for two frequencies: ω_{ANT} and $\omega_{ANT} + \omega_M$. The simulated conversion loss is about 0.7 dB, and the simulated return loss is less than 10 dB for all ports at 4 GHz. The quadrature coupler occupies an area of 0.073 mm^2.

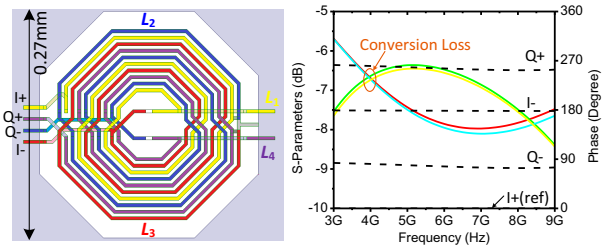

Fig. 5. Layout and simulated conversion loss (solid line) and relative port phases (dash line) of the quadrature coupler.

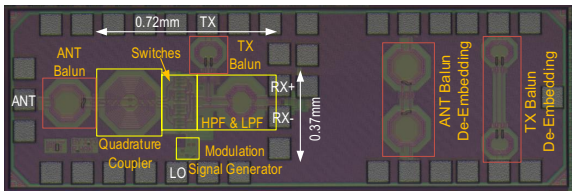

Fig. 6. Die photographs of the BDFC-based frond-end and back-to-back balun structures for de-embedding.

IV. Measurement Results

This BDFC-based full-duplex frond-end is fabricated using TSMC 65-nm bulk CMOS technology. Shown in Fig. 6, the core circuit including the quadrature coupler, switches, modulation signal generator, HPF and LPF occupies only 0.27 mm^2 area. The chip is tested by probing the ANT and TX pads; the low-frequency RX port is wire-bonded to the PCB and connected to an off-chip balun.

The RF performance of the BDFC-based frond-end is characterized by a Keysight PNA-X network analyzer (N5245B, configured for mixer measurement). The ANT balun, TX balun, and off-chip RX balun are de-embedded. The measured cross-frequency *S*-parameters for TX-to-ANT, ANT-to-RX, and TX-to-RX transmissions are shown in Fig. 7(a), (b), (c), respectively. The 3-dB insertion-loss bandwidth is from 3.4 to 4.6 GHz with 3.9-GHz modulation frequency (i.e. fractional bandwidth of 30%). The transmitter mode TX-ANT insertion loss is 3.0~5.8 dB. The receiver mode ANT-RX insertion loss is 3.2~6.1 dB. With 50-Ω load at the ANT port, the isolation between TX and RX is better than 25.5 dB across the whole operation band, which verifies our earlier analysis. The minimum noise figure (NF) is 5.8 and 5.9 dB when the TX is OFF and ON (with 0-dBm input power), respectively, showing the in-band full-duplex capability. As shown in Fig. 8, the measured IIP3 for the TX-to-ANT and ANT-to-RX directions are 29.5 and 27.6 dBm, respectively. The power consumption of the BDFC-based frond-end, entirely from the modulation signal generator, is 48 mW.

V. Conclusion

A new concept using frequency conversions of counter-propagating signals is demonstrated, which performs nonreciprocity similar to circulators and enables integrated in-band full-duplex systems. Table 1 compares the measured 4-GHz CMOS prototype with other state-of-the-art integrated

Table 1. Comparison with the State-of-the-Art Circulators in CMOS

	This Work	RFIC2019 [2]	JSSC2017 [4]	RFIC2018 [5]	JSSC2017 [6]	ISSCC2019 [7]
Technology	65-nm CMOS	40-nm CMOS	65-nm CMOS	180-nm SOI	45-nm SOI	45-nm SOI
Frequency (GHz)	3.4∼4.6	5.6∼7.4	0.65∼0.85	0.86∼1.08	22.7∼27.3	50∼56.8
Fractional Bandwidth	30%	28%	26.7%	17%	18%	14.6%
Isolation (dB)	25.5	18	15	25	18.5	20
TX-ANT/ANT-RX Insertion Loss (dB)	3.0/3.2	2.2/2.2	1.7/1.7	2.1/2.9	3.3/3.2	3.6/3.1
Noise Figure (dB)	5.8/5.9$^{(a)}$	2.4	4.3	3.2	3.3	3.2
TX-ANT/ANT-RX IIP3 (dBm)	29.5/27.6	17.5/17.5	27.5/8.7	50/30.7	20.1/19.9	19.4/19.0
On-Chip TX-RX Coupling	No	Yes	Yes	Yes	Yes	Yes
Down-Mixing for RX	Yes	No	Yes	No	No	No
Fully Integrated	Yes	Yes	No	Yes	Yes	Yes
Power Consumption (mW)	48	12.4	59	170	78.4	41
Core Area (mm^2)	0.27	0.45	25	16.5	2.16	1.72

$^{(a)}$ With TX off/on (0 dBm) and the homodyne RX down-conversion function included.

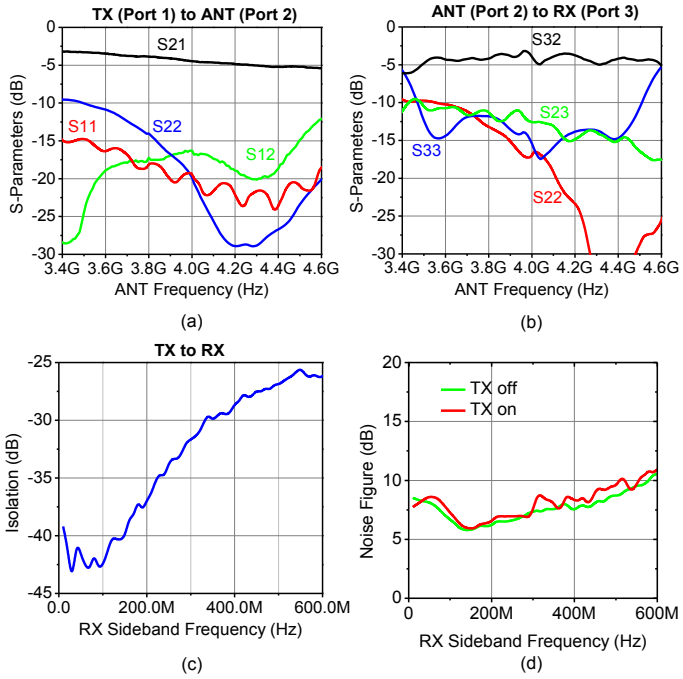

Fig. 7. Measured S-parameters of: (a) TX-to-ANT, (b) ANT-to-RX and (c) TX-to-RX paths, and (d) noise figure of the ANT-to-RX path.

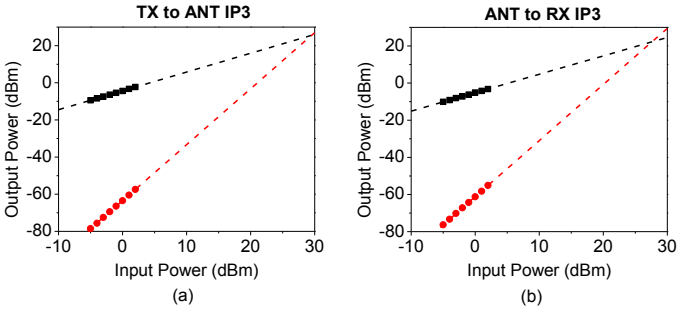

Fig. 8. Measured IP3 of (a) TX-to-ANT and (b) ANT-to-RX paths.

circulators. With the applied separation between the TX and RX frequencies, the presented scheme enables excellent isolation across a broad fractional bandwidth. The noise figure is expected to improve with more advanced technology nodes and SOI processes; we also note that the presented noise performance includes the integrated receiver down-mixer that the other chip works do not provide. Lastly, with only one set of switches in the signal path, high linearity is obtained without using a SOI or high-voltage CMOS process.

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