A 220-to-320-GHz FMCW Radar in 65-nm CMOS Using a Frequency-Comb Architecture

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***Abstract*— This article presents a CMOS-based, ultra-broadband frequency-modulated continuous-wave (FMCW) radar using a terahertz (THz) frequency-comb architecture. The high-parallelism spectral sensing provided by this architecture significantly reduces the bandwidth requirement for the THz front-end circuitry and ensures that the peak output power and sensitivity are maintained across the entire band of operation. The speed and linearity of frequency chirping are also improved by the comb system. An antenna-sharing scheme based on a square-mixer-first architecture is used, which not only leads to compact size but also facilitates the stitching of the multichannel radar IF data. To avoid the usage of high-cost silicon lens in the on-chip broadband radiation, a multi-resonance substrate-integrated-waveguide (SIW) antenna structure is innovated, which provides 15% fractional bandwidth for impedance matching. As a proof of concept, a five-tone radar prototype that seamlessly scans the entire 220-to-320-GHz band is demonstrated. In the measurement, the multi-channel-aggregated equivalent-isotropically radiated power (EIRP) is 0.6 dBm and is further boosted to ∼20 dBm with a TPX (polymethylpentene) lens. The measured minimum single-sideband noise figure (SSB NF) of the receiver, including the antenna loss and baseband amplifier, is 22.8 dB. Due to the comb architecture, the EIRP and NF values fluctuate by only 8.8 and 14.6 dB, respectively, across the 100-GHz bandwidth. The chip has a die size of 5 mm^2 and consumes 840 mW of dc power. This work marks the first CMOS demonstration of THz radar and achieves record bandwidth and ranging resolution among all radar front-end chips.**

***Index Terms*— Bandwidth, CMOS integrated circuit, frequency comb, frequency-modulated continuous-wave (FMCW) radar, substrate-integrated-waveguide (SIW) antenna, terahertz (THz).**

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I. Introduction

CHIP-BASED radar systems are quickly making their ways to manned/unmanned vehicles, industrial robotics, and consumer products, to name a few. In particular, many applications call for significantly increased radar-sensing resolution while keeping the form factor and cost low. This makes radar chips operating in the low-terahertz (THz) regime (∼300 GHz) very attractive. However, it is noteworthy that although such frequencies are already >4× higher than that of the mainstream millimeter-wave radars (24 and 77 GHz), the usable bandwidth is still insufficient for many emerging needs. For example, THz synthetic aperture radars (SARs) have been applied to rapid 3-D surface scanning of objects, and a 300-GHz SAR radar with 10-cm synthetic aperture can deliver an azimuth resolution of 1.5 mm for objects placed 30 cm away. However, for a matching ranging resolution, the radar bandwidth should be 100 GHz (i.e., ∼33% fractional bandwidth), which was not demonstrated in prior radars. Similarly, the abovementioned millimeter-level resolution is also highly desired for other areas, such as high-precision robotics and noninvasive detection of small defects in foam, plastic, and rubber products.

Conventional frequency-modulated continuous-wave (FMCW) radars are based on a single-tone architecture and thus provide limited frequency scanning range due to circuit limitations. In particular, for >100-GHz radars, since the operation frequencies are close or even above the cutoff frequencies of the silicon transistors, the related circuit designs need to routinely utilize high-Q resonance for efficiency enhancement. This inevitably reduces the circuit bandwidth. The high carrier frequency also mandates the usage of on-chip antennas, which further aggravates the problem. For front-side radiating structures such as patch antenna, the fractional bandwidth is severely limited to a few percent, due to the short inter-metal-layer distance. Back-side radiating structures, such as dipole and slot antennas, deliver much higher bandwidth, but they require high-cost silicon lens to mitigate the excitation of substrate mode. All these problems cause not only reduction of bandwidth that a radar can cover but also severe performance degradation at the two edges of the band. A survey of previously reported millimeter-wave and THz radars in silicon are given in Fig. 1. At present, the highest reported FMCW bandwidth is 70 GHz from the 130-nm SiGe radar in [1]. Excellent equivalent-isotropically radiated power (EIRP) and noise figure (NF) of 18.4 dBm (with a TPX lens) and 19.7 dB

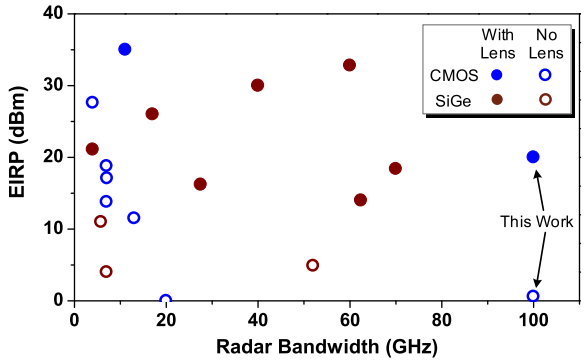


Fig. 1. Survey of prior millimeter-wave and THz radars using CMOS and SiGe technologies.

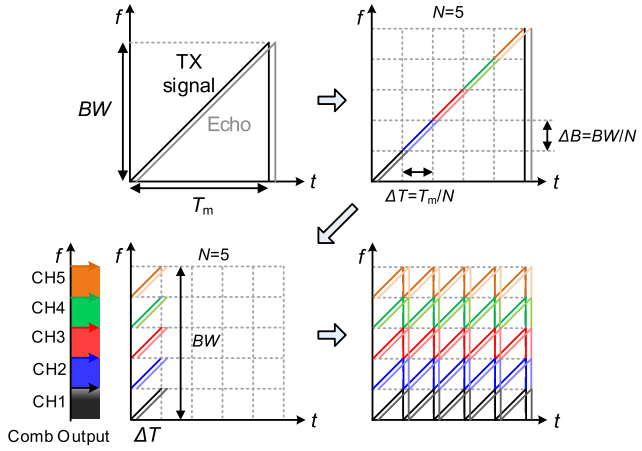


Fig. 2. Broad spectral sensing using simultaneous multi-channel operations in a THz-comb radar architecture.

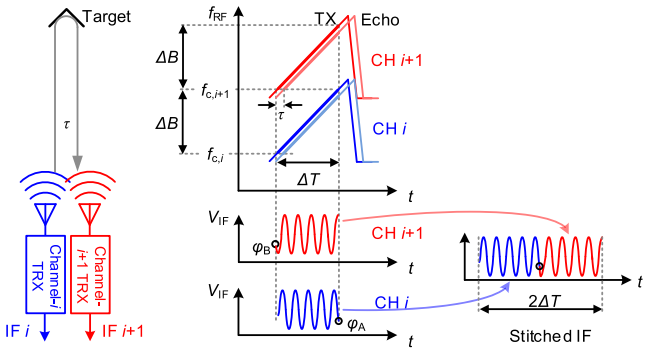


Fig. 3. Multi-channel phase coherency in an ideal THz comb radar. The IF data clipping under the over-chirping of the FM signal is also shown (for more details of over-chirping, see Section IV-B).

are demonstrated, respectively; they, however, vary by 10.5 and 28.6 dB across the 70-GHz bandwidth. Another 55-nm SiGe radar in [2] reduces the EIRP variation to 7.7 dB, but it requires the attachment of a silicon lens, and compared to [1], the achieved bandwidth and EIRP reduce to 62.4 GHz and 14 dBm, respectively. It is also noteworthy that all ultra-broadband radars demonstrated so far are based on high-speed SiGe processes (recently [3] reported a broadband frequency multiplier with 140-GHz bandwidth in a 130-nm SiGe process), and low cost CMOS-based radars still operate below 200 GHz and their bandwidths are within 20 GHz. In [4], a 2×2 pulse radar array at 160 GHz is built using a 65-nm CMOS process, and in [5], an FMCW radar at 145 GHz is built using a 28-nm CMOS process; they, however, only deliver bandwidths of 7 and 13 GHz, respectively.

Although the above tradeoff between performance and bandwidth seems fundamental, we demonstrate in this article that a THz-frequency-comb architecture, along with its high-parallelism spectral sensing scheme, is able to optimize both metrics in a scalable manner. As a prototype of this approach, a five-comb-tone radar transceiver, which is originally presented in [6], is implemented using a 65-nm bulk CMOS process. It provides seamless coverage of an entire 220-to-320-GHz band, and the variations of output power and NF in the band are only 8.8 and 14.6 dB, respectively. This work not only enables a theoretical bandwidth-limited ranging resolution of 1.5-mm (un-windowed) but also marks the first CMOS demonstration of radars reaching the THz regime. In Section II, the THz-comb architecture, as well as its advantages in radar sensing, is presented. In Section III, details of a few key circuit blocks of the radar are described. In Section IV, characterizations of the electrical performance and ranging resolution of the radar are provided. Finally, in Section V, we conclude this article with a comparison with prior state of the arts.

II. THz-Comb Radar for Broadband Sensing: Concept and Circuit Architecture

Fig. 2 shows the time-variant frequencies of the transmitted (TX) and received (RX) signals in a conventional single-tone FMCW radar with a total bandwidth of BW and chirping duration of T_m. For comparison, the concept of a frequency-comb radar is also shown in Fig. 2. Instead of consecutively scanning the entire bandwidth, it divides BW into N identical segments and sweeps them simultaneously using an array of dedicated transceivers (i.e., channels), which keeps equal spacing of $\Delta B = BW/N$ among their carrier frequencies (hence a frequency comb). As we will show next, each radar transceiver has its own antenna, and the received echo signal is directly mixed with the transmitted signal to generate an IF output. Note that a synthetic bandwidth technique similar to that in Fig. 2 was previously reported in a C-band radar in [7], where the multiple channels are scanned sequentially by a single, tunable transceiver. In our work, the small size of THz circuitry allows for parallel spectral sensing with a monolithic transceiver array.

For a certain channel (e.g., Channel-i), we express the TX signal as

$$S_{\mathrm{TX},i}(t) = A_{\mathrm{TX},i} \cos\left[\left(2\pi f_{c,i} + \frac{\pi \Delta B t}{\Delta T}\right)t + \varphi_i\right] \quad (1)$$

where $A_{\mathrm{TX},i}$ and φ_i are the signal amplitude and phase, respectively, $f_{c,i}$ is the frequency at the start of the chirp ($t = 0$), and $\Delta T = T_m/N$ is the duration of one chirp (see Fig. 3). Suppose that the time-of-flight of wave, determined

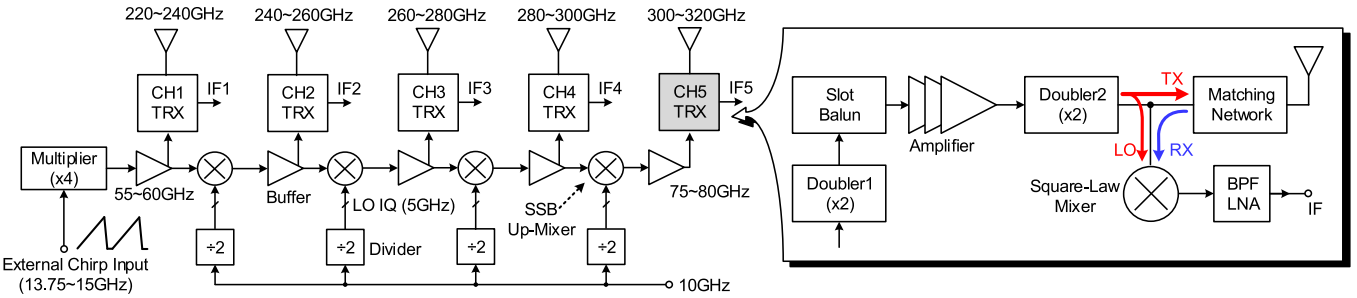


Fig. 4. Block diagram of the 220-to-320-GHz radar front end in CMOS.

by the object distance, is τ, and the received signal (with an amplitude of $A_{\mathrm{RX},i}$) for this channel is

$$S_{\mathrm{RX},i}(t) = A_{\mathrm{RX},i}\cos\left[\left(2\pi f_{c,i} + \frac{\pi\,\Delta B(t-\tau)}{\Delta T}\right)(t-\tau) + \varphi_i\right]. \tag{2}$$

After mixing the abovementioned signals, the output IF signal is

$$\begin{aligned} S_{\mathrm{IF},i}(t) \;&=\; S_{\mathrm{TX},i}(t)S_{\mathrm{RX},i}(t),\ \text{then, with low-pass filtering} \\ &\Longrightarrow \frac{A_{\mathrm{TX},i}A_{\mathrm{RX},i}}{2}\cos\left(\frac{2\pi\,\Delta B}{\Delta T}\tau t + 2\pi f_{c,i}\tau - \frac{\pi\,\Delta B\tau^2}{\Delta T}\right) \end{aligned} \tag{3}$$

where $\pi\,\Delta B\tau^2/\Delta T$ is in practice small enough and can be ignored. One key point of (3) is that the phase of $S_{\mathrm{IF},i}(t)$ is determined by the chirp slope $\Delta B/\Delta T$, the time-of-flight τ, and the frequency at the start of the chirp $f_{c,i}$, and not dependent on the initial phase of $S_{\mathrm{TX},i}$, which varies significantly among different channels. Note that $\Delta B/\Delta T$, τ, and $f_{c,i}$ are all independent with $S_{\mathrm{TX},i}$. In other words, the phase of IF signal relies on only the chirp slope and starting frequency, as well as the object distance, instead of the initial phase of $S_{\mathrm{TX},i}$. Also, the only term varies with channels is the starting frequency $f_{c,i}$ that is a known variable. Therefore, at the end of the chirp ($t = \Delta T$), the phase of the IF signal (φ_A in Fig. 3) becomes

$$\varphi_A = \varphi_{\mathrm{IF},i}(t = \Delta T) = 2\pi\,\Delta B\tau + 2\pi f_{c,i}\tau = 2\pi f_{c,i+1}\tau. \tag{4}$$

Note that (4) uses the condition $f_{c,i+1} = f_{c,i} + \Delta B$, which is accurately realized in our architecture to be shown next. It also shows that the IF phase of Channel-i at the chirp end is identical to the IF phase of Channel-$(i+1)$ at the chirp start (namely, $\varphi_B = \varphi_B$ in Fig. 3). It indicates that when the multi-channel IF signals are stitched in series (see Fig. 3), the result is in theory equivalent to the output expected from a hypothetical single-tone radar with the same total bandwidth of $\mathrm{BW} = \Delta B \cdot N$.

The comb radar architecture, due to its high-parallelism nature, brings about a few distinct advantages. First, the fractional bandwidth required for each THz-frontend component (including the on-chip antenna) is relaxed by N times. Correspondingly, high-Q passive structures can be adopted. This also allows for circuit configurations tuned at transistor optimal conditions, such as the maximum available gain near $f_{\max}$ [8]–[10]. Peak circuit performance, therefore, can be maintained across a broad frequency range in a relay manner. We note that although the peak EIRP and minimum NF are normally quoted in the literature on radars, the degraded performance at the band edges ultimately limits the detection distance or speed due to the lower SNR of the amplitude-modulated received signal. The presented scheme effectively improves those "worst case" merits. Second, the comb architecture also significantly relaxes the requirement for the radar chirping frequency synthesizer [e.g., direct-digital synthesizer (DDS)]. As shown in our radar system (see Fig. 4), all on-chip transceivers are referenced to a single synthesizer. Therefore, the fractional bandwidth required for the synthesizer is reduced by N times as well. The narrower bandwidth also enables lower power consumption and smaller relative chirped frequency error of the synthesizer. Note that such an error is also not accumulated over different comb channels (but is re-aligned instead) due to the successive frequency upconversion scheme; therefore, the overall linearity of the frequency chirping is improved by the comb architecture and hence reduced linewidth broadening after the fast Fourier transform (FFT) [7]. Third, bandwidth extension is achievable by simply adding more channel transceivers. Such high scalability comes with the expense of larger chip area and power. However, due to the compactness of THz components ($\sim$10$\times$ smaller than their peers at 77 GHz), we will show that the overall chip area remains acceptable. Also, Fig. 2 shows an $N\times$ time reduction for a full-bandwidth scan (for the same SNR), so the total energy consumed by the comb radar remains the same. With higher multi-channel-aggregated EIRP, the scheme is equivalent to the power combining of traditional radars. In fact, due to the aforementioned circuit efficiency enhancement, we in Sections IV and V demonstrate that our comb radar consumes less power than many single-tone THz radars.

The block diagram of our 220-to-320-GHz radar front end is shown in Fig. 4, which includes a daisy chain of successive-frequency-upconversion stages. The chain starts from a 13.75 to 15-GHz external chirp signal fed into a quadrupler and then amplifies the 55–60-GHz chirp signal and increases its frequency by 5 GHz in each chain stage. To obtain the LO quadrature phases for the single-sideband (SSB) mixer in each stage, the 5-GHz LO is generated by a set of static dividers ($\div 2$) with a 10-GHz input.[1] If the LO signal and the chirp signal are generated on chip, a cascaded phase-locked

[1]The off-chip source for the 10-GHz input is synchronized with the 13.75–15-GHz chirping signal.

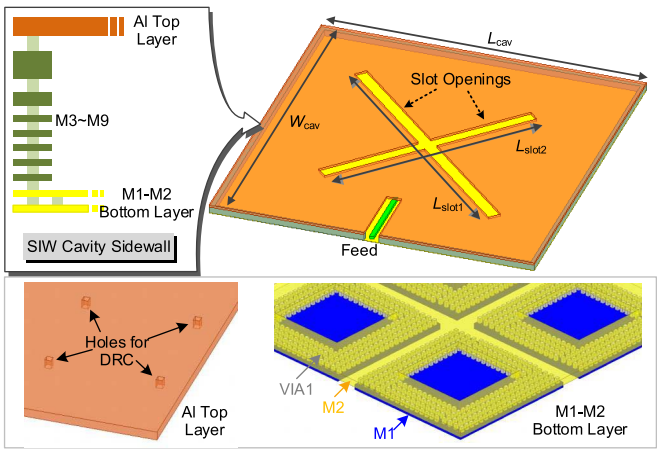


Fig. 5. 3-D structure of the SIW dual-slot antenna with multi-resonances.

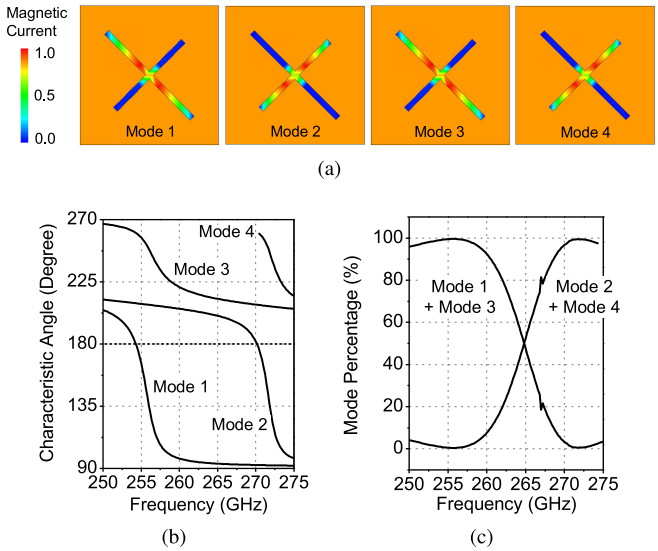


Fig. 6. Simulated CMs of the antenna. (a) Equivalent magnetic current distribution in the slots. (b) Characteristic angles. (c) Mode contributions at varying frequencies.

loop (PLL) architecture [11] can be used to generate and phase-synchronize the 10-GHz LO signal and the 55–60-GHz chirp signal [12]. The fact that the 10-GHz LO spectrum is directly shifted (rather than multiplied) to the THz output significantly lowers the phase-noise performance requirement for the 10-GHz PLL (compared to that of the 55–60-GHz PLL), allowing for larger design trade space for this block added to the synthesizer in a conventional radar system. Each stage also drives a THz transceiver, of which the block diagram is also given in Fig. 4. In the case of the fifth channel, the transceiver input at 75–80 GHz is frequency-doubled twice and is then radiated through an on-chip antenna. In the meantime, part of the THz signal power, as well as the echo signal received by the same antenna, is also injected into a square-law mixer (details given in Section III-C). Subsequently, the down-mixed IF signal representing the time of flight of the THz wave is obtained. Further digitization and processing of the multi-channel IF signals are performed off-chip.

III. Details of Circuit Implementations

We in this section describe the design details of key circuit blocks, mainly based on Channel-3 without loss of generality.

A. SIW-Backed Dual-Slot Antennas With Multi-Resonances

Even though the THz-comb architecture is used, each on-chip antenna should still provide good impedance matching and radiation efficiency across a wide bandwidth of 20 GHz, in order to cover the targeted 100-GHz aggregated bandwidth. Typically, antenna structures without on-chip ground planes, such as slot and dipole antennas, deliver impedance-matching ($S_{11} < -10$ dB) fractional bandwidth of >20% [13]. However, they require backside-attached silicon lens to avoid the excitation of substrate mode [2], [14], which, however, significantly increases the radar cost. Typical silicon lenses, given their small size (<1-cm diameter), also require precise chip antenna alignment with the lens center; such a configuration is, however, incompatible with our multi-antenna comb architecture. The on-chip dipole antennas with PCB backside reflectors [15], [16], although offer large bandwidth, require an impractical wafer thinning to <100 μm for ~300-GHz operations. They also normally have large lateral-direction coupling due to the loosely confined wave in the substrate and tilted radiation beam due to nearby metal structures. In comparison, ground-shielding antennas with front-side radiation, such as a patch antenna, mitigate the abovementioned problems. However, due to the high-Q resonance formed by the closely spaced top and bottom metal layers, the impedance-matching fractional bandwidth realizable with similar frequency and CMOS process is only 2%–3% [17]. Moreover, the coupling between two patch antennas is still large when they are placed side-by-side for minimum chip area.

In our chip, a substrate-integrated-waveguide (SIW)-backed dual-slot antenna with multiple resonances is adopted to enable both front-side radiation and wide matching bandwidth. The 3-D structure of the antenna is shown in Fig. 5. In the SIW cavity, M1 and M2 shunted layers form the bottom ground plane, M3-to-M9 stack forms the four sidewalls, and the top aluminum layer forms the upper cavity plane. Holes are dug on the bottom and top metal planes to pass the design-rule-check (DRC), and antennas are covered by metal dummy block layers to prevent the dummy metal fillings. In addition, two orthogonal slots are created in the top metal. Since an eigenmode analysis is not suitable for lossy, radiative structures, to explain the antenna behavior, analyses based on a characteristic-mode (CM) theory [18], [19] are performed. Using FEKO [20], four antenna CMs are identified, as shown in Fig. 6(a), and their characteristic angles (φ_{CA}) are given in Fig. 6(b). Modes 1 and 2 (with φ_{CA} going across 180°) are associated with the resonances of the longer and shorter slots, respectively; Modes 3 and 4 (with φ_{CA} being non-180° but exhibiting dramatic change), which are originated from the resonance of the SIW cavity, are the parasitic modes of Modes 1 and 2, respectively.

By adjusting L_{slot1} and L_{slot2} in Fig. 5, we position the resonance frequencies of Modes 1 and 2 at the two sides of

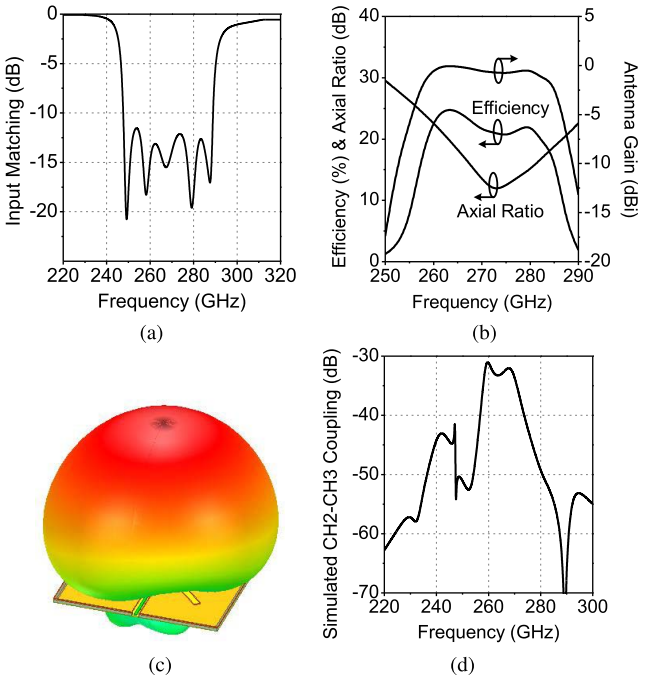


Fig. 7. Simulated results of the on-chip SIW antenna in Channel 3. (a) Input matching (antenna matching network included). (b) Radiation efficiency, axial ratio of polarization, and antenna gain. (c) radiation pattern. (d) Inter-antenna coupling.

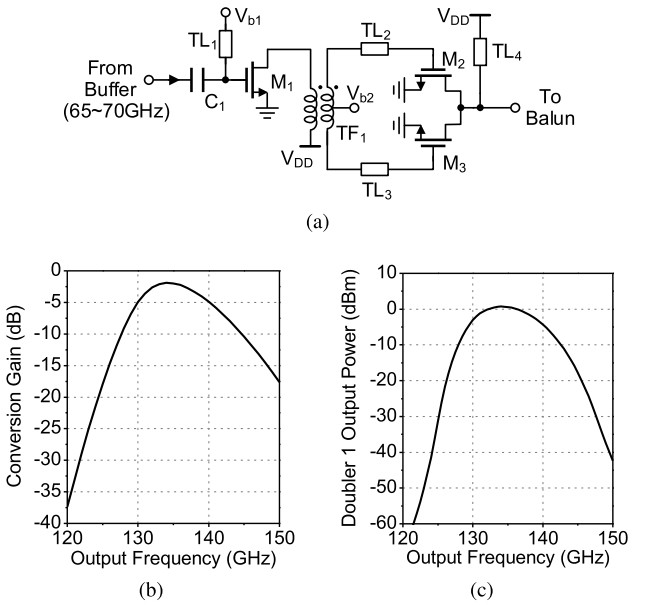


Fig. 8. (a) Schematic of Doubler 1 inside the radar transceiver. (b) Simulated doubler conversion gain at varying output frequency (P_{in} = 2 dBm). (c) Simulated doubler output power (the input power variation from the preceding circuitry is also included).

the radar channel band; in addition, tuning W_{cav} and L_{cav} (hence Modes 3 and 4) further flattens the off-resonance impedance change. These efforts eventually lead to a broad impedance-matching bandwidth from 250 to 290 GHz (i.e., 15% fractional bandwidth), as the simulation shown in Fig. 7(a). Also, note that the radiated waves from Modes 1 and 3 and Modes 2 and 4 are linearly polarized in two orthogonal directions. Therefore, as the contribution of each mode varies with frequency [see Fig. 6(c)], the polarization of the overall radiated field rotates.[2] The simulated antenna pattern is shown in Fig. 7(c), which has a gain of $-1\sim0$ dBi across the 260–280-GHz band. Finally, Fig. 7(d) shows that due to the high confinement of the resonance wave in the metal cavity, as well as the difference of antenna center frequencies, the inter-antenna coupling is weak (<-31 dB).

B. THz Transmitter Chain

The schematic of Doubler 1 of the THz transceiver is shown in Fig. 8(a). The millimeter-wave signal from the frequency -conversion chain drives a common-source buffer (M_1) and is then turned into differential mode through a single-loop transformer (TF_1). A push–push structure is then used to generate the second-harmonic component while suppressing the tone at input frequency. As shown in Fig. 8(b) and 8(c), the peak conversion gain and output power of Doubler 1 are

[2]This is different from circular polarized waves, which is undesired for our TX-RX antenna sharing scheme. Since the antenna feed in Fig. 5 aligns with the centers of both slots, the radiated fields in the two orthogonal directions are always in-phase. The polarization of the total radiation is therefore always linear, as the >11.6-dB simulated axial ratio shown in Fig. 7(b).

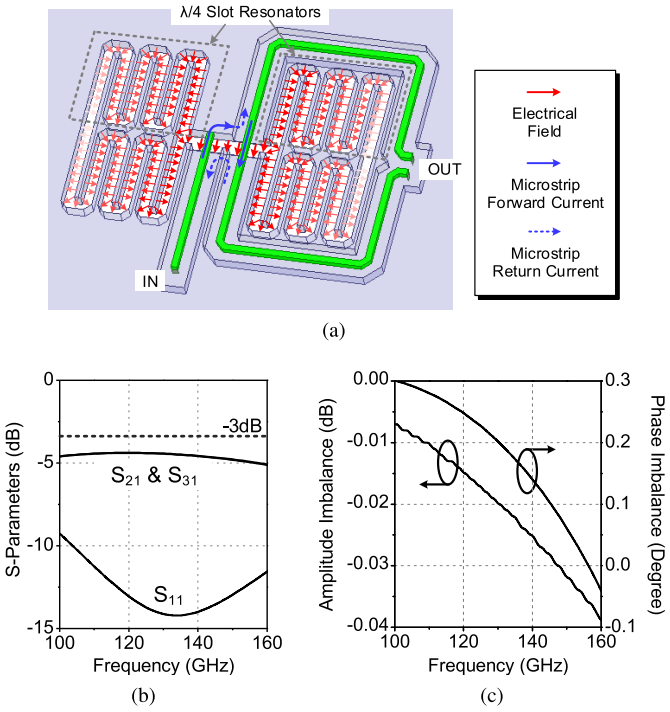


Fig. 9. (a) 3-D structure of the 135-GHz slot-based balun. (b) Simulated insertion loss (S_{21} and S_{31}) and return loss (S_{11}). (c) Simulated phase and amplitude imbalance at the differential outputs.

-2 dB and 0.7 dBm, respectively. The simulated dc power of the entire circuit in Fig. 8(a) is 21 mW.

As shown in Fig. 4, before the second frequency doubling in the THz transceiver, the signal from Doubler 1 is converted into differential mode using a slot balun [see Fig. 9(a)] and is boosted by a chain of amplifiers [see Fig. 10(a)]. Since the

amplifiers are based on a pseudo-differential topology with a neutralization technique (details to be given next), they are sensitive to any amplitude and phase imbalance of the input signal. To minimize such imbalance, a sub-THz balun structure based on a pair of folded slot resonators [21] is adopted. As shown in Fig. 9(a), the balun input and output consist of a single-ended microstrip line and a pair of differential microstrip lines, respectively. A gap in the ground plane couples the input and output; it is also enclosed by two pairs of quarter-wavelength slot resonators that present high impedance on the two ends of the ground gap. The resonators are folded for compact size and minimum radiative loss. With the excitation by the single-ended signal in the input microstrip, only a fully differential quasi-TE mode wave is allowed in the ground gap [22]. Meanwhile, since the microstrip pair and the slot resonators at the output side are completely symmetric, when the abovementioned quasi-TE wave is coupled back to microstrip mode, the generated output signals are expected to keep perfect out-of-phase balance across a wide range of frequency. Our full-wave electromagnetic simulation shows that the insertion loss of the balun is 1.3 dB [see Fig. 9(b)] and the amplitude/phase imbalance across a 100–160-GHz band is negligible [see Fig. 9(c)].

The signal generated by the slot balun is then amplified by three identical, pseudo-differential amplifier stages, as shown in Fig. 10(a). The stages are coupled through central-tapped transformers. In each stage, a cross-coupled capacitor pair (e.g., C_4 and C_5) is used to create negative capacitance that cancels C_{gd} of the transistors. Although this neutralization scheme does not provide the highest possible gain compared to the techniques in [8]–[10] and [21], the device unilaterization that this scheme enables allows for higher stability and broader bandwidth [23]. The simulated gain of the amplifier chain is shown in Fig. 10(b), with an average value of ∼7 dB in the 130–140-GHz band. Finally, the TX signal is frequency doubled again by a pair of push–push transistors (M_{10} and M_{11}). The inductive reactances provided by transmission lines TL_7 and TL_8 boost the swing of the device drain voltages (hence higher nonlinearity), and TL_9 and TL_{10} are used as part of the output matching network. In the simulation, the amplifier chain and Doubler 2 consume dc power of 57 and 24.8 mW, respectively, and the final TX output power (as shown in Fig. 10(c), is −5 to −1.5 dBm at 260–280 GHz.

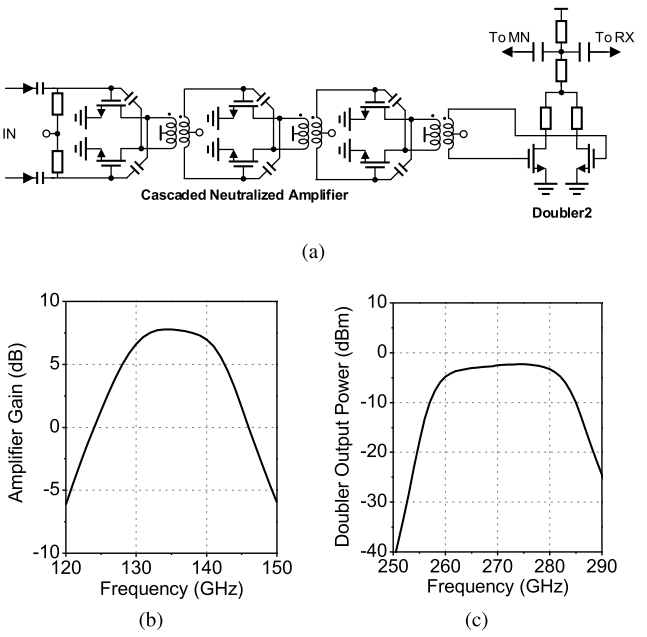


Fig. 10. (a) Schematic of Doubler 2 and its input amplifier inside the THz radar transceiver. (b) Simulated gain of the cascaded neutralized amplifier chain including the input slot balun. (c) Simulated output power of Doubler 2 with an input power of −1 dBm.

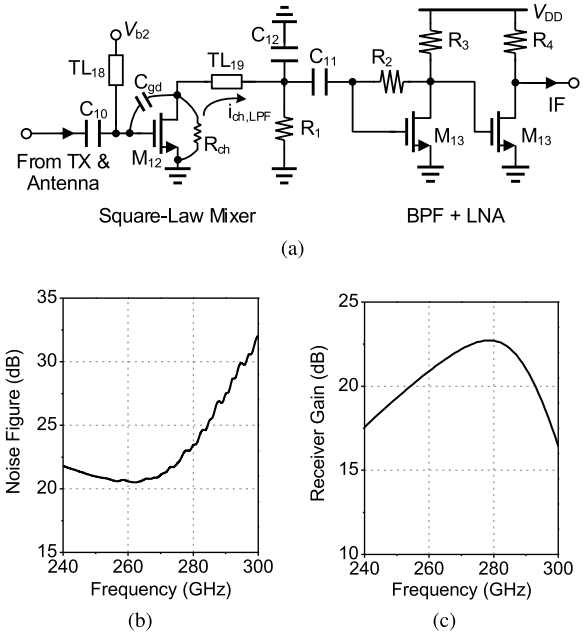


Fig. 11. (a) Schematic of the THz radar receiver chain. (b) Simulated SSB NF of the square-law mixer. (c) Simulated conversion gain of the receiver chain. The IF frequency in the simulation is 3 MHz.

C. THz Receiver Chain

Most of the previous chip radars employ separate antennas for the TX and RX [2], [4], [5]. Such a configuration, however, is not desirable in our comb architecture because the integration of the associated on-chip antennas requires an exceedingly large die area. In comparison, antenna sharing between TX and RX significantly reduces the chip area, but the direct injection of the large power TX signal into RX causes severe nonlinearity or even saturation of the RX low-noise amplifier. To mitigate this problem, a circularly polarized antenna cascaded with a directional coupler is used in the SiGe radar in [14]. Since the operation frequency of our radar has exceeded the transistor speed limit of the 65-nm CMOS process used here (f_{max} = 280 GHz), a pre-amplifier in the RX front end would not be possible, and the radar echo signal can only be directly down-converted. Although this passive-mixer-first architecture has degraded sensitivity (i.e., lower conversion gain and higher NF), its high linearity also makes the abovementioned antenna-sharing scheme possible.

The schematic of the radar receiver of one channel is shown in Fig. 11(a), where a unique square-law mixer topology

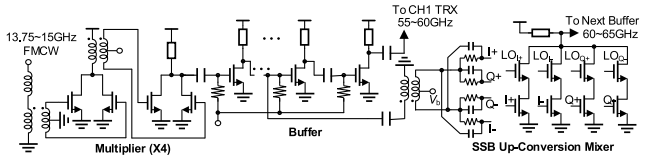


Fig. 12. Schematics of input multiplier (X4), buffer, and SSB mixer.

is adopted. The mixer is based on a MOSFET (M_{12}) with zero drain bias ($V_D = 0$ V) and sub-threshold gate bias ($V_G = V_{b2} = 0.28$ V $< V_T$). The channel resistance $R_{\rm ch}$ therefore changes exponentially with the instantaneous gate voltage ($V_g = V_G + v_g$)

$$R_{\rm ch} = R_{\rm ch0} \cdot e^{\frac{V_T - V_g}{n\phi_t}} = R_{\rm ch0} \cdot e^{\frac{V_T - V_G - v_g}{n\phi_t}} \tag{5}$$

where n is the ideality factor (close to unity), ϕ_t is the thermal voltage (26 mV at room temperature), and $R_{\rm ch0}$ is the channel resistance at $V_g = V_T$. Next, we note that at THz frequencies, the ac voltages at gate and drain are similar ($v_g \approx v_d$) due to the parasitic capacitance $C_{\rm gd}$ between the two terminals. Therefore, the channel current is

$$i_{\rm ch} \approx \frac{v_g}{R_{\rm ch}} = \frac{v_g}{R_{\rm ch0} \cdot e^{\frac{V_T - V_G - v_g}{n\phi_t}}} = \frac{e^{\frac{V_G - V_T}{n\phi_t}}}{R_{\rm ch0}} v_g \cdot e^{\frac{v_g}{n\phi_t}} \tag{6}$$

$$\approx \frac{e^{\frac{V_G - V_T}{n\phi_t}}}{R_{\rm ch0}} \left(v_g + \frac{v_g^2}{n\phi_t} \right). \tag{7}$$

In Fig. 11(a), the second-order term in (8) is used for RX down-conversion; by directly superposing the TX and echo signals on the device gate ($v_g = v_{\rm TX} + v_{\rm RX}$), an IF signal ($f_{\rm IF} = f_{\rm TX}$-$f_{\rm RX}$) carrying the object distance information is obtained

$$i_{\rm IF} = \frac{e^{\frac{V_G - V_T}{n\phi_t}}}{n\phi_t R_{\rm ch0}} |v_{\rm TX} v_{\rm RX}| \cos\left[(\omega_{\rm TX} - \omega_{\rm RX})t + \varphi_{\rm IF}\right]. \tag{8}$$

The presented THz square-law mixer well fits the antenna-sharing architecture and consumes zero dc power. Its fully passive condition not only accommodates large input power but also provides an output with minimum flicker noise [24]. The latter is particularly important for short-range THz radars, of which the generated IF frequency is normally low. In the simulation, the mixer has $P_{\rm 1dB}$ of -5.5 dBm, and a single-sideband noise figure (SSB NF) of $20.6 \sim 23.6$ dB in the 260–280-GHz band [see Fig. 11(b)]. Following the mixer is a two-stage, self-biasing baseband amplifier, which has 3.3-nV/Hz$^{1/2}$ simulated input-referred noise (lower than the mixer output noise) and enables an overall conversion gain of 21–21.7 dB for the receiver chain [see Fig. 11(c)]. An *RC* high-pass filter is added between the THz mixer and the baseband amplifier, in order to suppress any unwanted low-frequency IF signal caused by the reflections at objects (e.g., bond wires) in close proximity to the chip. It also filters out the low-frequency components due to the power fluctuation of the THz LO signal during chirping (see Section IV-B), which is also down-converted by the THz square-law mixer.

D. Successive Frequency-Conversion Chain

Between radar channels, the frequency conversion for each THz transceiver input is realized by a buffered SSB mixer (see Fig. 12). To generate the RF *I–Q* signals for the mixer, a set of broadband and compact *RC* polyphase filters are adopted. The loss of the filters is compensated by a chain of common-source amplifiers in each stage. Each SSB mixer increases the frequency by 5 GHz, and the 5-GHz mixer *I–Q* LO signals are generated from a digital divider ($\div 2$) clocked at 10 GHz. At the input of the frequency-conversion daisy chain, two push–push frequency doublers that are cascaded through a transformer are used to convert the input FMCW signal at 13.75–15 GHz into 55–60 GHz.

The spurs due to the successive frequency-conversion chain may be of concern. These spurs with 5-GHz frequency spacing derive from the SSB mixer due to the RF and LO *I-Q* imbalance. The measured spurs are about 39 dB lower than the THz transmitted signal. Besides, antenna coupling between channels generates leakages. All spurs and leakages are down-converted by the square-law mixer and then generate dc due to the self-mixing and ($m \cdot 5$ GHz) out-of-band IF signals, where m is the integer. As shown in Fig. 11(a), the dc due to the self-mixing is blocked by the *RC* high-pass filter. The low-pass output characteristic of the square-law mixer suppresses the out-of-band IF signals. The simulated out-of-band input $P_{\rm 1dB}$ of the whole receiver limited by the square-law mixer is -5.5 dBm, which is higher than the power of spurs and leakages. Therefore, all spurs and leakages do not affect the receiver.

IV. Measurement Results

The 220-to-320-GHz comb radar is implemented using TSMC 65-nm bulk CMOS technology, and its die photograph is shown in Fig. 13(a). The chip occupies an area of 2×2.5 mm^2. For testing, the chip is mounted on a PCB with standard wire bonding [see Fig. 13(b)]. As shown in Fig. 13(a), the bond pads are placed away from the on-chip antennas with the largest possible distance, in order to minimize the radiation interference from the bond wires. To enhance the antenna directivity, a detachable low-cost TPX polymethylpentene lens (diameter = 25.4 mm and focal length = 10 mm) is placed at the front side of the chip [see Fig. 13(c)]. The measured total power consumption of the CMOS radar chip is 0.84 W.

A. Characterization of Electrical Performance

In this part of the measurement, the RF input of the chip is provided by an external signal generator with no FM chirping, and each THz transceiver can be activated/de-activated independently. The performance of the chip transmitter mode is measured using the setup shown in Fig. 14(a). First, we use a horn antenna ($G_{\rm ant} \approx 25$ dBi), a VDI WR-3.4 vector network analyzer (VNA) frequency extender (configured in receiver mode), and a spectrum analyzer to down-convert and measure the radiated waves of the chip. Since the polarization directions of the SIW-backed dual-slot antennas rotate with frequency, the measured output power by placing the horn antenna

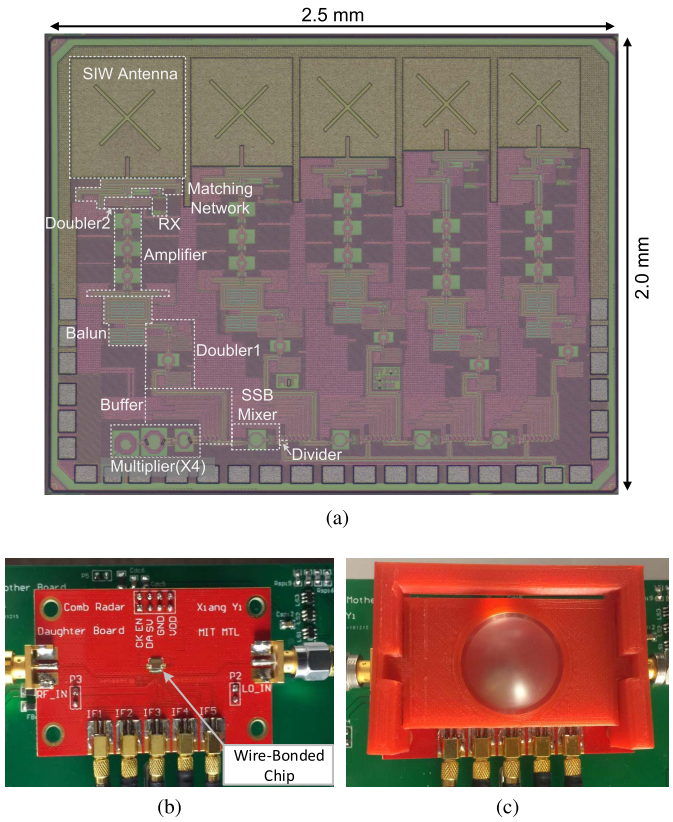


Fig. 13. Photographs of (a) 220-to-320-GHz CMOS radar, (b) wire-bonded chip on a PCB, and (c) chip package with a front-side TPX lens.

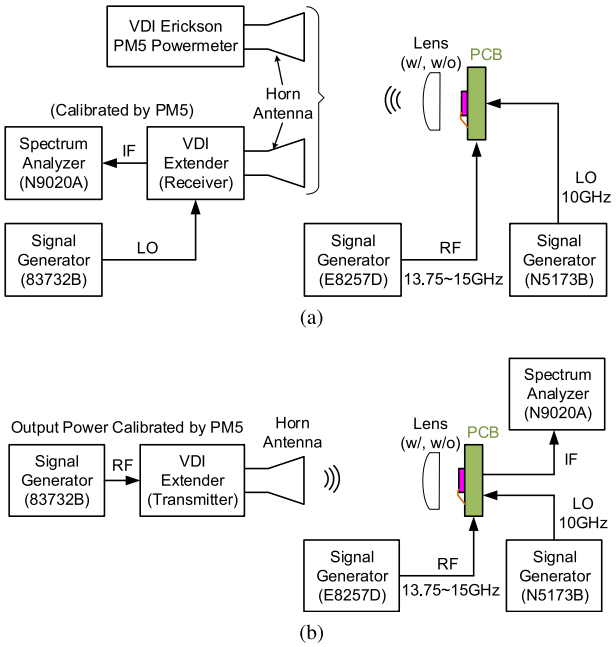


Fig. 14. Measurement setups for RF performance of (a) TX and (b) RX.

vertically and horizontally is added together. Fig. 15(a) shows the measured power at varying distance d between the chip (without the TPX lens) and the VDI extender. Note that a VDI Erickson PM5 power meter is also used to calibrate the conversion loss of the VDI extender across the WR-3 band and to directly measure the radiated power for $d < 5$ cm as a

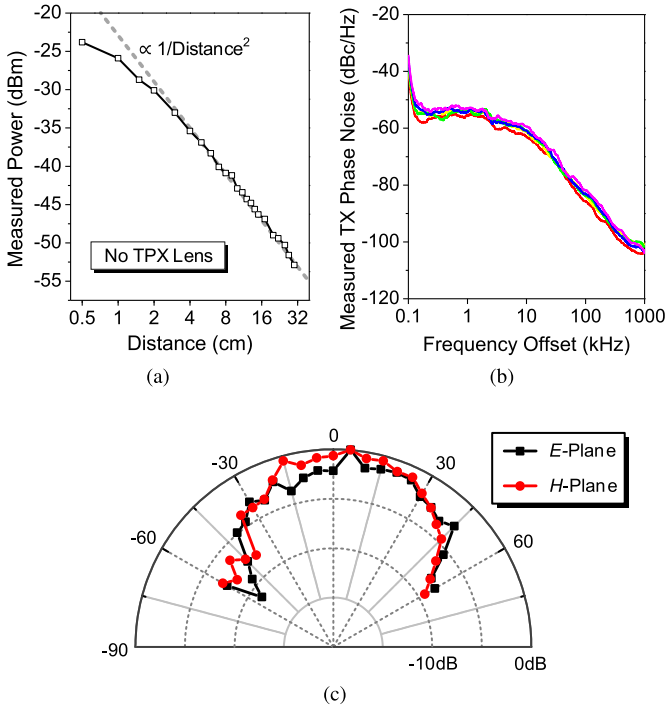


Fig. 15. (a) Power received by the VDI VNA extender at varying distance. (b) Measured TX phase noise of the radar. (c) Measured TX radiation pattern without the TPX lens. Note that these results are from Channel 3 of the chip.

cross-check. Fig. 15(a) shows that beyond the far-field limit of ~3 cm, the results match the Friis equation [25] well, and the calculated EIRP is around −10 dBm. In Fig. 15(b), the phase noise of all channel outputs measured by down-converting them into IF signals is shown. At 1-MHz offset, the phase noise, which is mainly limited by the multiplied phase noise of the LO signal for VDI extender, is about −100 dBc/Hz on average. In Fig. 15(c), the measured radiation pattern of the chip (Channel-3), again without the TPX lens, is shown, which has a 3-dB beamwidth of ~90° and well matches the simulated result in Fig. 7(c). Finally, by turning on the THz transceivers one-by-one and by sweeping the input RF frequency (13.75–15 GHz), the measured EIRP of each channel is shown in Fig. 16. The peak multi-channel-aggregated EIRP of the radar[3] (without lens) is 0.6 dBm, and it is evident that with the THz comb architecture, the fluctuation of the EIRP across the entire 100-GHz bandwidth is only 8.8 dB. With the TPX lens, the multi-channel aggregated EIRP increases significantly to ~20 dBm.

Next, to measure the detection sensitivity of the radar chip, a setup shown in Fig. 14(b) is used. The VDI WR-3.4 VNA extender is configured in the transmitter mode and its output radiated from a horn antenna is again calibrated by the Erickson PM5 power meter. The IF output ($f_{IF} = 4$ MHz) of each radar channel is measured by a spectrum analyzer. Again, the measured output power by placing the horn antenna

[3]Although the output waves of the channels are not coherent, the multi-channel aggregated EIRP is still a meaningful metric for a fair comparison with prior single-tone radars, in terms of the equivalent signal-to-noise ratio (with the same integration time), detection distance, and energy efficiency.

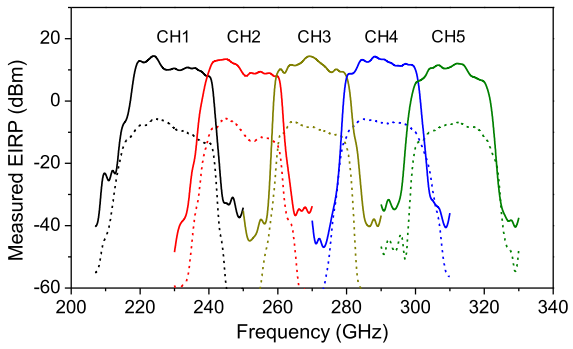


Fig. 16. Measured EIRP of each radar channel with (solid line) and without (dashed line) the TPX lens.

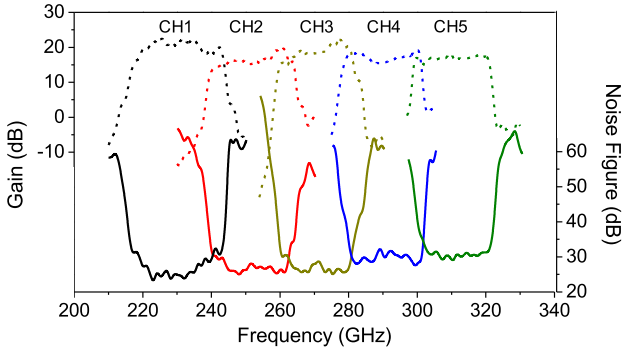
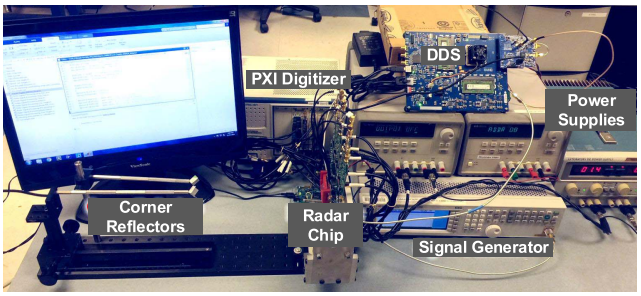
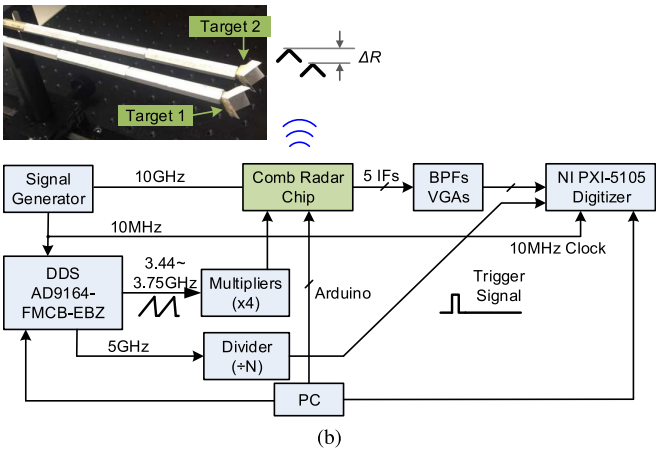


Fig. 17. Measured conversion gain (dashed lines) and SSB NF (solid lines) of each radar channel without the TPX lens.



(a)



(b)

Fig. 18. (a) Photograph and (b) block diagram of the setup used for the testing of radar ranging capability.

vertically and horizontally is added together. To quantify the conversion gain of the chip receiver, we derive the radiation power impinging on each chip antenna as

$$P_R|_{\text{dBm}} = P_{\text{TX}}|_{\text{dBm}} + G_{\text{TX,ant}}|_{\text{dBi}} + 20\log_{10}\frac{\lambda}{4\pi d} + D_R\Big|_{\text{dBi}} \tag{9}$$

where P_{TX} and G_{TX} are the output power and antenna gain of the VDI extender source, respectively, and D_R is the directivity of the chip antenna (7 dBi). The conversion gain of each receiver channel is therefore

$$G_C|_{\text{dB}} = P_{\text{IF}}|_{\text{dBm}} - P_R|_{\text{dBm}} \tag{10}$$

where P_{IF} is the IF output power of the chip. Based on (10), the measured results without using the TPX lens are shown in Fig. 17. Note that this conversion gain, with a peak value of 22 dB, includes the amplification of the receiver baseband buffer and the antenna efficiency of ~20%. Finally, the baseband output noise floor P_N of each receiver channel is measured, which then gives the SSB NF of the chip by using the gain method

$$NF|_{\text{dB}} = P_N|_{\text{dBm/Hz}} - (-174|_{\text{dBm/Hz}}) - G_C|_{\text{dB}} \tag{11}$$

which is plotted in Fig. 17. The minimum measured NF (again including the baseband amplifier and antenna loss) is 22.2 dB, and its fluctuation across the 100-GHz bandwidth is 14.6 dB.

B. Radar Demonstration and Characterization

To realize ranging detection, the input FMCW chirp signal is generated by a DDS (AD9164-FMCB-EBZ) and a multiplier chain, as shown in Fig. 18(b). The five radar IF outputs are acquired synchronously by a multi-channel digitizer (NI PXI-5105) and then calibrated and stitched by MATLAB in a PC. Similar to the operation of conventional FMCW radars, over-chirping is applied in the generation of the sawtooth FM signal in the DDS to ensure that the entire channel bandwidth (ΔB = 20 GHz in Fig. 3) is covered without the impact of the ramping-down portion of the sawtooth signal. Accordingly, in MATLAB, the IF data sections outside the duration of ΔB is clipped off (see Fig. 3). Note that the IF stitching in Fig. 3 only requires precise ΔB and ΔT; such conditions are ensured by the global 10-MHz clock signal in Fig. 18(b), which synchronizes the DDS (with a DDS chirping slope of 625 MHz/μs) and the PXI digitizer (with ΔT = 32 μs). Also, note that (4) in Section II shows the starting points of the ΔT clipped sections of IF data that do not need to be precise; they only need to be identical across all five channels.

Similar to conventional FMCW radars, signal calibration is applied before the IF stitching, in order to correct a few systematic non-idealities associated with the circuit implementation. First, due to the fluctuations in TX power (see Fig. 16) and RX gain (see Fig. 17), the IF signal strength has non-flat frequency response inside each channel and mismatches among different channels; this results in amplitude

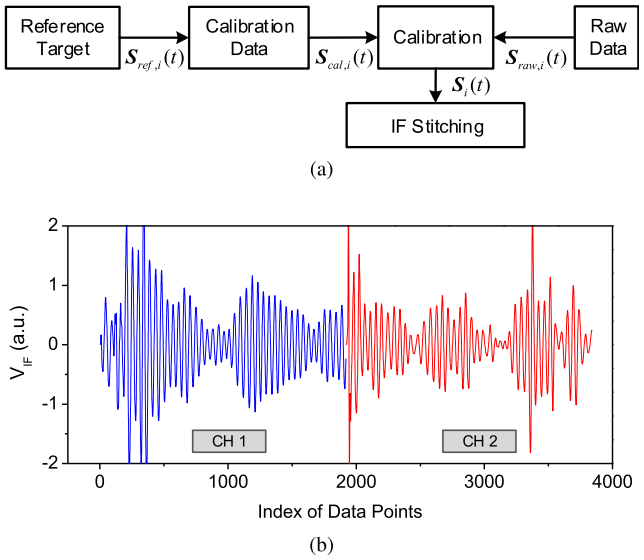


Fig. 19. (a) FMCW radar signal calibration process. (b) Example of a section of calibrated and stitched data for two corner reflectors spaced with a distance of $\Delta R = 19$ mm.

modulation of the IF signal during chirping and spectrum broadening after performing the FFT [26], [27]. Second, there are two sources of delay (phase) mismatches among the channels: one is from the antenna and matching network, and the other one is from the different locations of antennas on the chip. The latter can be ignored when the object is right in the front of radar and with sufficiently large distance (>20 cm). To detect objects in other directions, a phase gradient similar to that in a linear phased array should be applied. Third, any chirp nonlinearity will also cause IF spectrum broadening [28]. Finally, the amplitude fluctuations of TX signal can be directly rectified and down-converted by the square-law mixer in the RX and generate a low-frequency false signal; fortunately, it can be filtered out by the high-pass filter in the RX as mentioned earlier. To address the aforementioned gain and phase mismatches, as well as the spectrum-broadening problems, a calibration method derived from [28] and shown in 19(a) is adopted. A single-point-like target (i.e., a corner reflector in our experiment) is used as the reference target to generate the calibration data for each channel. Assume that $\boldsymbol{S}_{\text{ref},i}(t)$ is the Hilbert transform of the ith-channel reference IF signal, and the ith-channel calibration data $\boldsymbol{S}_{\text{cal},i}$ is

$$\boldsymbol{S}_{\text{cal},i}(t) = \boldsymbol{S}_{\text{ref},i}(t) \cdot e^{-j\left(2\pi \overline{f}_{\text{IF}} t + 2\pi \overline{f}_{\text{IF}} \Delta T(i-1) + \varphi_1\right)} \tag{12}$$

where $\overline{f}_{\text{IF}}$ is the mean target frequency of $\boldsymbol{S}_{\text{ref}}$ and φ_1 is the phase of $\boldsymbol{S}_{\text{ref},1}$. Therefore, the aforementioned non-idealities of raw data, $\boldsymbol{S}_{\text{raw},i}$, can be one-time calibrated by $\boldsymbol{S}_{\text{cal},i}$, and the calibrated IF signal is

$$\boldsymbol{S}_i(t) = \boldsymbol{S}_{\text{raw},i}(t) / \boldsymbol{S}_{\text{cal},i}(t). \tag{13}$$

Finally, the calibrated IF signals are stitched in the time domain.

A set of corner reflectors are measured to verify the IF stitching process after the signal calibration. Fig. 19(b) shows the waveform of two corner reflectors with the data of two

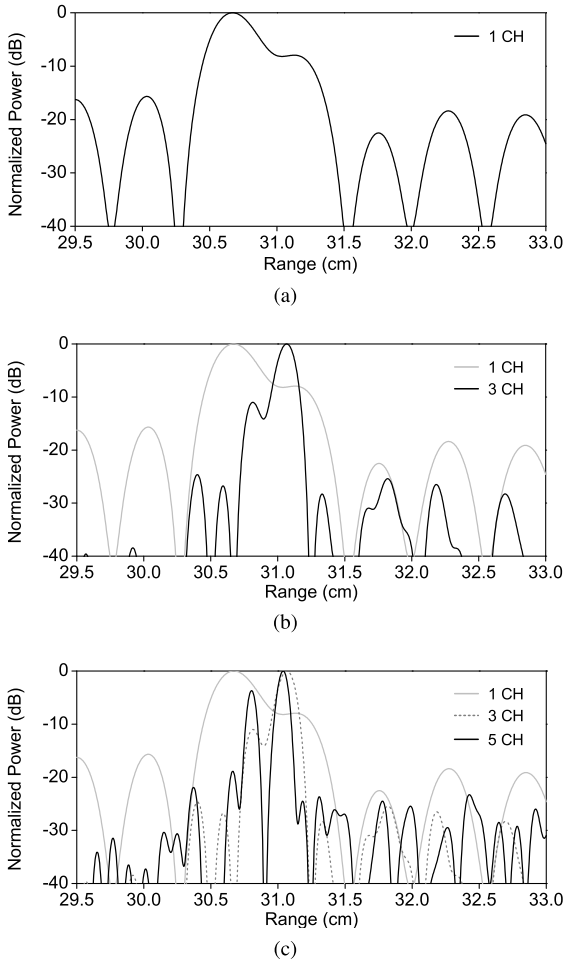


Fig. 20. Measured FFT results (Hamming window) of two corner reflectors ($\Delta R = 2.5$ mm) with IF data from (a) one, (b) three, and (c) five channels.

radar channels. It can be seen that the modulated envelope of IF signal, which stems from two closely spaced IF tones representing the two objects, is continuous over the stitched channels; the extended periods of that envelope (hence higher FFT resolution) due to stitching, therefore, help to distinguish those two tones in the IF spectrum. Two corner reflectors are used to measure the range resolution of the comb radar. In order to see the two separated spectrum peaks clearly with 100-GHz bandwidth and Hamming window (broadening factor is 1.5), these two corner reflectors have a 2.5-mm range difference, so the corresponding separable range difference without windowing is 1.67 mm. Fig. 20 shows the improvement of the range resolution in comb radar: a single channel [BW = 20 GHz, see Fig. 20(a)] is unable to resolve the objects; with the stitching of three adjacent channels [BW = 60 GHz, see Fig. 20(b)], the object separation starts to show; and with all five channels stitched together [BW = 100 GHz, see Fig. 20(c)], the separation becomes distinct. It also indicates that the resolution limit is still not reached in Fig. 20(c). The linewidth of the windowed IF lobe corresponds to a value very close to the theoretical windowed resolution of 2.25 mm or the theoretical bandwidth-limited resolution of 1.5 mm.

Finally, the accuracy of the ranging detection is measured by using one corner reflector at a varying distance of 30–200 cm

TABLE I

SUMMARY OF THE CHIP PERFORMANCE AND COMPARISON WITH OTHER STATE-OF-THE-ART BROADBAND RADARS IN SILICON

References	Technology	Frequency (GHz)	Bandwidth (GHz)	Resolution (mm)[a]	Output EIRP (dBm)	Minimum NF (dB)	EIRP & NF Fluctuation (dB)	Chip Size (mm^2)	DC Power (mW)
T-THz 2018 [1]	130-nm SiGe	305∼375	70	2.1	6, 18.4[b]	19.7	10.5 & 28.6	2.85	1700
T-MTT 2019 [2]	55-nm SiGe	189.9∼252.3	62.4	2.4	14[c]	NA	7.7 & NA	0.51	87
JSSC 2014 [4]	65-nm CMOS	157.9∼164.9	7	21	18.8	22.5	3 & NA	20	2200
ISSCC 2019 [5]	28-nm CMOS	138∼151	13	11.5	11.5	4[d]	1.5 & 4	6.5	500
T-THz 2016 [14]	130-nm SiGe	210∼270	60	2.5	32.8[c]	21	20 & 29	3.2	1800
This Work	65-nm CMOS	220∼320	100	1.5	0.6[e], 20[e]	22.2	8.8 & 14.6	5	840

[a] Theoretical resolution determined by $\frac{c}{2 \cdot BW}$ (c: speed of light). [b] With TPX lens. [c] With silicon lens.
[d] Effective isotropic NF including the antenna directivity. [e] Multi-channel aggregated EIRP.

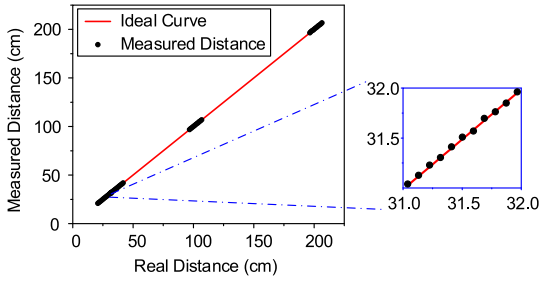


Fig. 21. Measured ranging accuracy of the comb radar.

on a linear stage. As shown in Fig. 21, the measured values agree well with the real distances. The range accuracy with 0.32-ms integration time is within 0.2 mm, which is limited by the reference rule.

V. CONCLUSION

Although it is challenging to achieve high fractional bandwidth in THz sensing microsystems, the circuit down-scaling due to the increasing frequency opens up the opportunity in a single-chip integration of multi-tone transceiver arrays for high-parallelism spectral coverage. Such a comb architecture breaks the conventional tradeoffs among bandwidth, performance, and efficiency. The radar chip presented in this article showcases that advantage. Table I summarizes its performance and comparisons with the other state-of-the-art broadband radars in silicon. This work marks the first CMOS implementation of FMCW radars operating above 200 GHz, as well as the largest bandwidth. More importantly, although the SiGe counterparts [1], [14] have wide bandwidth and high EIRP, their EIRP and NF fluctuation are higher than that of the presented radar which are 8.8 and 14.6 dB across the 100-GHz bandwidth, respectively.

The presented THz-comb sensing scheme multiplies the amount of hardware (amplification, filtering, data sampling, and so on) needed at the baseband. However, due to the increased equivalent FMCW chirping speed, the overall energy efficiency is not degraded. This additional hardware overhead is also expected to significantly shrink with more advanced CMOS technology nodes. Note that $f_{\max}$ of the 65-nm CMOS process used in this work is only 280 GHz; with the recent development of FinFET ($f_{\max} = 450$ GHz in [29]) and FDSOI ($f_{\max} = 370$ GHz in [30]) CMOS technologies, the EIRP and NF are expected to improve significantly, too, which further make low-THz radar sensing more practical for emerging applications that require higher resolution and smaller form factor.

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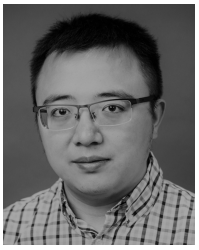

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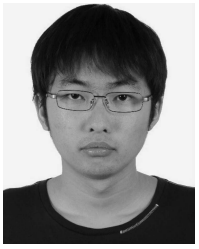

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