11.9 A 105Gb/s Dielectric-Waveguide Link in 130nm BiCMOS Using Channelized 220-to-335GHz Signal and Integrated Waveguide Coupler

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The rapid surge of data transmission within computation, storage and communication infrastructures is pushing the speed boundary of traditional copper-based electrical links. Recent realizations of 100Gb/s wired links require advanced FinFET technologies, high-cost packaging/cables and power-consuming equalization. High-frequency waves over dielectric waveguides have been considered as an alternative solution that exploits the low-loss, broadband medium while maintaining compatibility with existing silicon IC platforms. However, since its debut in 2011 [1], this scheme, previously using ≤140GHz carriers, has only achieved data rates of up to 36Gb/s [2]. It is expected that higher carrier frequencies (e.g. >200GHz) and multi-channel aggregation would further increase the data rate while shrinking the interconnect size; but that scheme has been hindered by challenges related to the required high-order multiplexer and ultra-broadband waveguide coupler operating efficiently at sub terahertz (sub-THz) frequencies. In this paper, using a 130nm SiGe BiCMOS technology, we present a multi-channel, multiplexer/coupler-integrated transmitter (Tx) that delivers a data rate of 105Gb/s (3×35Gb/s). To demodulate each channel, a 35Gb/s coupler-integrated receiver (Rx) is also developed. Our link, including the chipset and a 0.4mm-wide, 30cm-long dielectric ribbon, experimentally demonstrates the potential speed, efficiency, size and cost advantages of THz fiber links in high-speed inter-server and backplane fabrics.

The architecture of the Tx is shown in Fig. 11.9.1. It divides a band ranging from 220 to 335GHz into three 35GHz-wide channels. Two 5GHz-wide guard bands are inserted to ensure isolation between adjacent channels. The Tx consists of three sub-harmonic LO paths generating signals at f_{LO}=110, 130 and 150GHz. The 130GHz signal is obtained from a frequency tripler with a 43.3GHz input, and is then amplified by three cascode power amplifier stages. Part of the 130GHz power is diverted to the other two LO paths, which utilize single-sideband mixers to shift the input tones by ±20GHz to generate signals at 110 and 150GHz. To reduce the circuit size and power consumption, the frequency doubling for the link-carrier generation (at 220, 260 and 300GHz) and the data modulation are realized within a single component (Fig. 11.9.2). A push-push structure (T_7-T_8) is adopted for the second-harmonic generation. The tail current of the transistor pair is switched by the incoming data stream via T_9, hence realizing OOK modulation of the THz carrier. The capacitor C_1 is chosen to be sufficiently large so that when T_7 and T_8 are active, it acts as a current path at $2f_{LO}$ in order to increase the frequency conversion efficiency; meanwhile it is small enough to still allow for up to 35GHz modulation of the tail current. The NPN devices T_7~T_9 are biased by a PMOS T_{10} through a dumbbell broadband stop structure, which isolates the large parasitic capacitance of T_{10} from the THz output path. The doubler-modulator module consumes 22mW of power, and with ~0dBm input LO, its output power is around -12dBm with ~3dB fluctuation across the 35GHz modulation frequency range (Fig. 11.9.2).

A high-Q triplexer, based on three hairpin filters, is implemented on the chip (Fig. 11.9.2). It not only prevents the injection of THz carrier power into the closely-spaced channels, but also suppresses the lower sideband spectrum of the modulated output for improved spectral efficiency. Traditional high-order filter topologies with rapid roll-off adopt cascaded resonators, which cause excessive loss at THz frequencies. Our hairpin filter utilizes four quarter-wave, twist-modified split-ring resonators that are placed adjacent to each other. The resultant one-to-all electric and magnetic couplings, through inter-resonator capacitance and inductance respectively, reduce the filter size and loss. A quasi-elliptical filter response is implemented with three passband poles and four stopband zeros. For verification, three standalone triplexer test structures are fabricated, allowing for separate tests of the three channel filters. The results (Fig. 11.9.2) agree well with the simulation, showing a 3dB pass bandwidth of 30~35GHz and 10~30dB stop-band rejection. Finally, the multi-channel-aggregated output is coupled into a dielectric ribbon (Rogers R3006, 0.4×0.25mm^2 of cross-section) through an integrated waveguide coupler (Fig. 11.9.3) [4]. The dielectric ribbon is sized to operate in a single-mode regime in the excited horizontal polarization. The coupler is based on a differential substrate-integrated-waveguide (SIW) structure, which turns a microstrip input signal into a leaky travelling wave that is exposed to the dielectric ribbon through the slot of the SIW. As the wave propagates in the longitudinal direction, it gradually couples to the EH_1 hybrid mode of the dielectric waveguide. The SIW cross section is tapered (from W_{C1}=364μm to W_{C2}=204μm in Fig. 11.9.3) to present an increasing characteristic impedance; this further boosts the coupling and decreases the length of the coupler to 750μm. Compared to prior works [1,2,5,6], this coupling scheme eliminates the lossy THz-signal routing to off-chip couplers/radiators, and enables a planar waveguide placement with a direct contact to the chip edge. In the simulation (Fig. 11.9.3), the coupler exhibits a low insertion loss of 2.5~6dB across the entire 220~340GHz band.

To form a complete all-silicon link with the Tx, a single-channel Rx integrating the same waveguide coupler is implemented using the 130nm BiCMOS process. Shown in Fig. 11.9.3, T_{15}~T_{17} form an active balun, with full-band matching, that converts the single-ended THz input from the coupler into a pair of differential currents. To downconvert the sub-THz energy to baseband, these currents are injected into four resistively loaded switching transistors T_{11}~T_{14}, which are driven by an externally applied LO signal. Through a three-stage buffer pair, the recovered data is amplified and extracted at the output. The above THz down-conversion mixer operates across a broad band. In the experiment, the applied LO is selected to be at 220, 260 and 300GHz and manually tuned for phase coherence with the Tx, so that each transmitted channel is tested. Future multi-channel receivers to be developed will include the same triplexer as that in Fig. 11.9.2, as well as separate Rx circuits shown in Fig. 11.9.3 for each channel.

The fabricated Tx and Rx chips are 2.4×3.9mm^2 and 0.9×0.9mm^2 in size. The assembly of the link is shown in Fig. 11.9.4, where a dielectric ribbon is directly bonded with low permittivity epoxy on top of the two chips. Unlike optical links, no precise waveguide-chip alignment is required in this assembly. Link lengths of 5cm and 30cm are chosen, which are ultimately limited by the available space of the assembly and fragility of the thin ribbon, rather than the link budget. The test setup is also shown in Fig. 11.9.4. To include the impact of inter-channel interference, two PRBS-7 generators simultaneously drive both the channel under test and an adjacent channel of the Tx chip. On the Rx side, a VDI WR3.4GX-M source provides the THz LO signal through a Cascade probe. LO frequencies of 220, 260 and 300GHz are applied respectively to test the transmission in Channel 1~Channel 3. Only one of the differential outputs of the Rx (hence 3dB lower SNR) is measured by a single-ended high-speed oscilloscope. In Fig. 11.9.5, the eye diagrams of the three channels running at 35Gb/s are shown. Without any equalization, the three-channel bit-error rate (BER) is ≤5×10^{-9} for the 5cm distance, and ≤5×10^{-8} for the 30cm distance. With a reduced channel data rate of 30Gb/s, the BER is improved to <10^{-12}. Lastly, by extending one end of the fiber into a WR-3 horn antenna feeding an Erickson PM5 power meter, the peak output power of the Tx channels is measured to be -24dBm. The DC power of the Tx and Rx are 256mW and 73mW, respectively. The energy efficiency of the Tx is 2.4pJ/b. A future inclusion of a 40GHz/20GHz PLL (for the carrier generator) with typically tens of mW of DC power [7] would increase the above value to ~3pJ/b. Shown in Fig. 11.9.6, this link has 3× higher data rate than prior art and has the smallest interconnect size due to its integrated coupler and the small dimension of the THz dielectric waveguide. Future applications of the work include medium-reach (meter-level) datacentric interconnects with high speed and low latency, as well as lightweight communications within autonomous cars, drones and other aeronautical vehicles.

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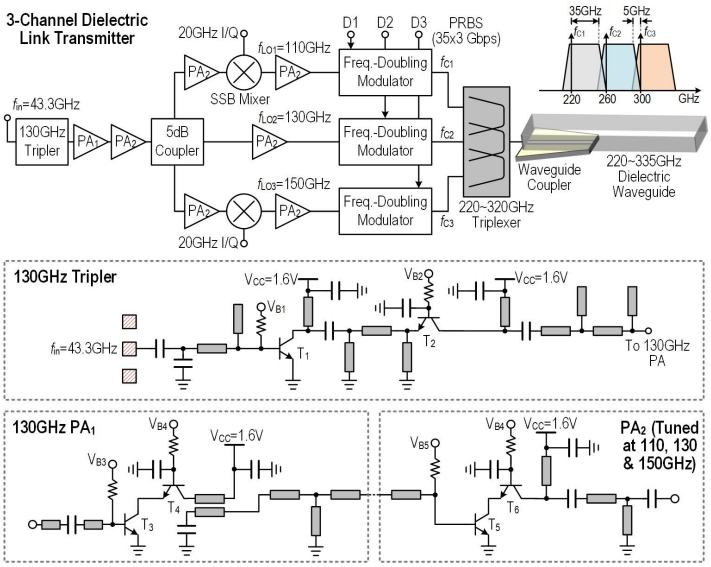


Figure 11.9.1: (Top) system diagram and (bottom) the multiplier and amplifier chain for LO generation.

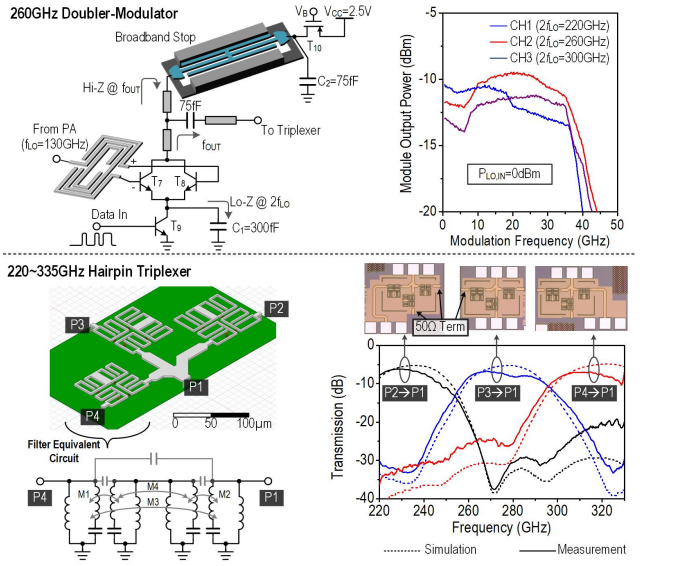


Figure 11.9.2: (Top) design of the 260GHz doubler-modulator, and (bottom) the design, simulation and measurement of the 220~335GHz hairpin triplexer.

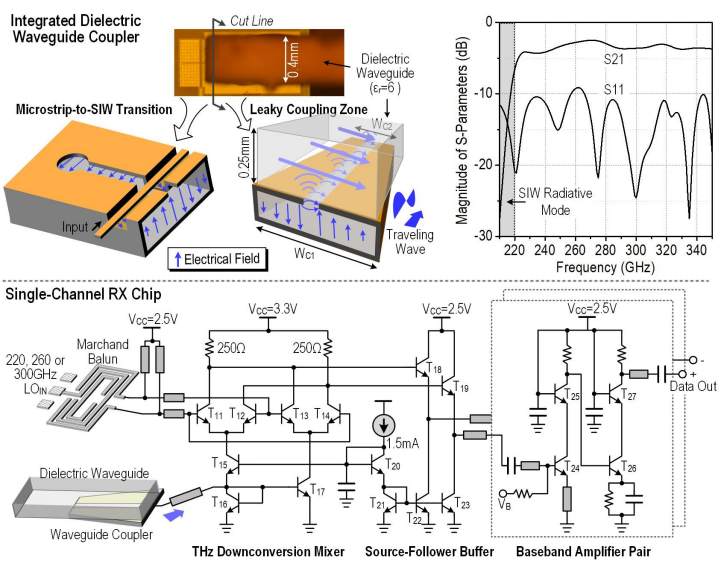


Figure 11.9.3: (Top) the integrated waveguide coupler and simulation results. (Bottom) schematic of the coupler-integrated, single-channel link receiver.

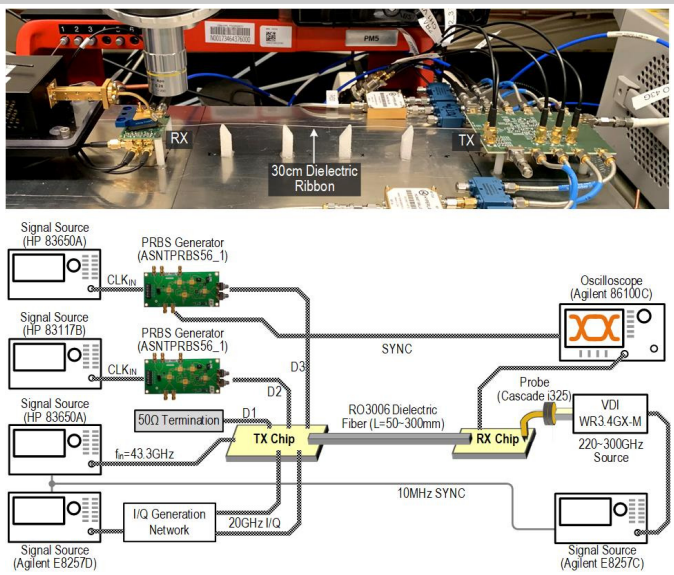


Figure 11.9.4: (Top) photo of the link with a 30cm dielectric waveguide connecting the Tx and Rx chips. (Bottom) the block diagram of the link testing setup.

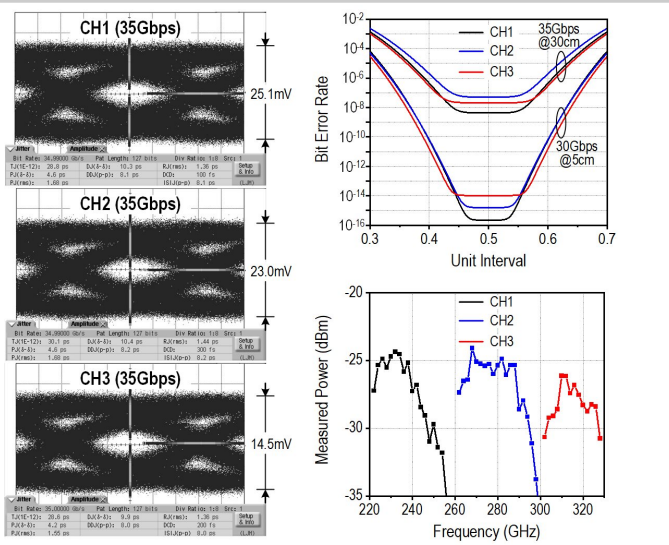
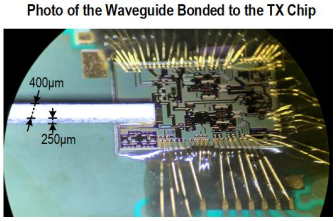
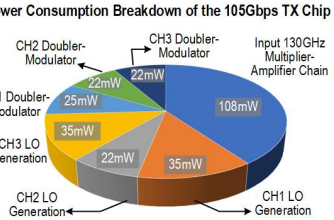


Figure 11.9.5: (Left) measured eye diagram of the 30cm link with an aggregated data rate of 3x35Gb/s, (top right) the measured BER, and (bottom right) the measured output power of each channel.

Photo of the Waveguide Bonded to the TX Chip



Power Consumption Breakdown of the 105Gbps TX Chip



Comparison with Prior Dielectric Waveguide Links

	Technology	Carrier Frequency (GHz)	Data Rate (Gbps)	BER	Fiber Coupler	Fiber Size (W×H, mm)	Demonstrated Link Length (cm)	TX DC Power & Efficiency	RX DC Power & Efficiency
JSSC 2011 [1]	40nm CMOS	57, 80	12.5+12.5†	<10^{-12}	Quasi Yagi (Off-Chip)	8×1.1	120	56mW 2.2pJ/bit	87mW 3.5pJ/bit
SSC-L 2018 [2]	55nm SiGe	130	36	<10^{-8} @25Gbps	Vivaldi (Off-Chip)	1.3×1.3	100	216mW†† 6pJ/bit	No RX
ESSCIRC 2016 [5]	40nm CMOS	120	17.7	<10^{-12}	Tapered Slot (Off-Chip)	2 (Circular)	100	11.1mW 0.63pJ/bit	59.6mW 3.4pJ/bit
JSSC 2019 [6]	28nm CMOS	140	12	<10^{-12}	CPW-WG Transition (Off-Chip)	1.9×1.0	100	65mW 5.4pJ/bit	165mW 13.8pJ/bit
This Work	130nm BiCMOS	220, 260 & 300	35×3‡	5×10^{-8}	Leaky SIW (Integrated)	0.4×0.25	30	256mW††, 73mW‡‡, 2.4pJ/bit	2.1pJ/bit
			30×3‡	<10^{-12}					

† Full-duplex transmission (12.5Gbps each way)
†† Input signal sources (16.25GHz in [2], 43.3 & 20GHz in this work) not included
‡ The link is demonstrated with a three-channel TX and one-channel RX
‡‡ LO source (220~300GHz) not included

Figure 11.9.6: (Top) fiber connection and power consumption breakdown of the Tx chip, and (bottom) a comparison with other dielectric-waveguide links.

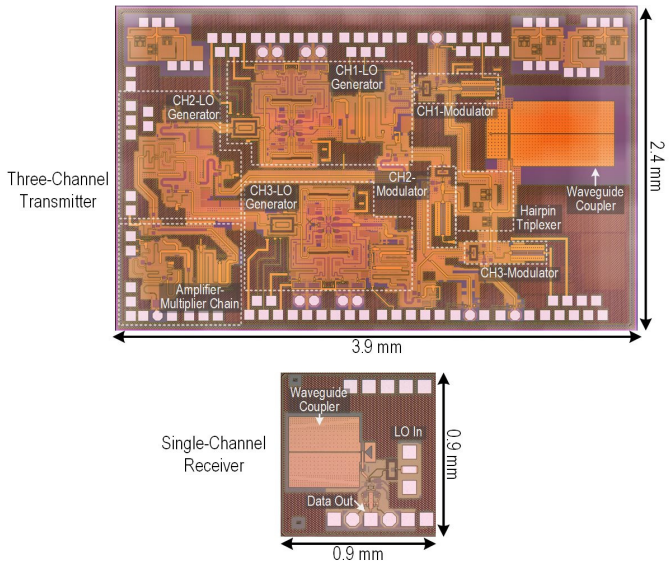


Figure 11.9.7: Die micrographs of the 3-channel transmitter and the single-channel receiver.

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