A 110-to-130GHz SiGe BiCMOS Doherty Power Amplifier with Slotline-Based Power-Combining Technique Achieving >22dBm Saturated Output Power and >10% Power Back-Off Efficiency

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Self Introduction

Xingcun Li

- **Ph.D. student (2017-Present)**

Tsinghua University, Beijing, China

- **Visiting student (2020)**

Massachusetts Institute of Technology (MIT), Boston, MA

- **B.S. degree (2013-2017)**

University of Electronic Science and Technology of China (UESTC), Chengdu, China

- **Research interests**

Silicon-based mm-Wave and THz integrated circuits for radar and wireless communication.

Outline

- Motivation
- Power Combining Doherty PA Architecture
- Slotline-based Power Combiner
- Circuit Implementation
- Measurements
- Conclusion

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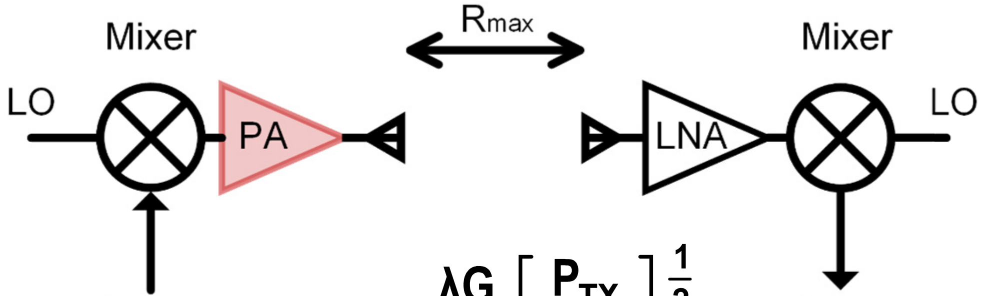
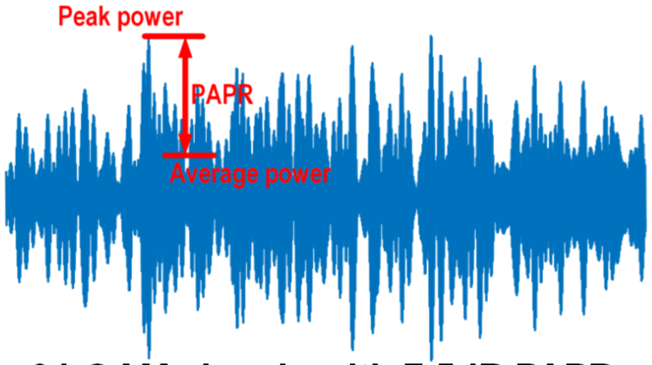
Motivation

- Beyond 5G, the increasing demand for 100+Gbps data rates requires a **broad available spectrum**. **(D-band is attractive)**
- High output power (P_{TX}) is required for a large link distance. **(The high output power amplifier (PA) plays an important role)**
- Peak and power back-off (PBO) efficiency enhancement is desirable for **high peak-to-average power ratio (PAPR) signals. (PBO efficiency needs to be improved)**

[Smartcitiesworld.net]



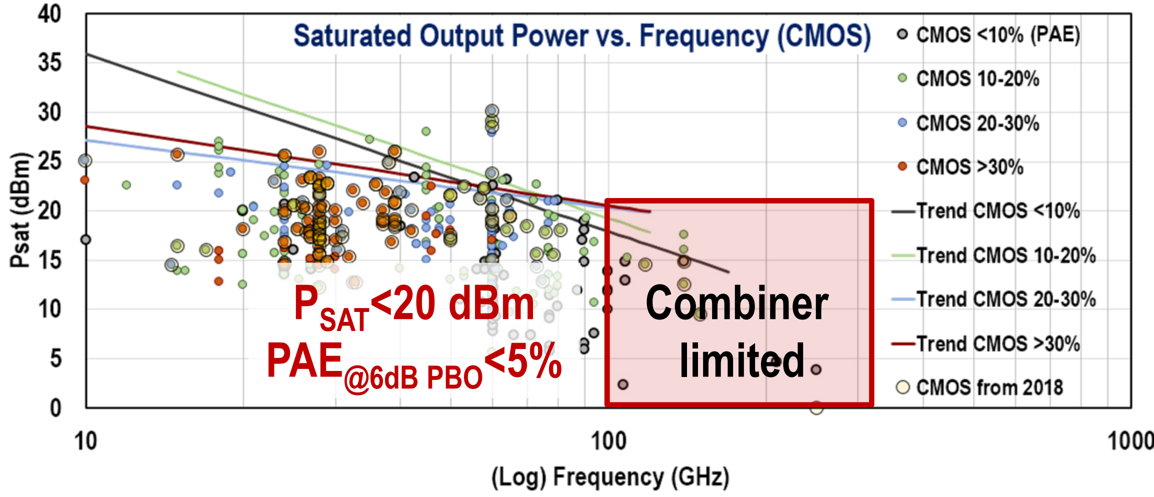
$$R_{max} = \frac{\lambda G}{4\pi}\left[\frac{P_{TX}}{S_{min}}\right]^{\frac{1}{2}}$$



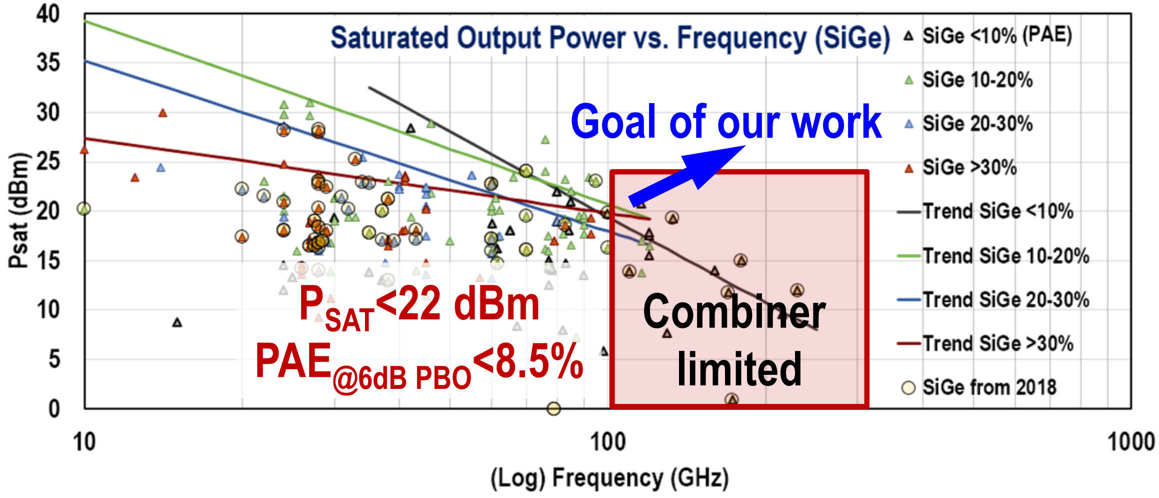
64-QAM signals with 7.5dB PAPR

Motivation

- **Existing silicon-based sub-THz PA solutions**
  - ✓ High integration with other blocks
  - ✓ Low-cost
  - X Limited output power P_{OUT}
  - X Limited peak/PBO efficiency



- **Emerging solutions for sub-THz PA**
  - ➢ Low-loss power combining technique with PBO efficiency enhancement



[H. Wang et al., Power Amplifiers Performance Survey 2000-Present]

Motivation

- **PBO efficiency enhancement techniques**

<table>
<tr><th>Outphasing PA</th><th>Envelope tracking PA</th><th>LMBA</th><th>Conventinal Doherty PA</th></tr>
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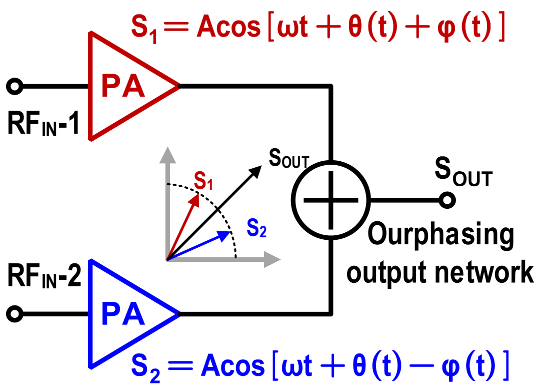
<td>
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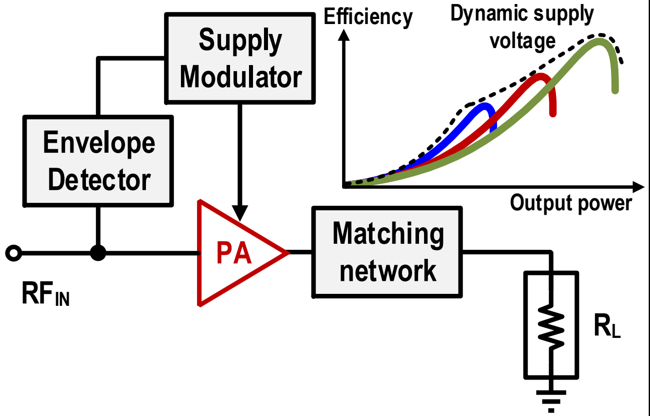
<td>
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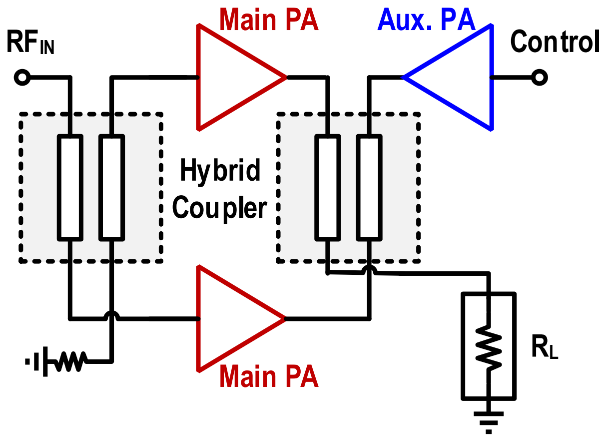
<td>
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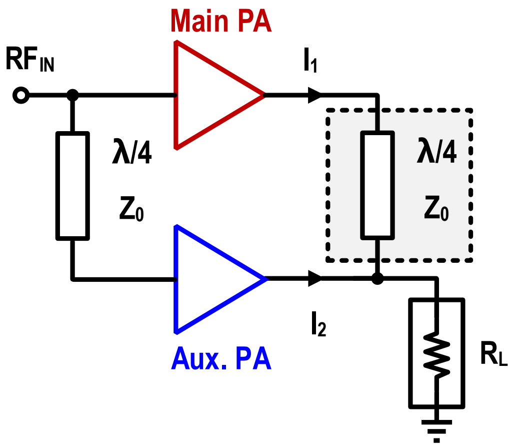
<td>
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<tr>
<td>X Dual input
X Narrow bandwidth
X Baseband overhead</td>
<td>X Complexity
X Limited modulation bandwidth
X Inefficient supply modulator</td>
<td>X Limited bandwidth
X High loss of coupler
X Area overhead (90º Hybrid)</td>
<td>X Narrow bandwidth
X Area overhead (λ/4 T-line)</td>
</tr>
<tr>
<td>[B. Rabet et al., ISSCC, 2018]
[S. Li et al., ISSCC, 2020]</td>
<td>[Z. Popovic, Microw. Mag., 2017]</td>
<td>[D. Shepphard et al., MWCL,2016]
[V. Qunaj et al., ISSCC, 2021]</td>
<td>[E. Kaymaksut et al., T-MTT, 2015]
[F. Wang et al., JSSC, 2019]</td>
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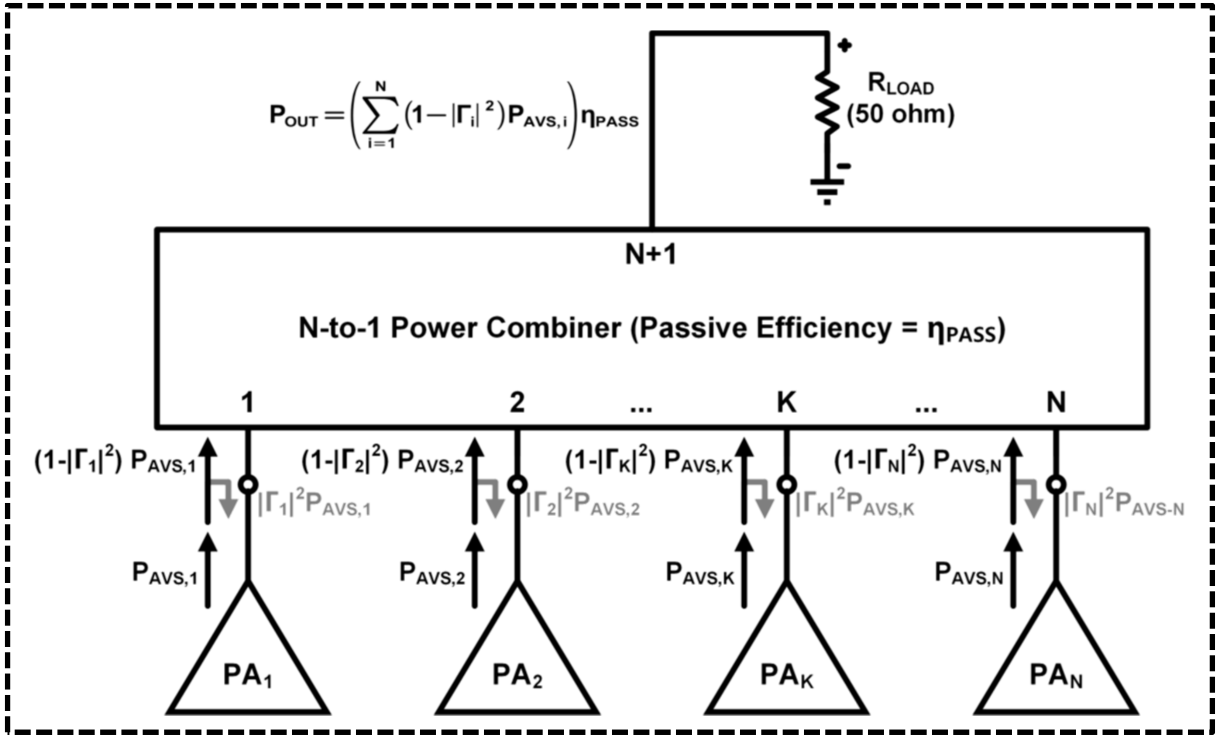
Motivation

- **Low-loss power combiner/matching networks**

Power combining network



[X. Li et al., JSSC, 2021]

Two factors affect the power loss:

- Reflection at the input port:

$$\Gamma_i = \frac{Z_{IN,i} - Z_{OPT}}{Z_{IN,i} + Z_{OPT}^*} \rightarrow$$

Impedance Matching
&
Port Imbalance

- Passive efficiency (η_{PASS}) of the combiner:
  - ☐ Conductor loss
  - ☐ Dielectric loss
  - ☐ Radiation loss

Combiner Structure

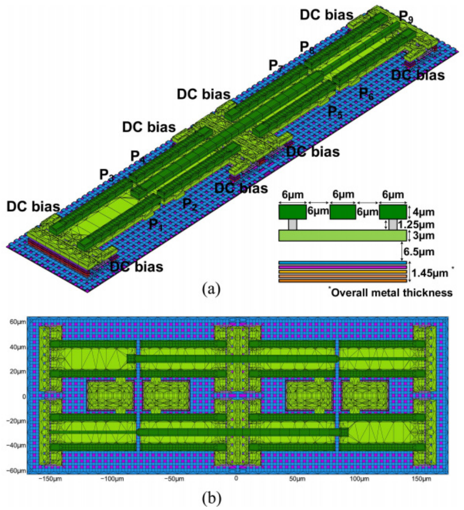
Motivation

- **Existing silicon-based sub-THz power combiner**

☺ Low-loss combining

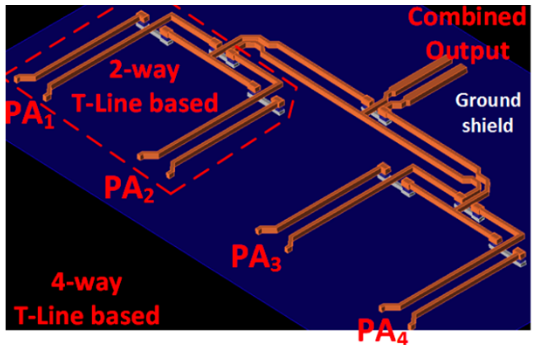
☹ No PBO efficiency enhancement

Three-conductor combiner



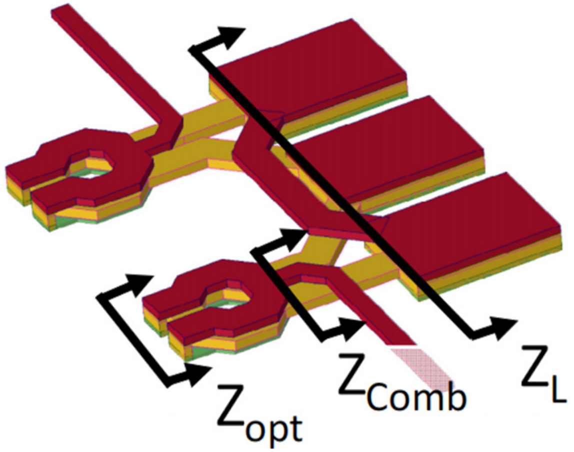
[S. Daneshgare et al., T-MTT, 2018]

Zero-degree combiner



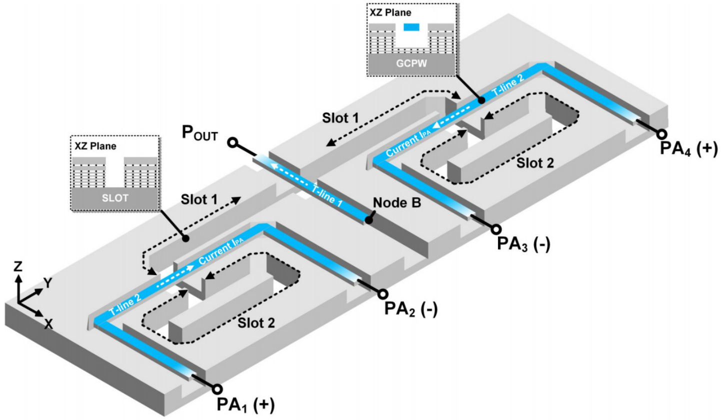
[M. Eissa et al., ISSCC, 2019]

Transformer-based combiner



[B. Philippe et al., ISSCC, 2020]

Slotline-based combiner



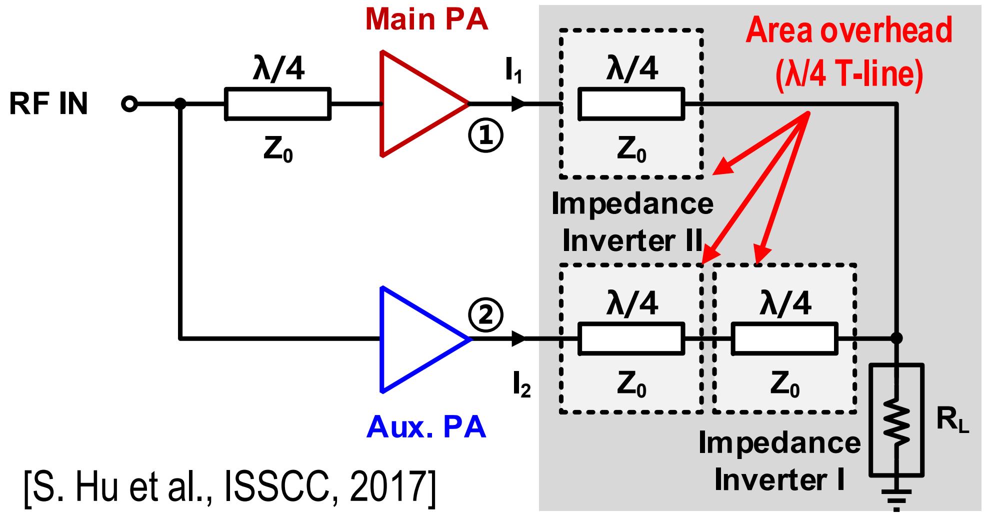
[X. Li et al., JSSC, 2021]

Outline

- Motivation
- **Power Combining Doherty PA Architecture**
- Slotline-based Power Combiner
- Circuit Implementation
- Measurements
- Conclusion

Power Combining Doherty PA Architecture

- Broadband Doherty PA with two impedance inverters



[S. Hu et al., ISSCC, 2017]

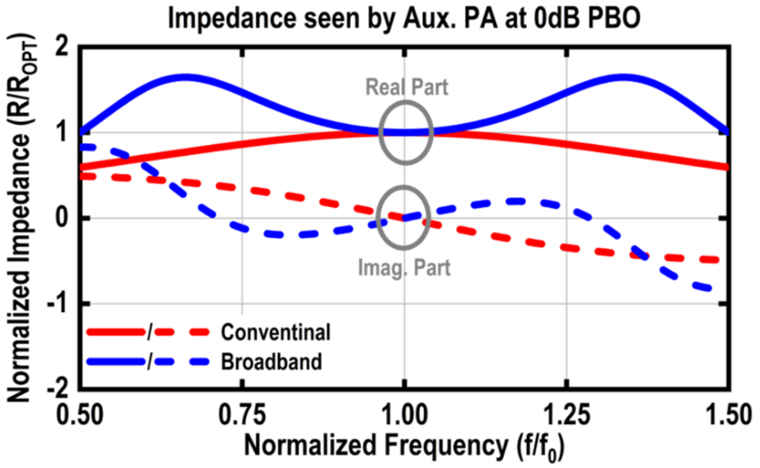
For Symmetrical PA：

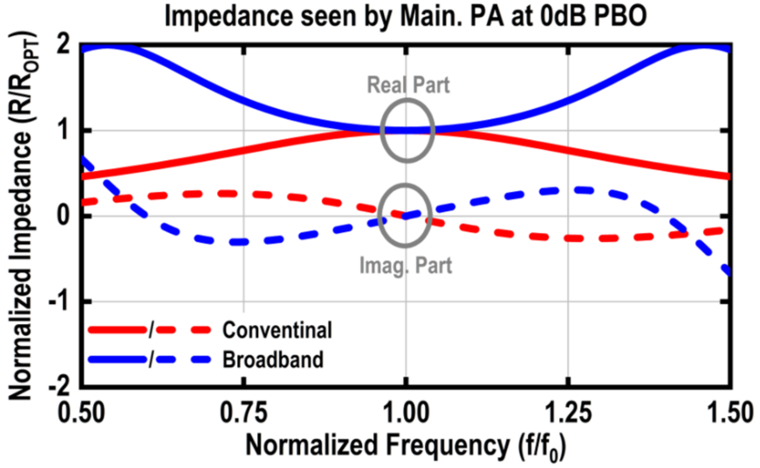
- 6-dB PBO (I_2=0):

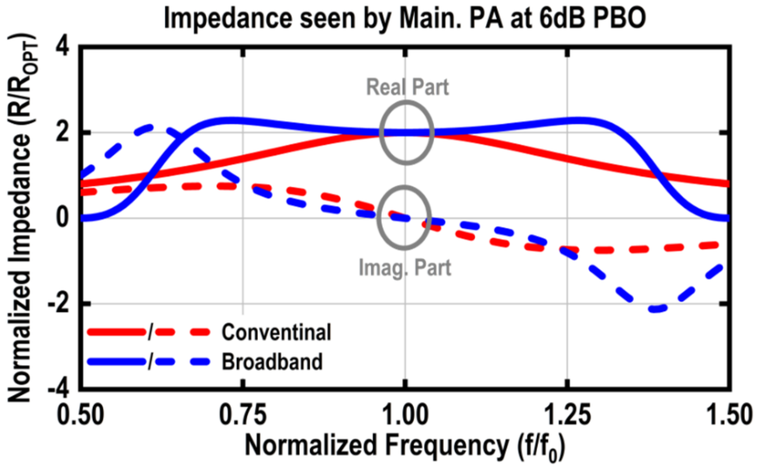
$$\begin{cases} Z_{IN1} = \frac{Z_0^2}{R_L} = 2R_{OPT} \\ Z_{IN2} = \infty \end{cases}$$

- 0-dB PBO (I_2=jI_1):

$$\begin{cases} Z_{IN1} = \frac{Z_0^2}{R_L} - Z_0 = R_{OPT} \\ Z_{IN2} = Z_0 = R_{OPT} \end{cases}$$

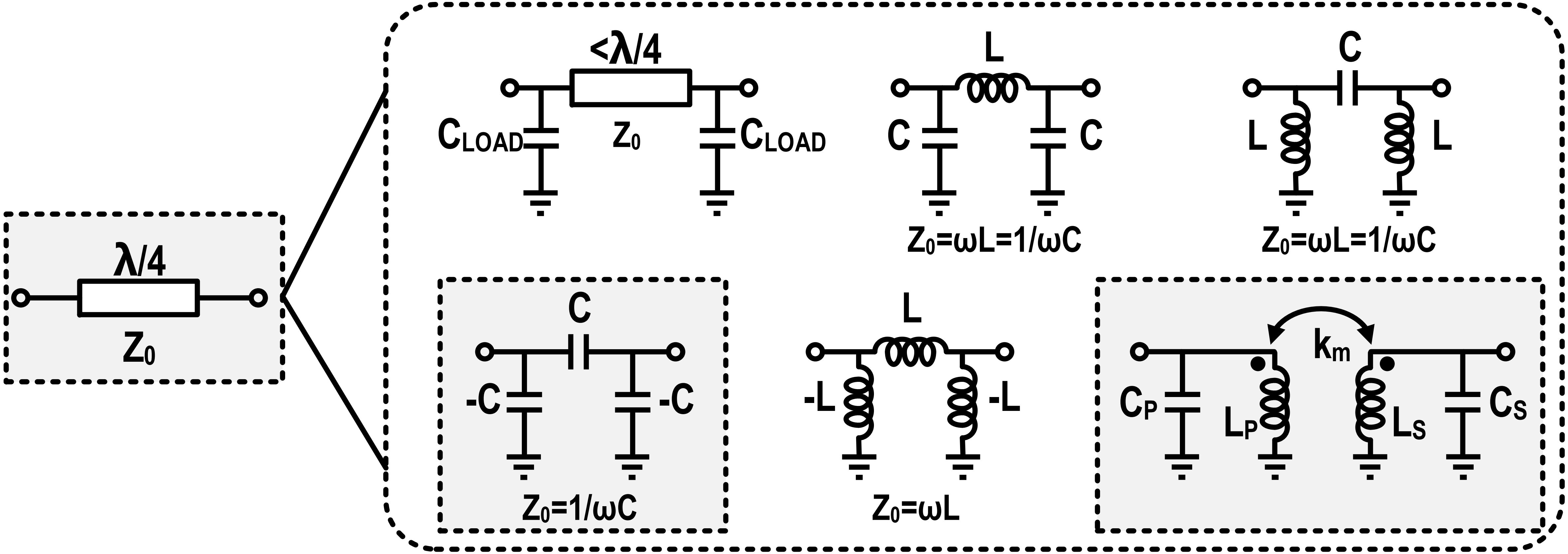






Power Combining Doherty PA Architecture

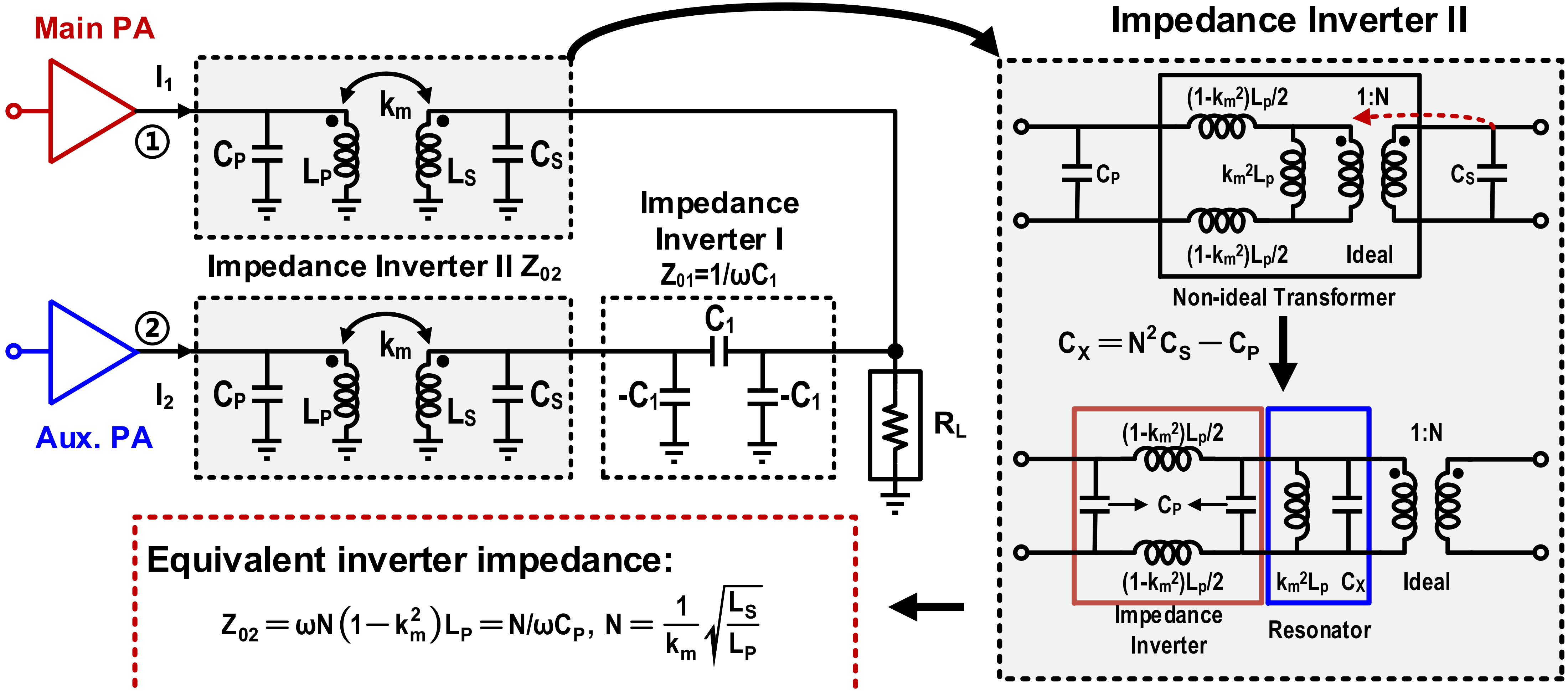
- **Compact impedance inverters**



[F. Wang et al., JSSC, 2021]

Power Combining Doherty PA Architecture

- **Broadband Doherty PA with compact inverters**

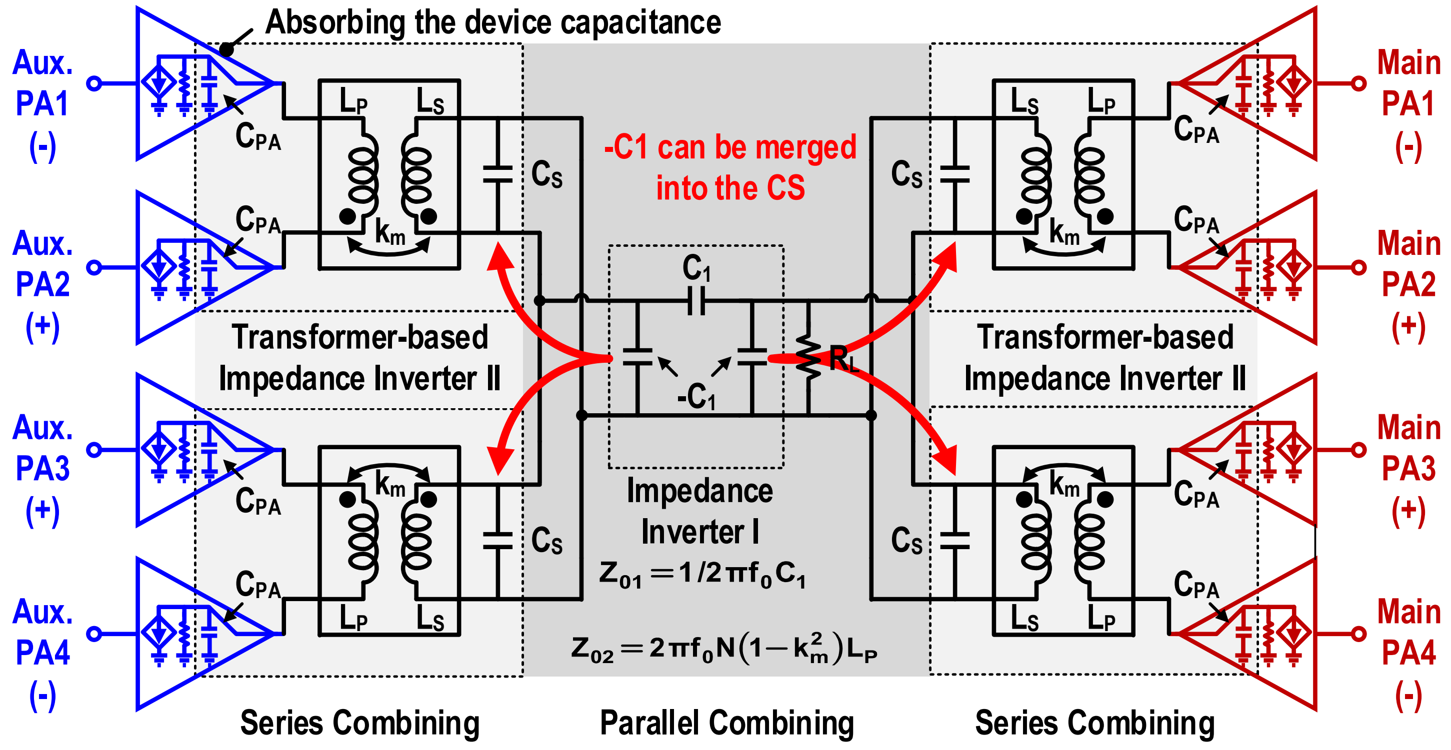


Equivalent inverter impedance:

$$Z_{02} = \omega N\left(1-k_m^2\right)L_P = N/\omega C_P,\ N = \frac{1}{k_m}\sqrt{\frac{L_S}{L_P}}$$

Power Combining Doherty PA Architecture

- **Power combining Doherty PA architecture**
  - ✓ Absorb the device capacitance C_{PA}
  - ✓ $-C_1$ can be absorbed into C_S

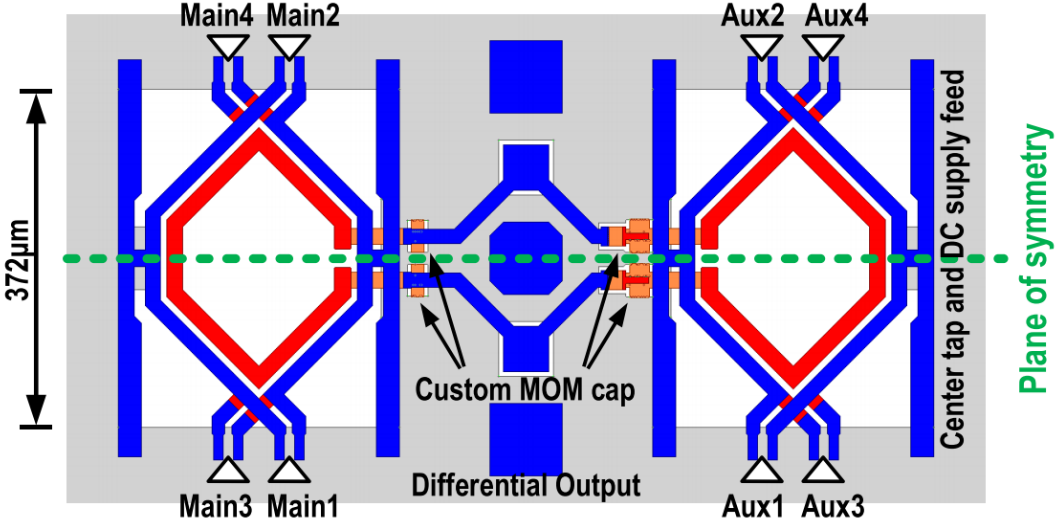


- Active load modulation
- Broadband
- Compact topology
- Hybrid power combining

How to realize? Use transformers and capacitors for sub-THz or THz?

Power Combining Doherty PA Architecture

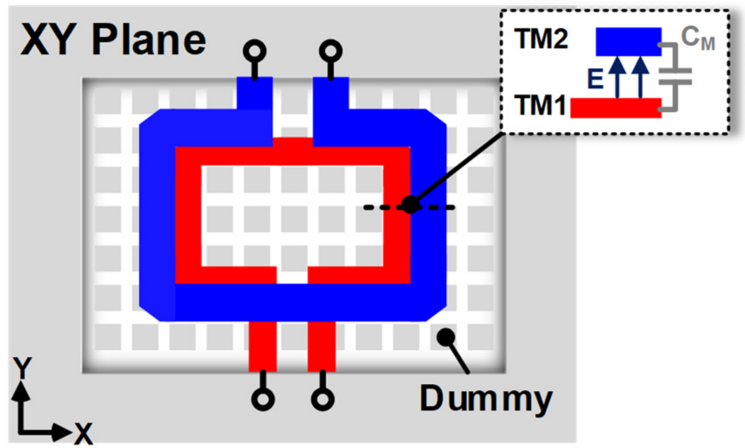
- **Conventional transformer-based implementation for mm-wave PA**



[F. Wang et al., JSSC, 2021]

- Differential output
  - X Lossy differential line
  - X Unfriendly for testing
- Many MOM capacitors
  - X Unfriendly for sub-THz EM simulation

Coupling Structure I



- Strong inter-winding capacitor C_M
- Undesired common-mode signals
- High Loss at high frequencies
- Filling dummy for DRC check

Outline

- Motivation
- Power Combining Doherty PA Architecture
- **Slotline-based Power Combiner**
- Circuit Implementation
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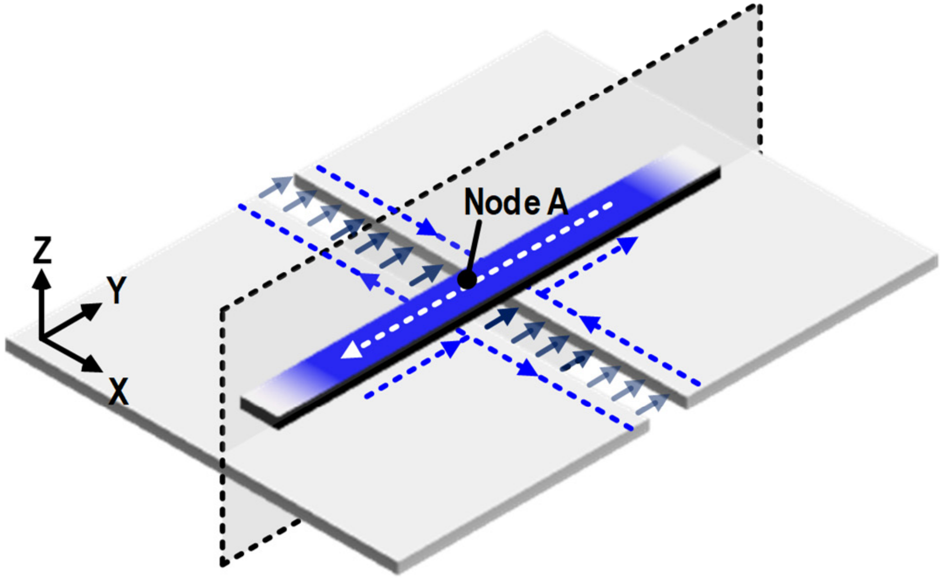
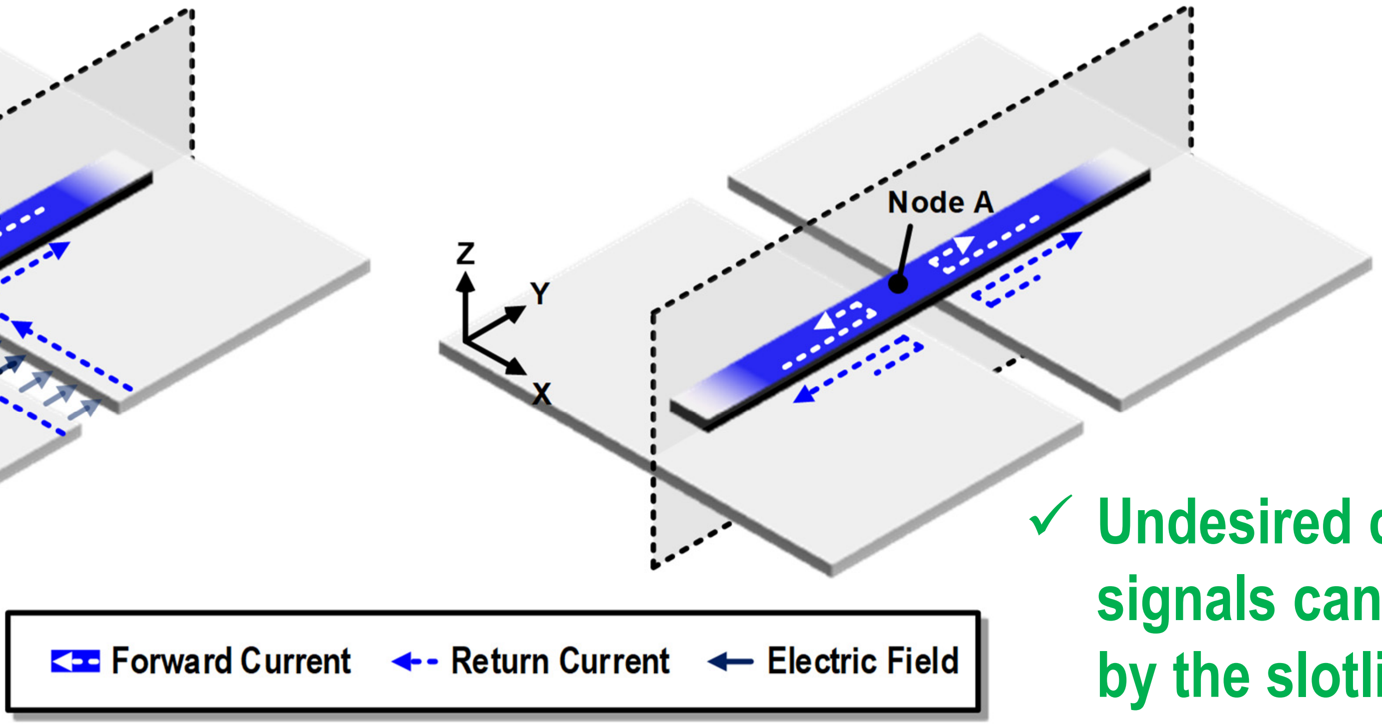
Slotline-based Power Combiner

- Microstrip-to-slotline transition structure

Odd-mode:
Transmission mode at the slotline is excited

Even-mode:
TM-mode wave at the slotline is suppressed

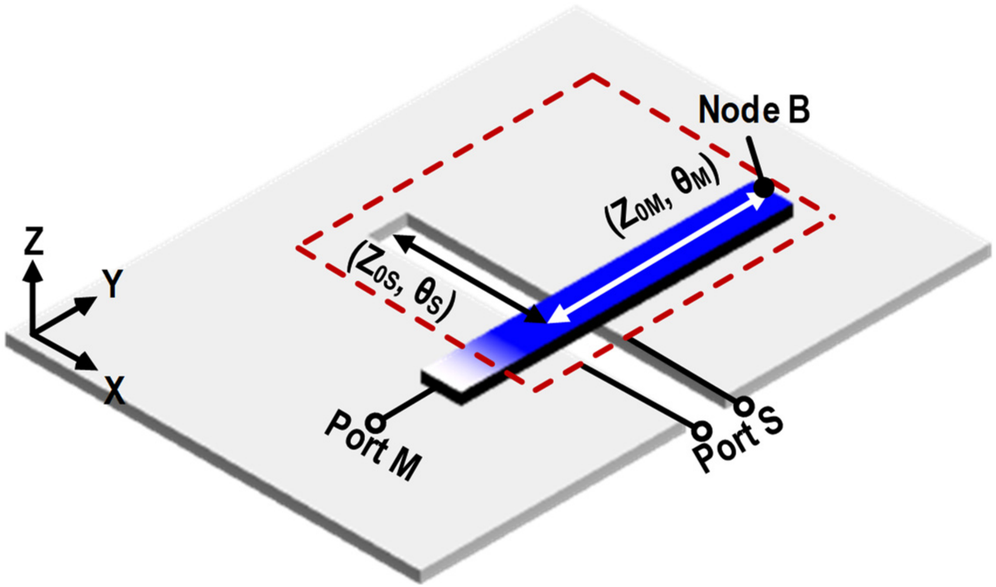


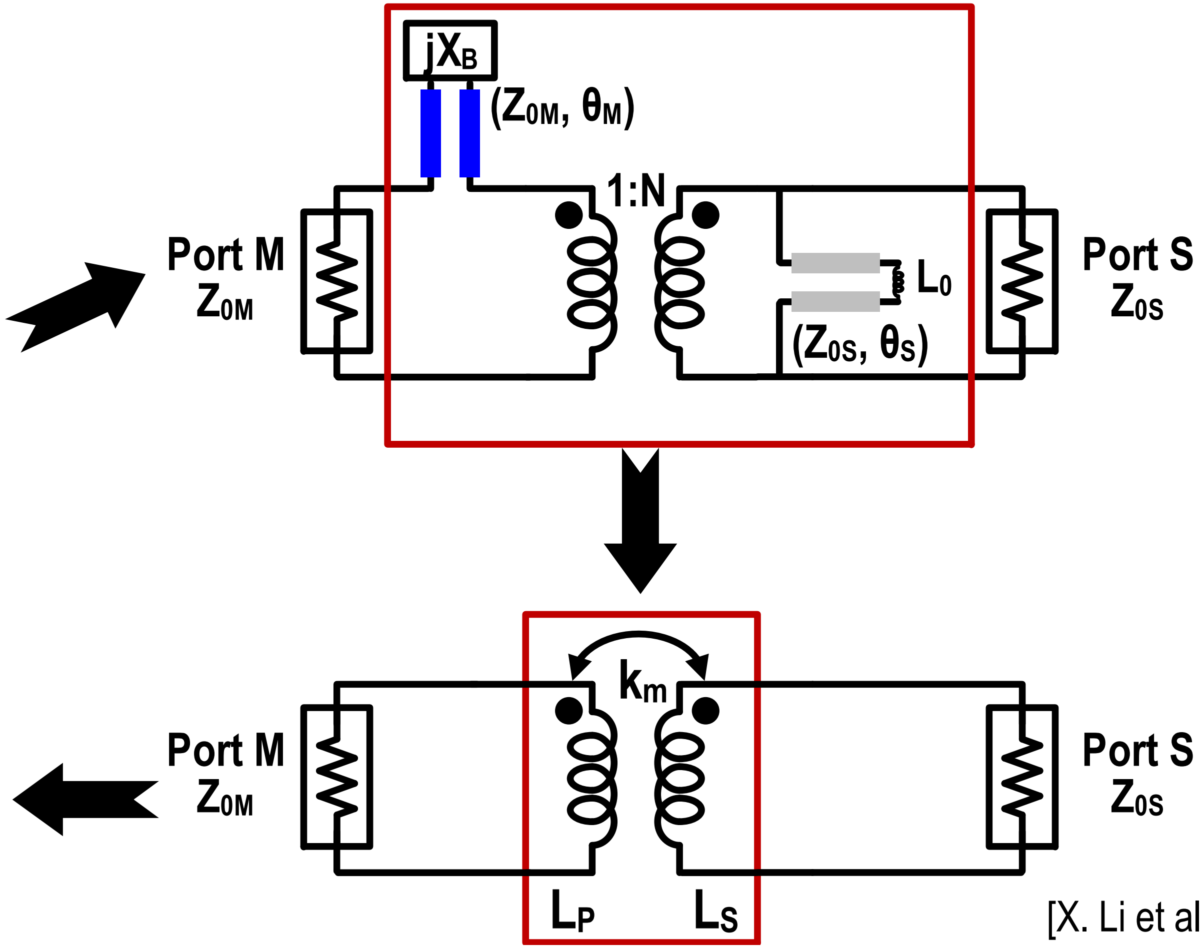


✓ Undesired common-mode signals can be suppressed by the slotline.

Slotline-based Power Combiner

- Microstrip-to-slotline transition structure





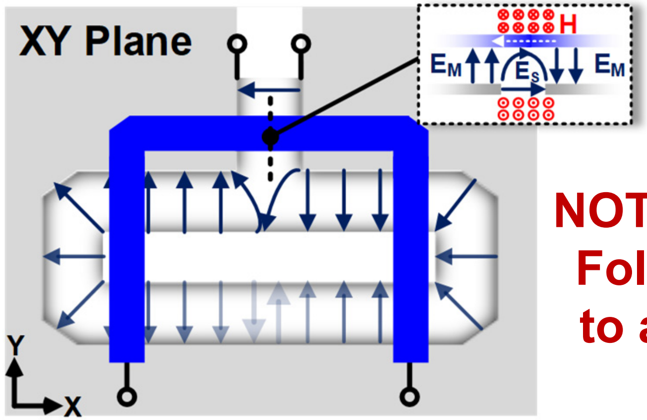
✓ Slotline-microstrip transition can realize a non-ideal transformer.

[X. Li et al., JSSC, 2021]

Slotline-based Power Combiner

- **Slotline-based power combiner implementation**

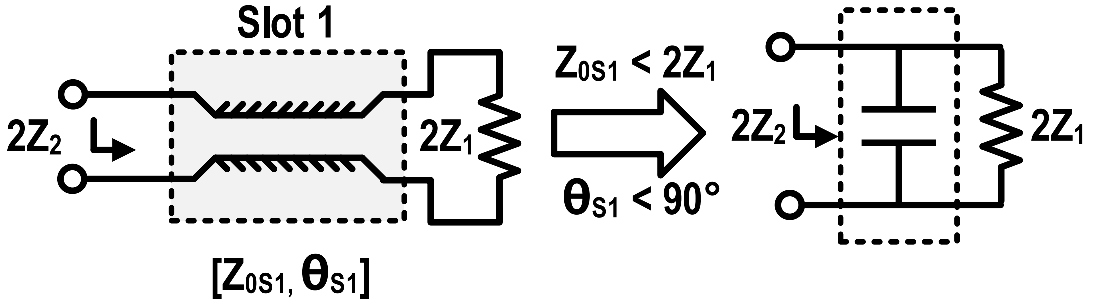
Proposed Coupling Structure II (GCPW-to-slotline transition-based)



NOTE !!
Folded slots used to avoid radiation

- Eliminated C_M due to orthogonal E_M and E_S
- Excellent common-mode suppression
- Lower Loss with solid stacked metals
- Easily pass the DRC check

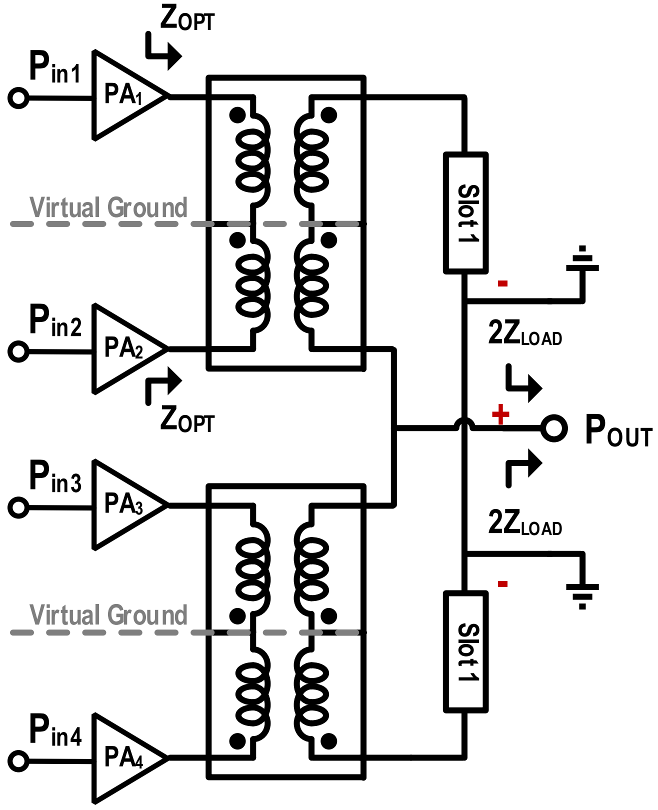
Capacitance implementation for C_S-$C_1/2$



- Use slotline
  - √ Friendly for EM simulation
  - √ Low loss for transmission mode
  - √ Easily achieve a single-end output with a slotline-to-GCPW transition

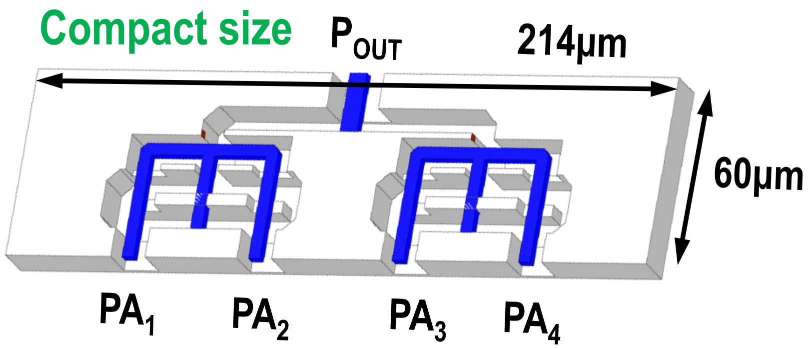
Slotline-based Power Combiner

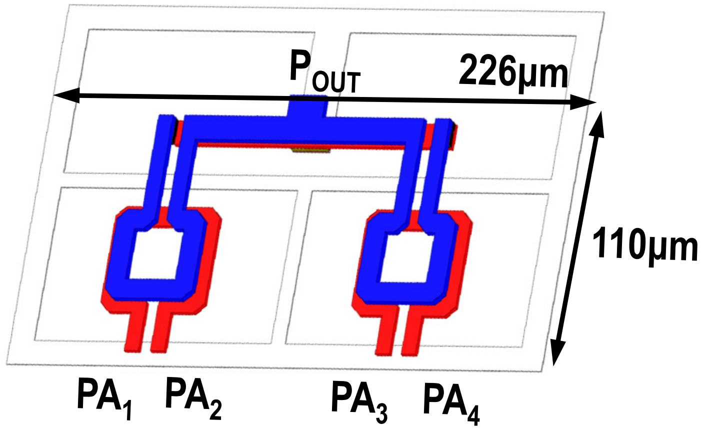
- **Slotline-based power combiner implementation**

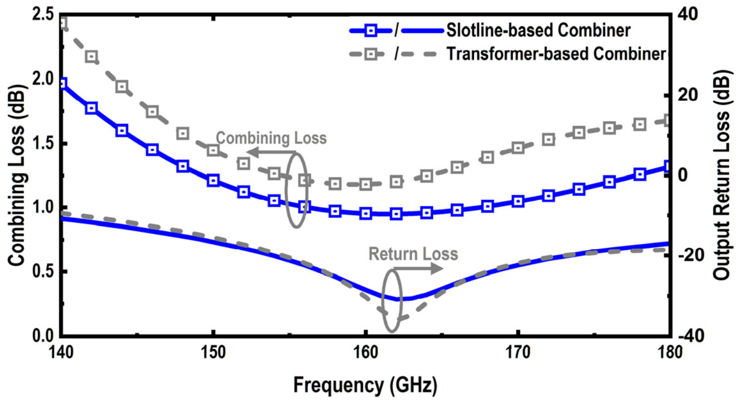


[X. Li et al., JSSC, 2021]

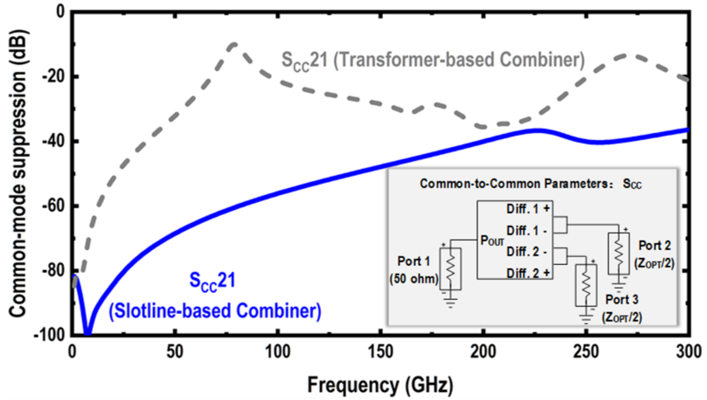
Slotline-based power combiner VS Transformer-based power combiner







Lower power loss

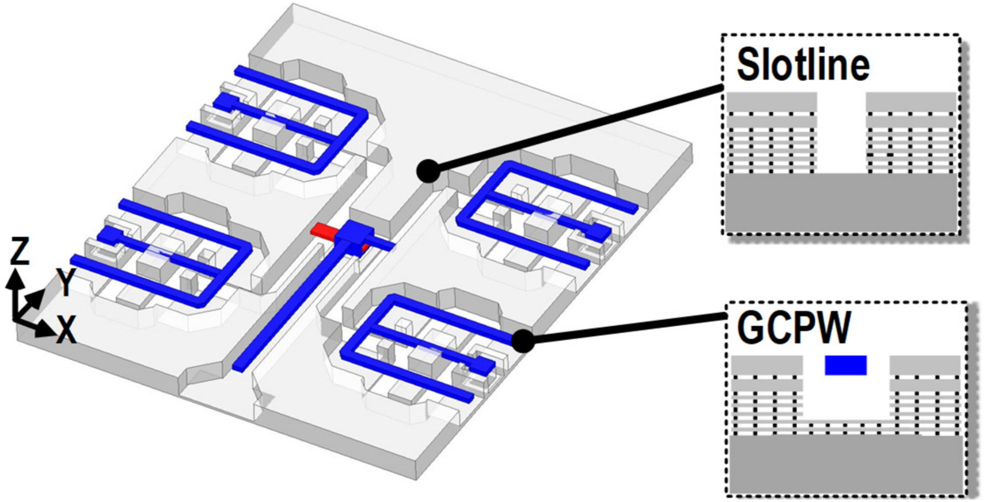


Higher common-mode suppression

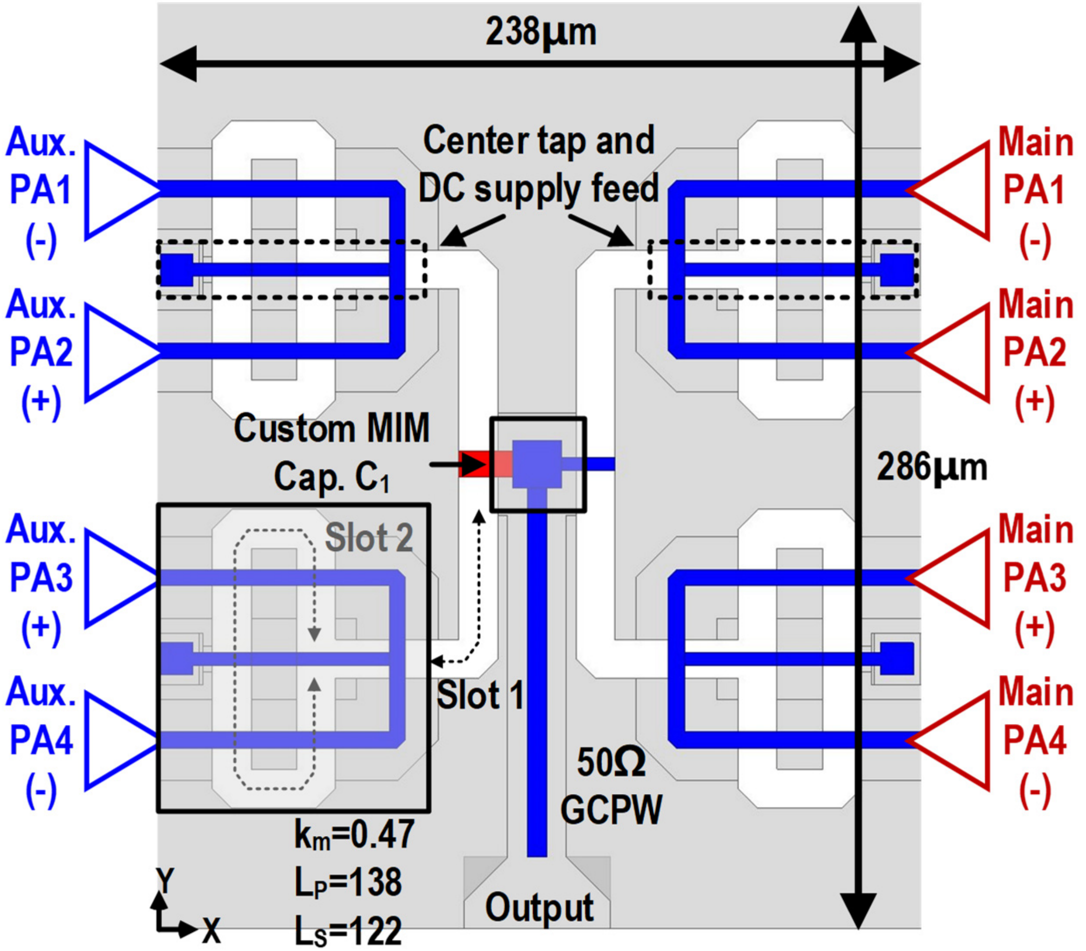
Slotline-based Power Combiner

- **Slotline-based Doherty power combiner**
  - ☺ 8-way hybrid (parallel-series) power combining
  - ☺ Less capacitor
  - ☺ Single-end output
  - ☺ Compact layout

3D EM Simulation Model

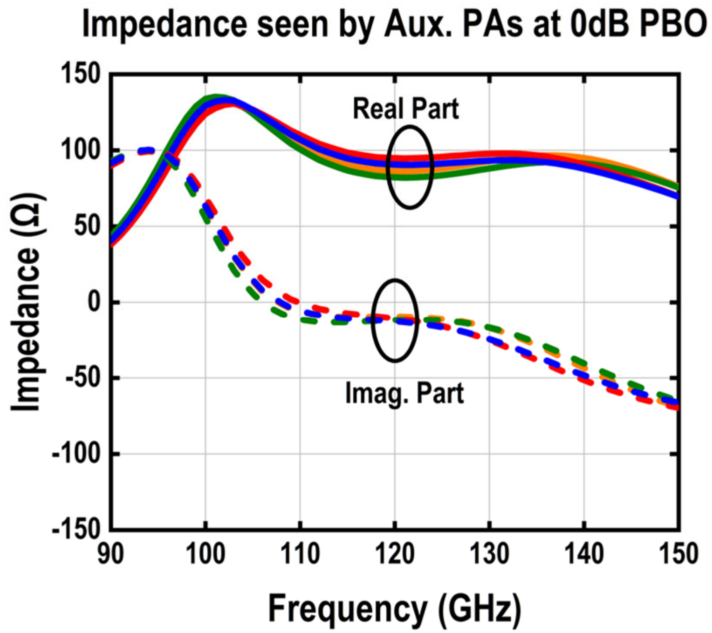


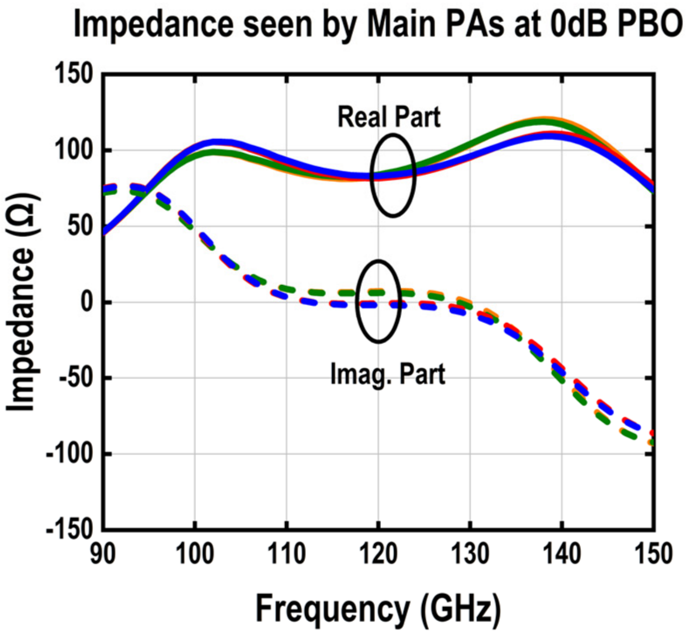
Top View of the Combiner

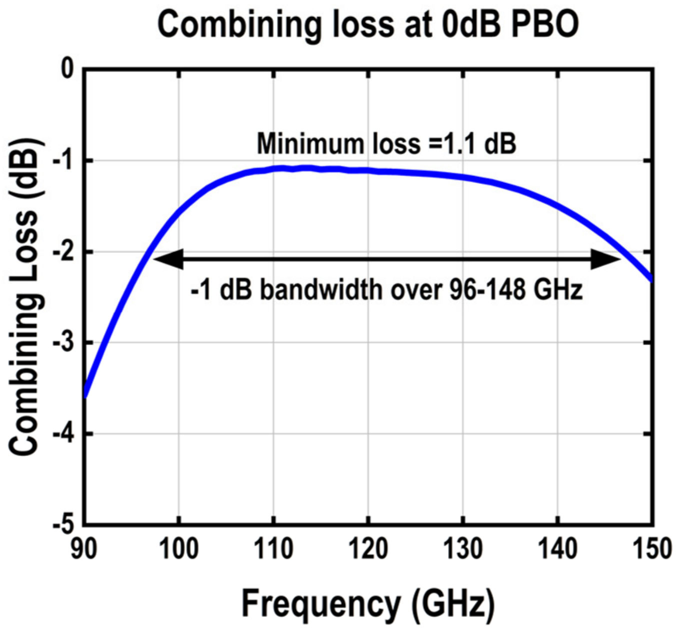


Slotline-based Power Combiner

- **Slotline-based Doherty power combiner**
  - Full EM simulations at 0dB power back-off





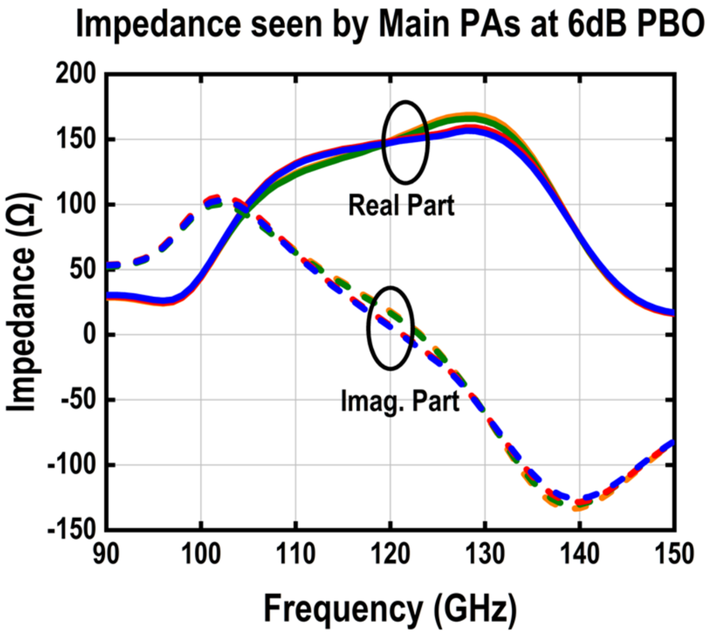


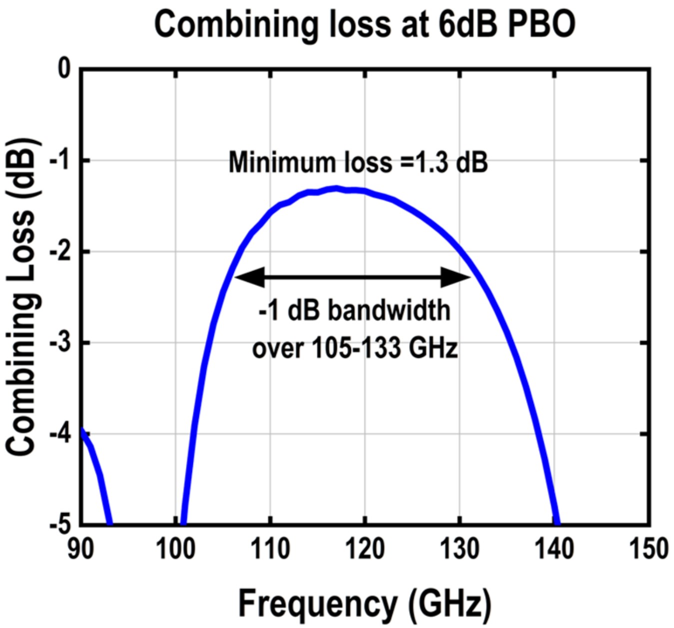
✓ Small port impedance difference

✓ Broadband and low-loss power combining

Slotline-based Power Combiner

- **Slotline-based Doherty power combiner**
  - Full EM simulations at 6dB power back-off





✓ Small port impedance difference

✓ Broadband and low-loss power combining

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- **Circuit Implementation**
- Measurements
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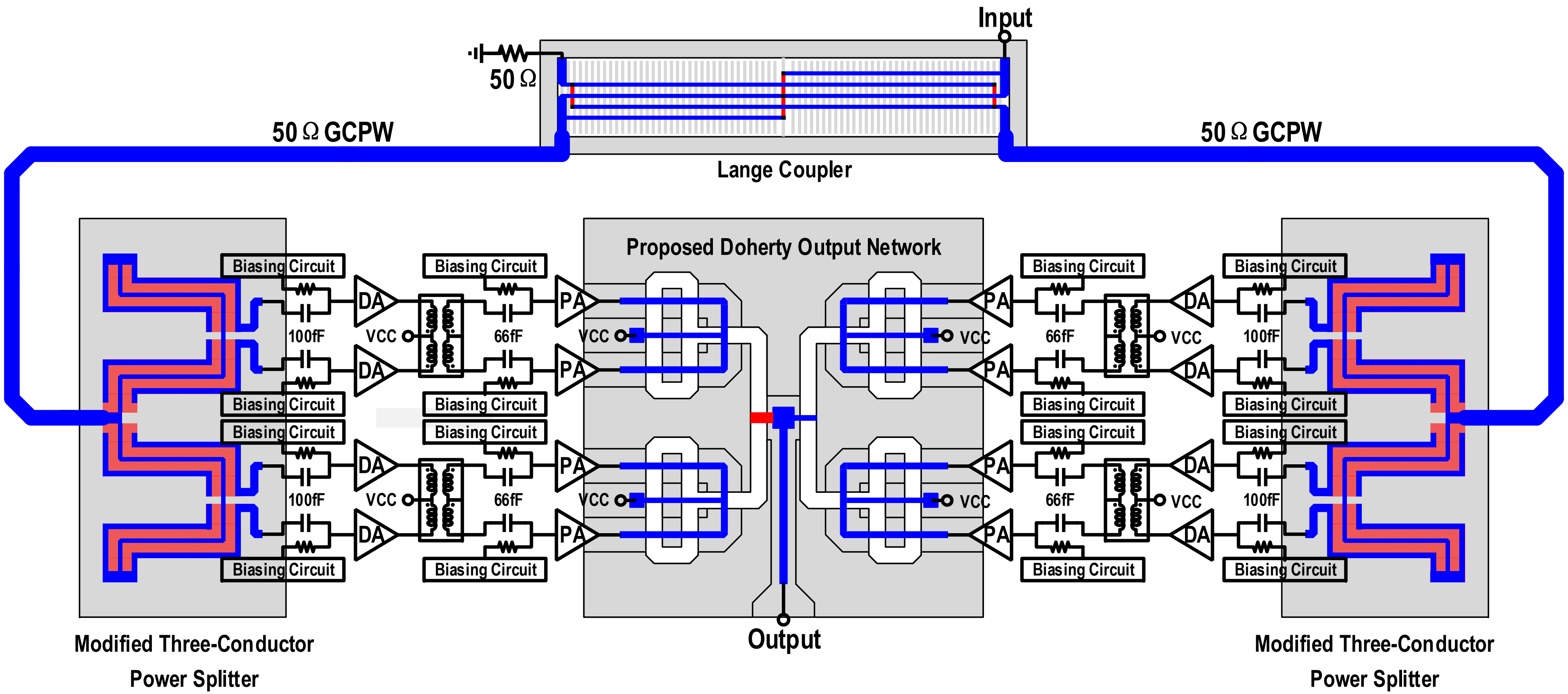
Circuit Implementation

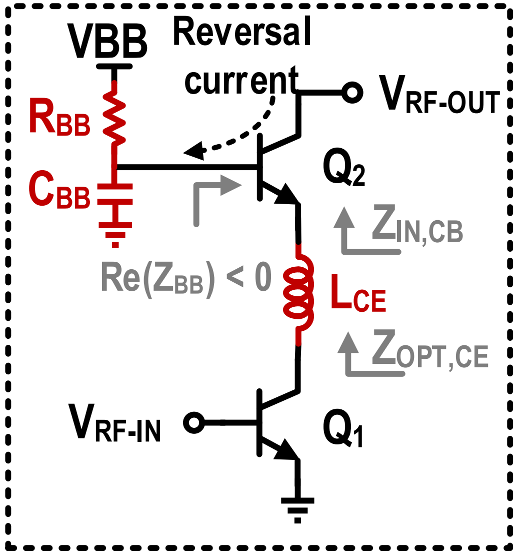
- **Top schematic**
  - ✓ 0.13μm SiGe BiCMOS: f_T/f_{max}=350/450GHz



Circuit Implementation

- **Top schematic**
  - ✓ Stacked DA/PA stages: VCC=4V
  - ✓ Linear-bias circuit

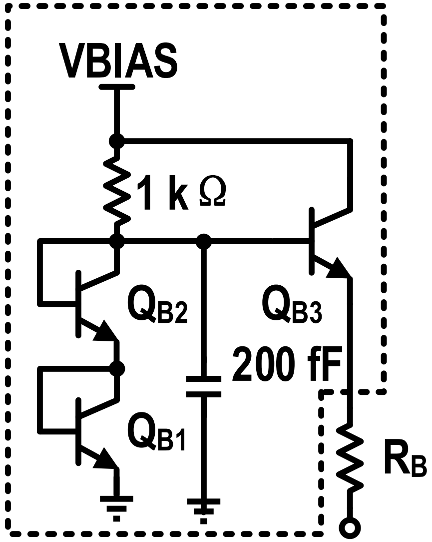
DA/PA Core



DA stage:
- Q_1/Q_2: 6x0.07x0.9 µm^2
- R_{BB}: 200 Ω
- C_{BB}: 200fF

PA stage:
- Q_1/Q_2: 10x0.07x0.9 µm^2
- R_{BB}: 200 Ω
- C_{BB}: 250fF

Biasing Circuit



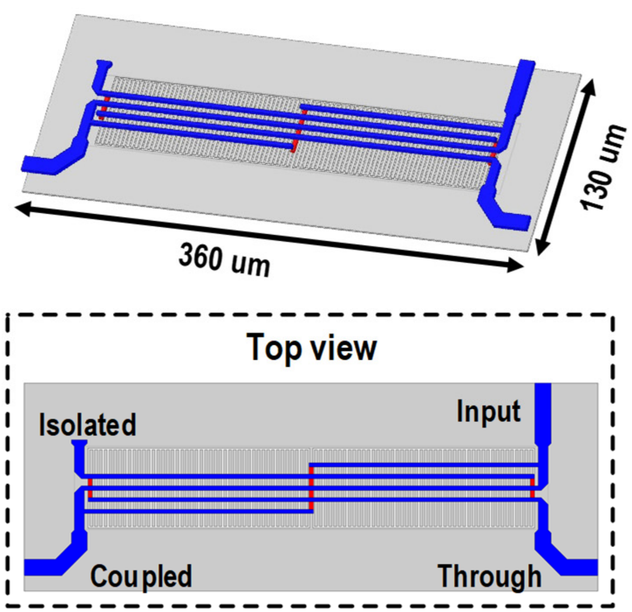
DA stage:
- Q_{B1}-Q_{B3}: 1x0.07x0.9 µm^2
- R_B: 100 Ω

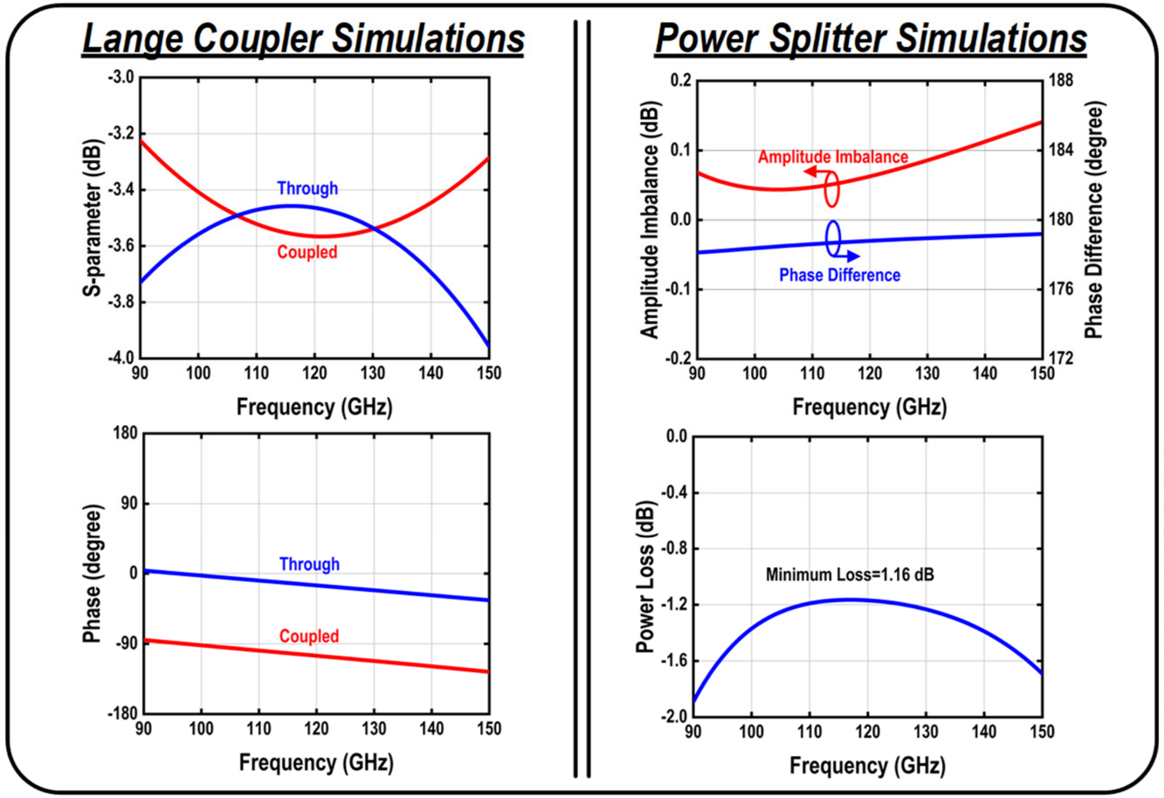
PA stage:
- Q_{B1}-Q_{B3}: 1x0.07x0.9 µm^2
- R_B: 300 Ω

Circuit Implementation

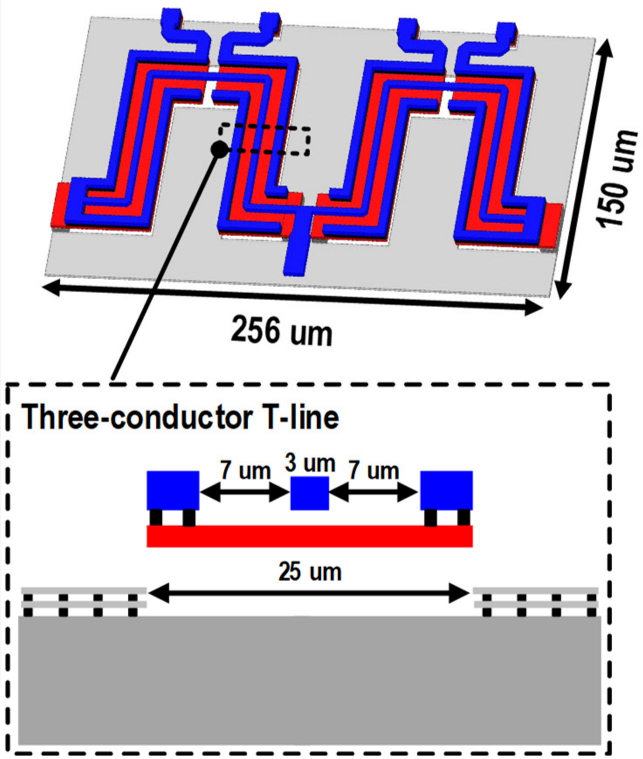
- **Top schematic**
  - ✓ Power splitting and phase shifting: Lange coupler+three-conductor-based balun.

Lange coupler



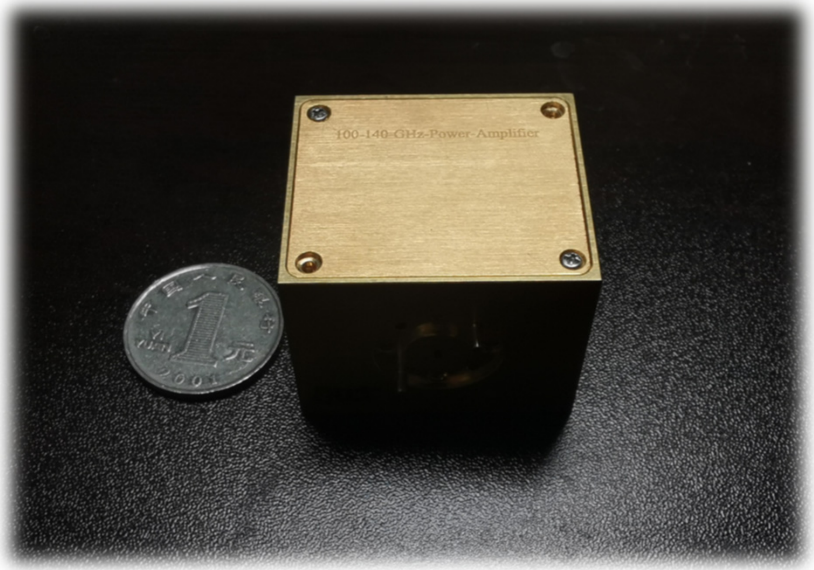


Three-conductor-based power splitter

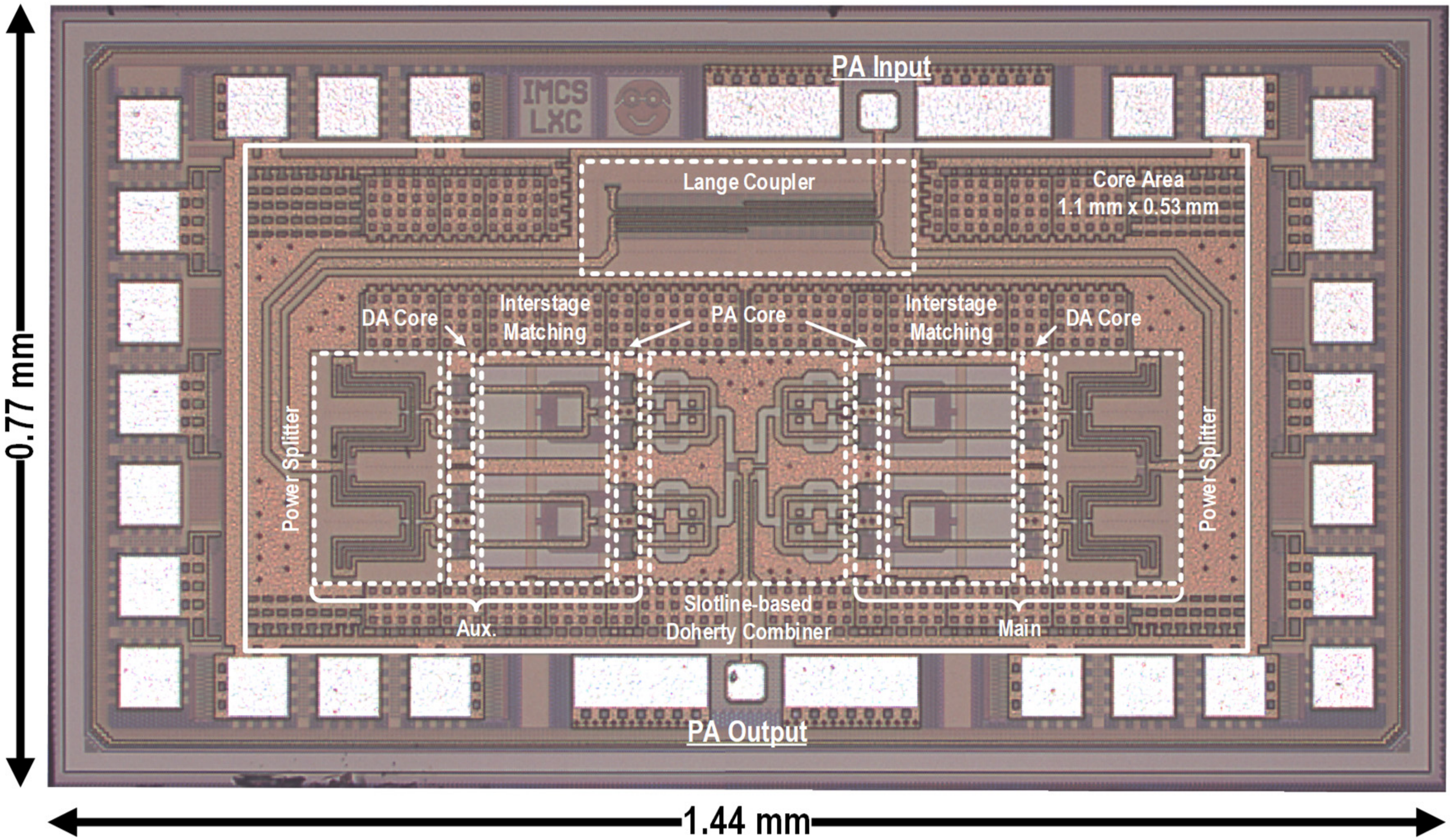


Circuit Implementation

- **Chip microphotograph and package module**
  - 1.11mm^2 total chip size
  - 0.58mm^2 core area



Package module



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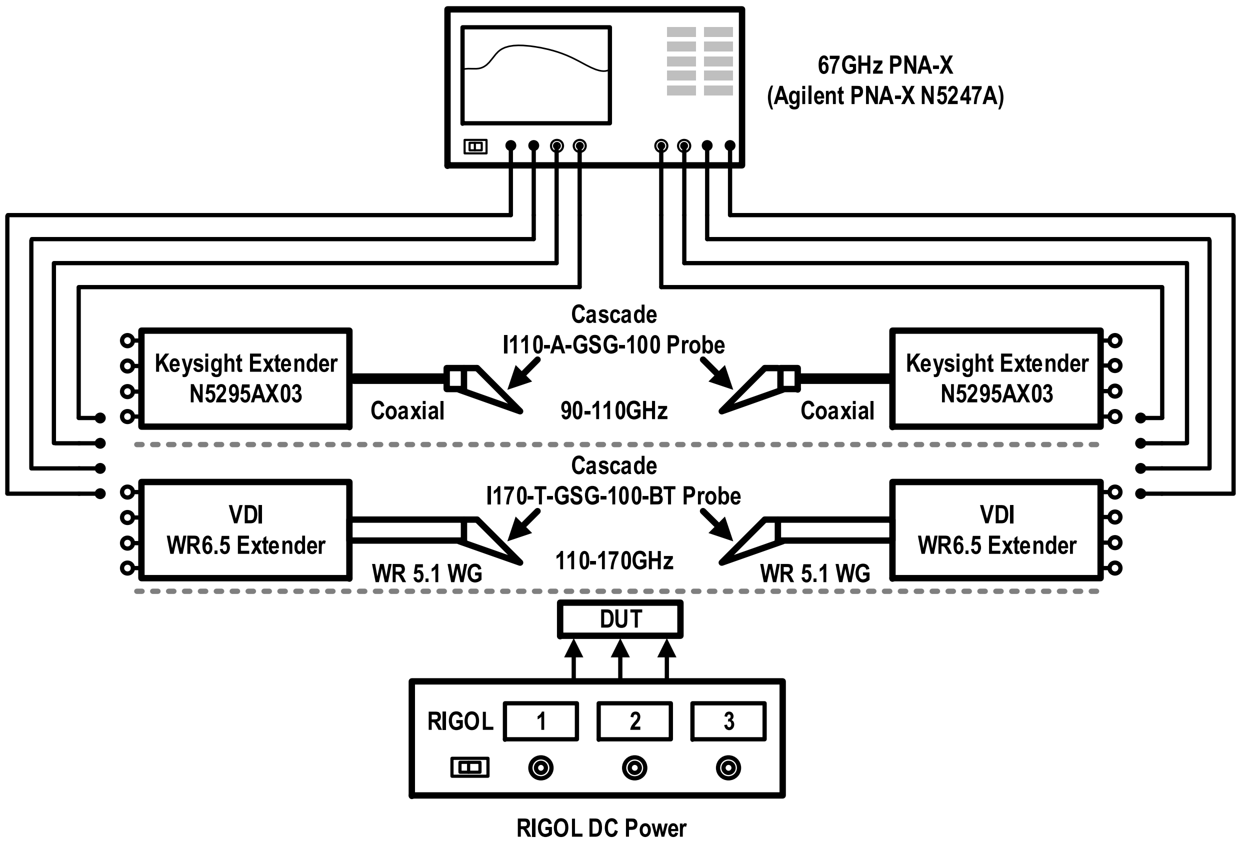
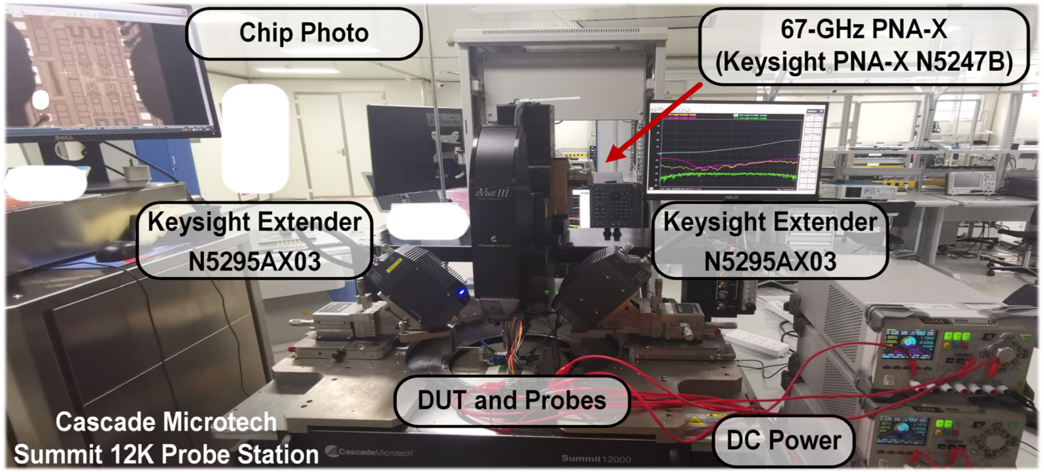
Measurements

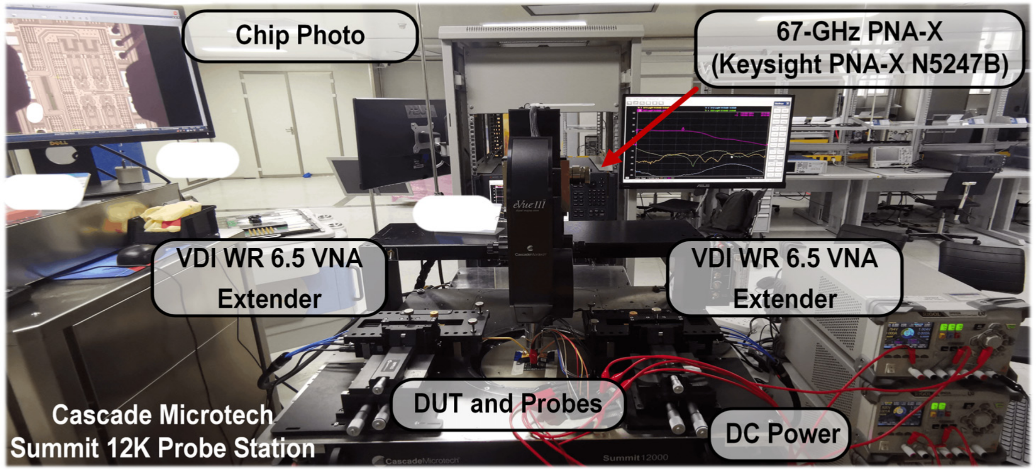
- **S-parameter measurement setup**



90-110GHz S-parameters

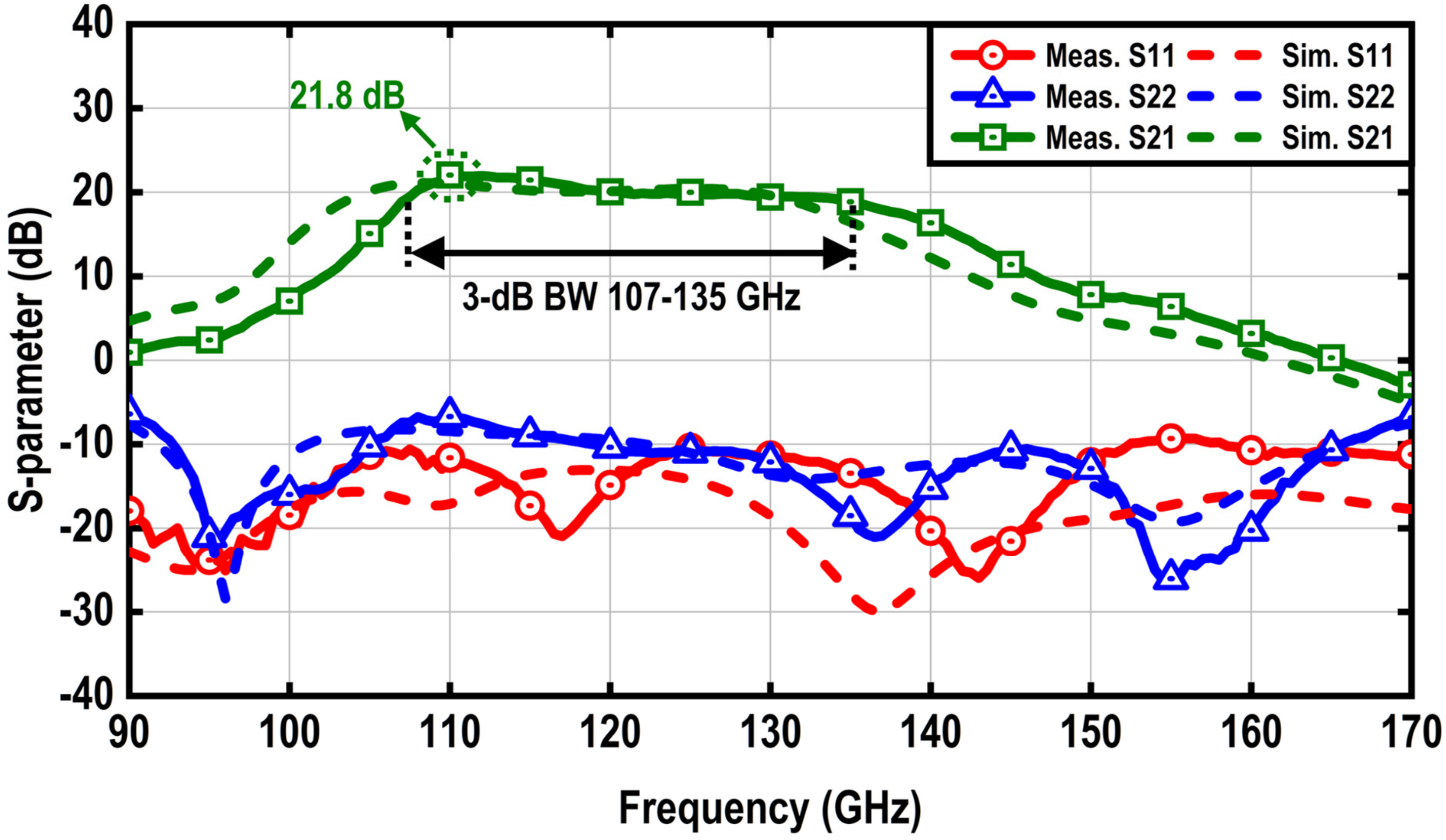


110-170GHz S-parameters



Measurements

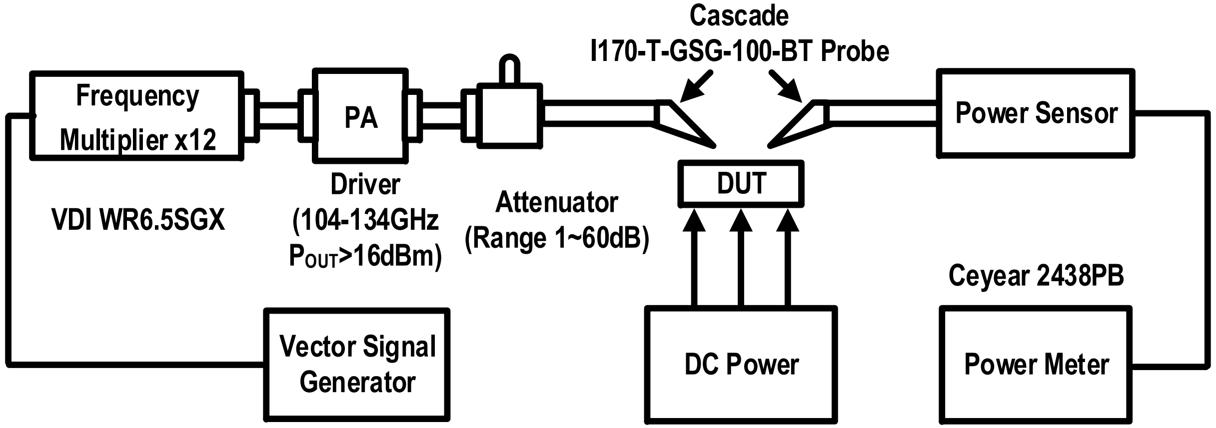
- **S-parameter measurement results**



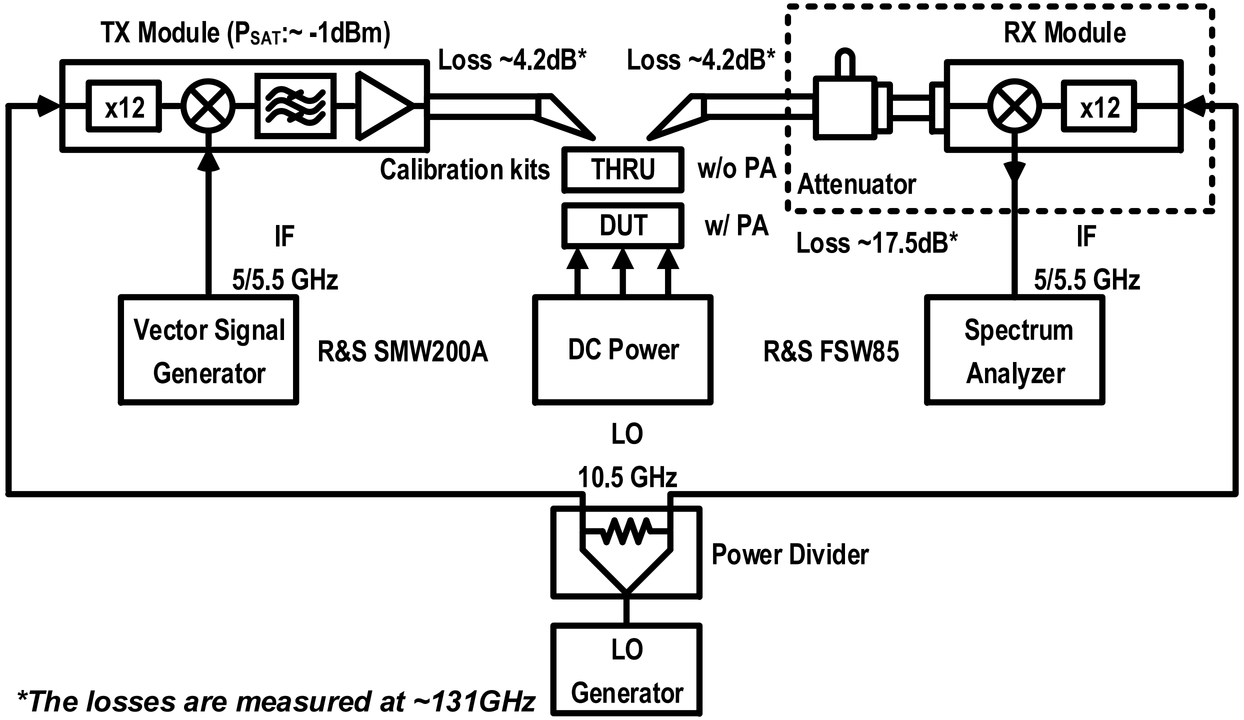
Measurements

- **Large-signal measurement setup**

Large-Signal CW Measurements



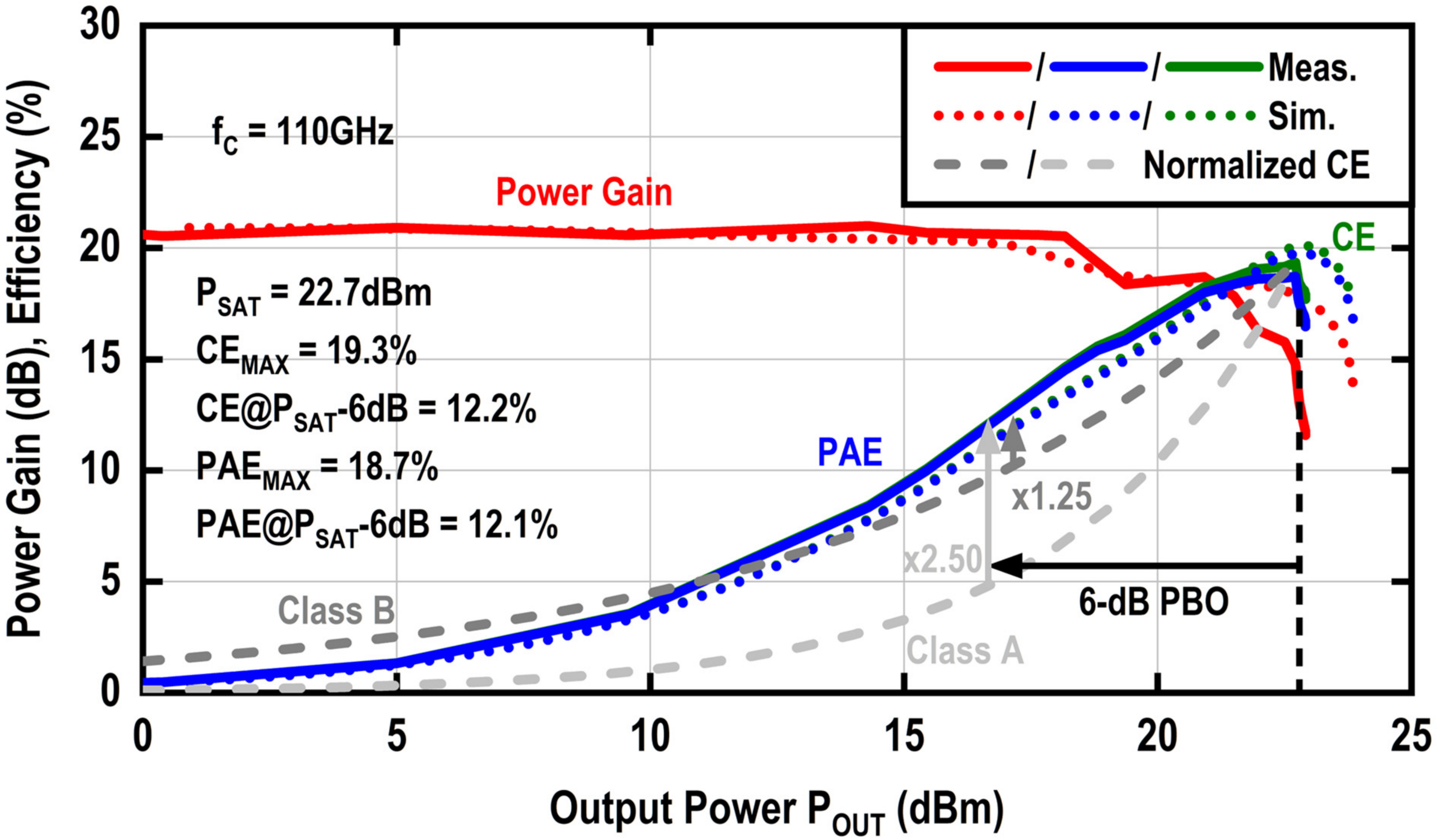
Large-Signal Modulation Measurements



**The losses are measured at ~131GHz*

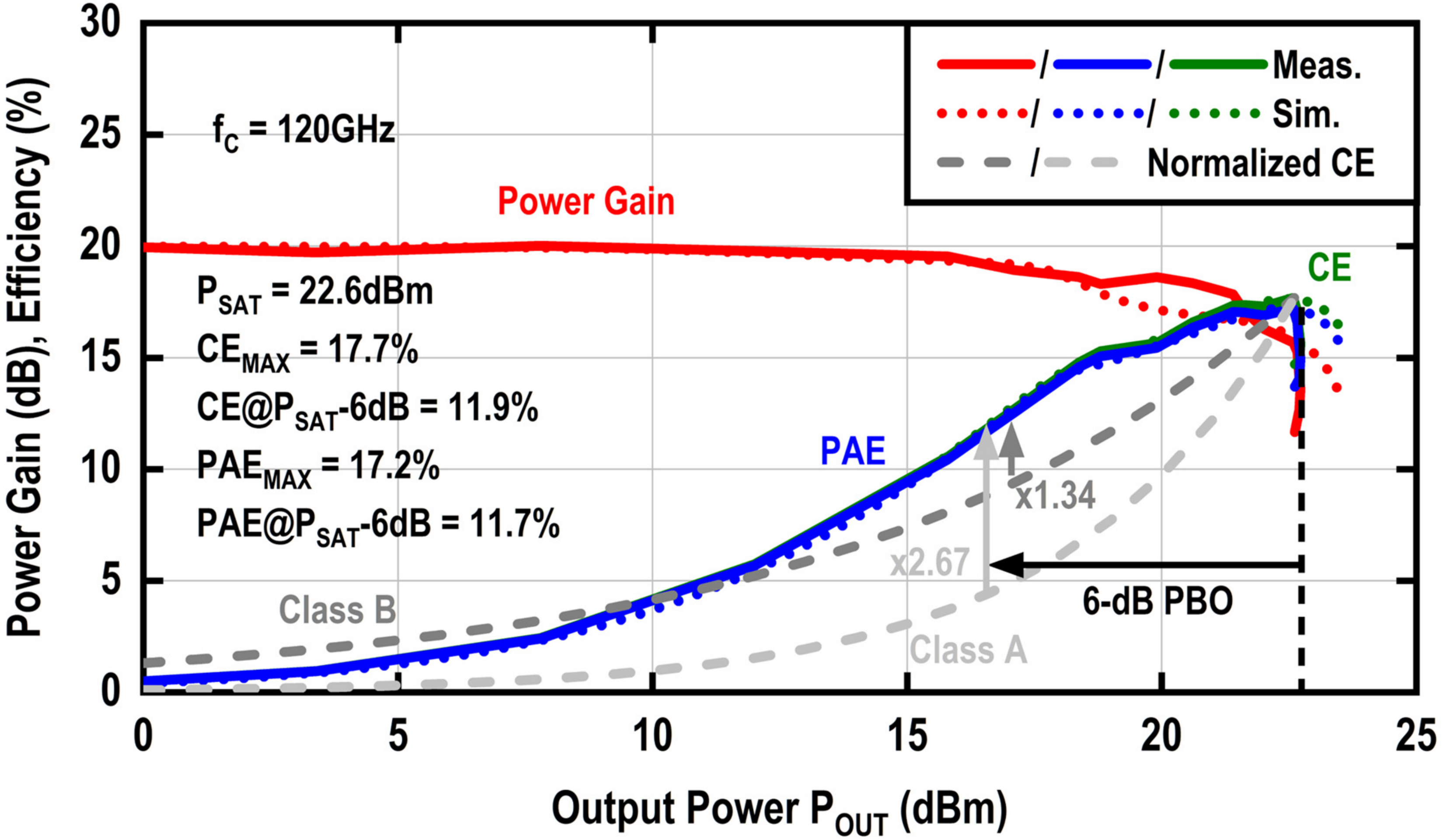
Measurements

- Large-signal continuous-wave measurement results at 110GHz



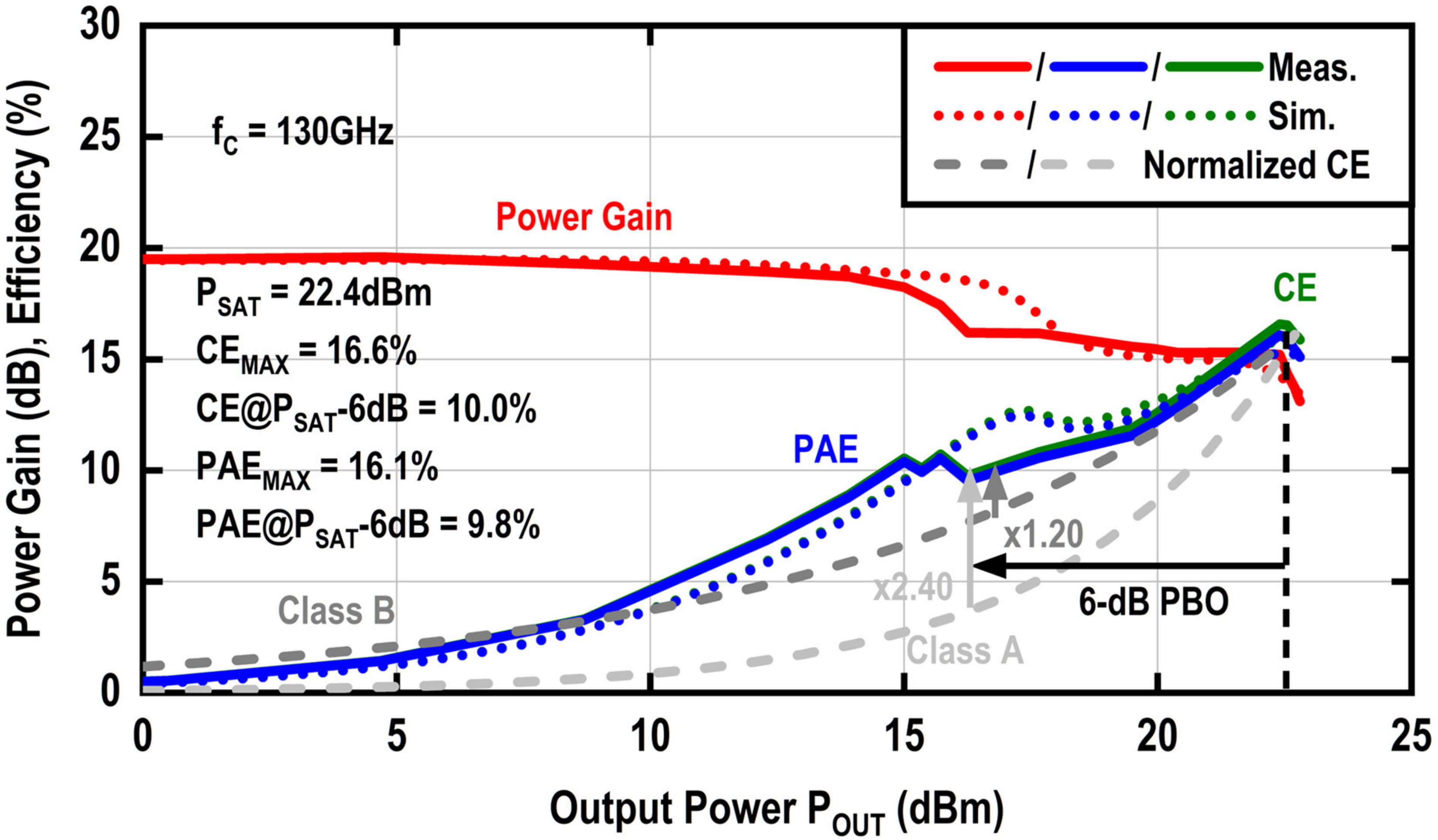
Measurements

- Large-signal continuous-wave measurement results at 120GHz



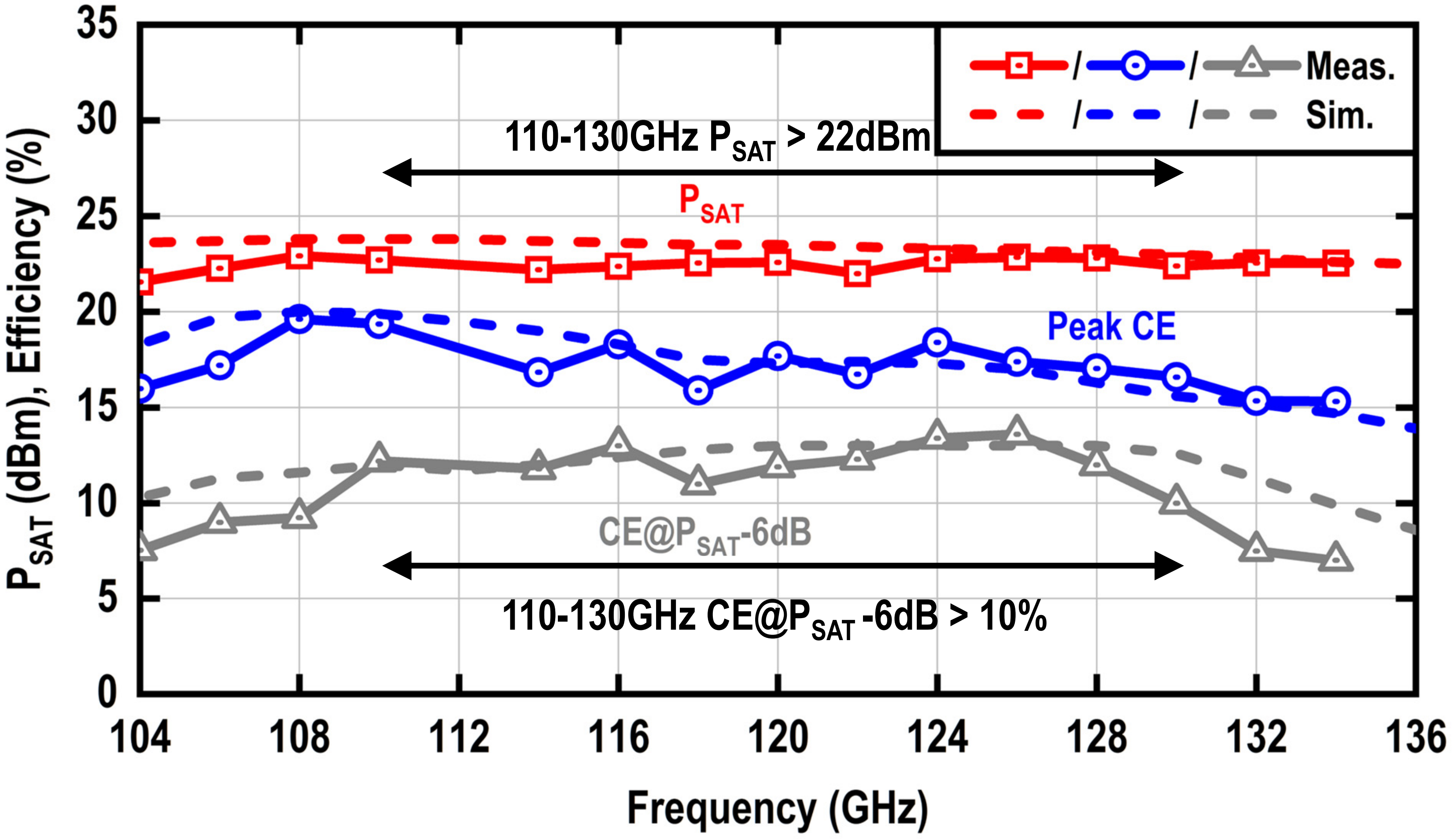
Measurements

- **Large-signal continuous-wave measurement results at 130GHz**



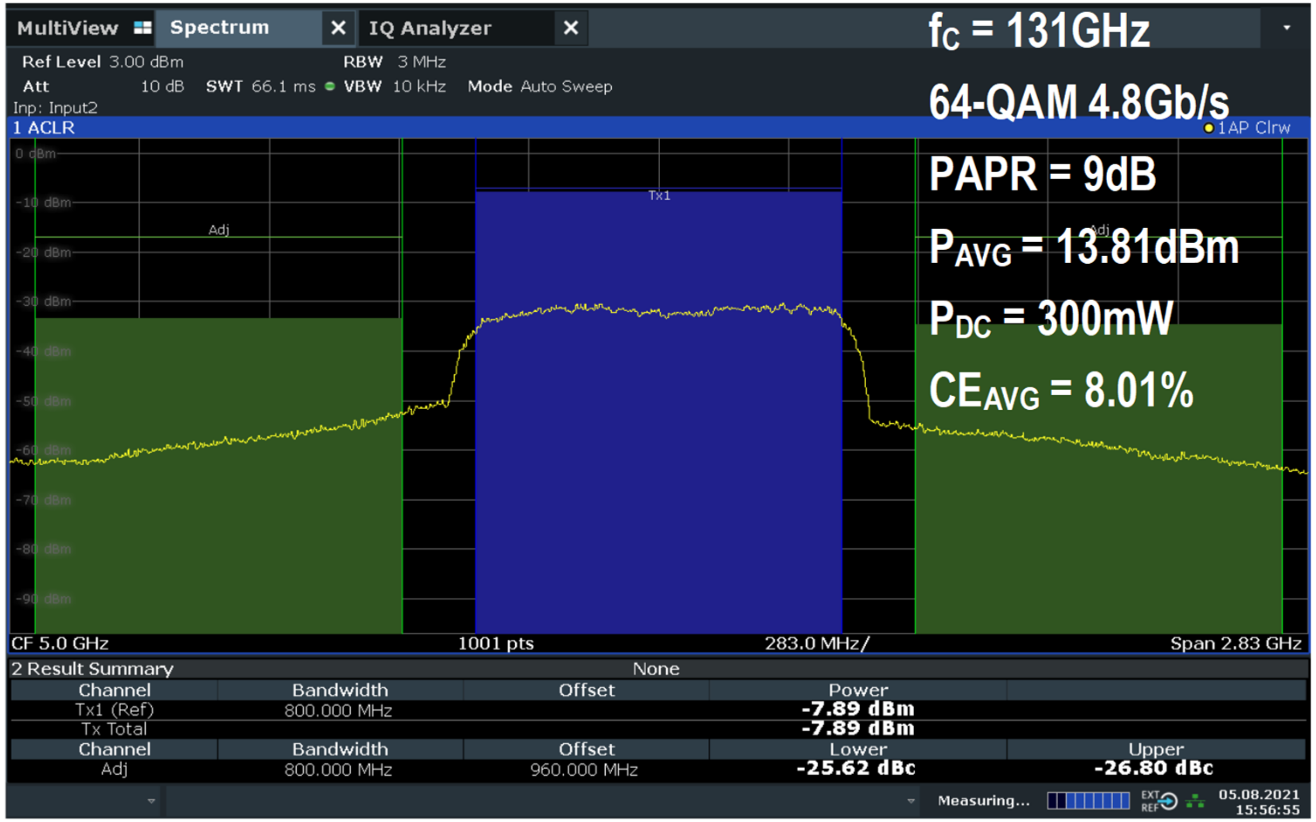
Measurements

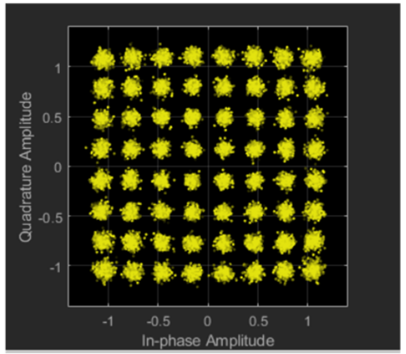
- Large-signal continuous-wave performance over frequency



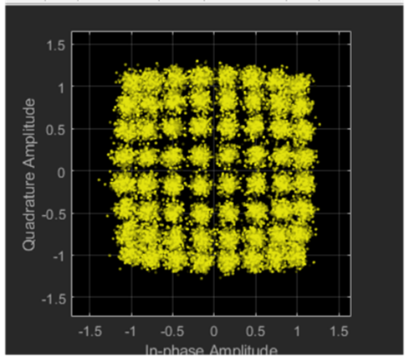
Measurements

- **Large-signal modulation measurement results**
  - ✓ 4.8Gb/s single-carrier 64-QAM signal with a 9dB PAPR





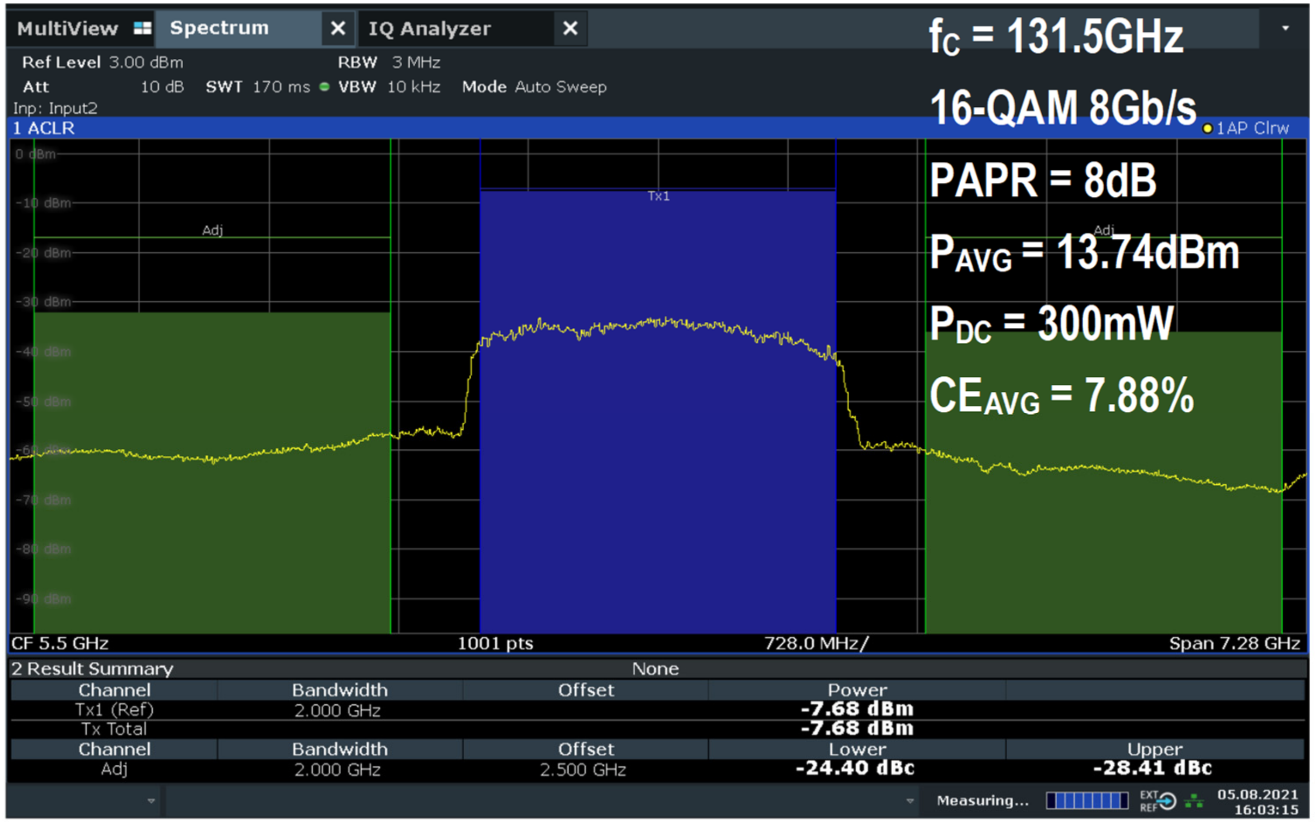
w/o PA EVM = 6.2%

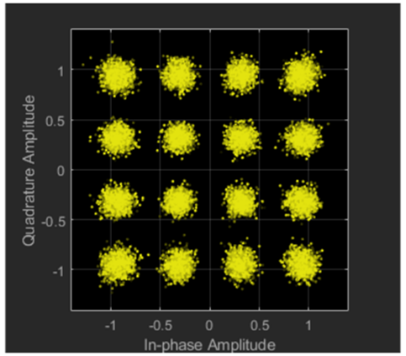


w/ PA EVM = 10.9%

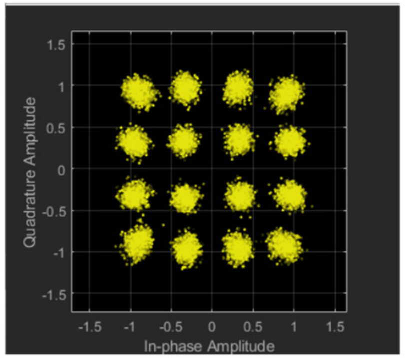
Measurements

- **Large-signal modulation measurement results**
  - ✓ 8Gb/s single-carrier 16-QAM signal with a 8dB PAPR





w/o PA EVM = 10.7%

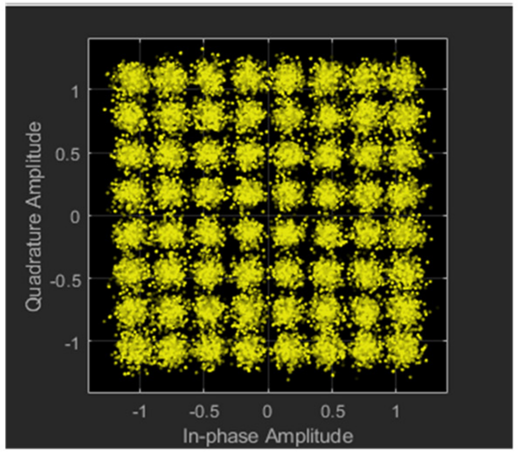


w/ PA EVM = 11.6%

Measurements

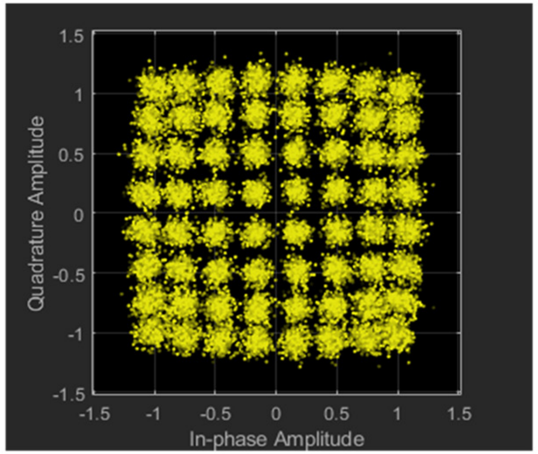
- **Large-signal modulation measurement results**

<u>f_C=131.5GHz 64-QAM 1.6GSym/s (9.6Gb/s) PAPR=9dB</u>



w/o PA

EVM = 9.9%*

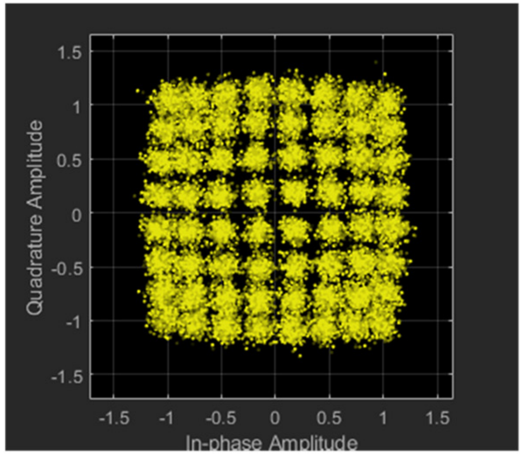


w/ PA

P_{AVG} = 12.65dBm

CE_{AVG} = 6.39%

EVM = 10.5%



w/ PA

P_{AVG} = 13.88dBm

CE_{AVG} = 8.14%

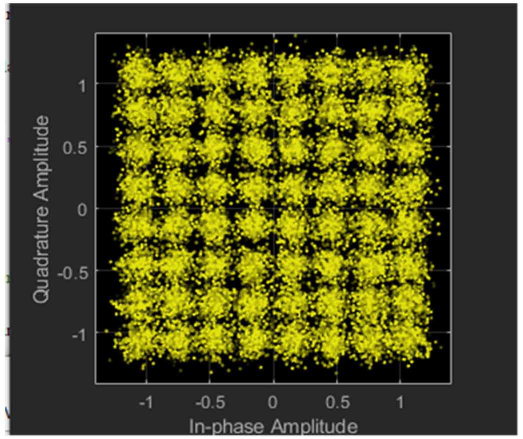
EVM = 12.4%

*The EVM performance of high-order and wideband modulated signals is limited by the Tx module.

Measurements

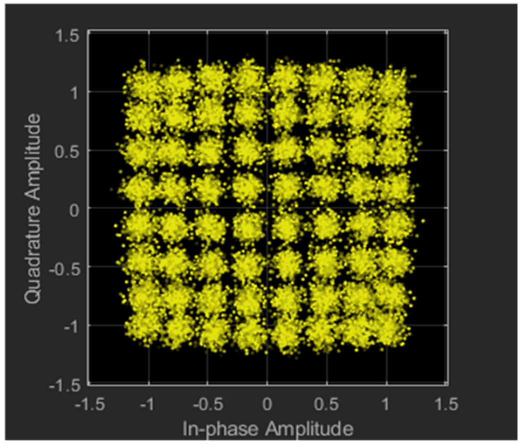
- **Large-signal modulation measurement results**

f_C=131.5GHz 64-QAM 2GSym/s (12Gb/s) PAPR=9dB



w/o PA

EVM = 11.0%*

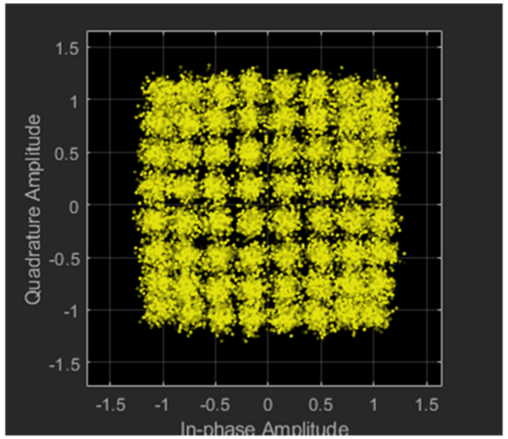


w/ PA

P_{AVG} = 12.49dBm

CE_{AVG} = 6.16%

EVM = 11.1%



w/ PA

P_{AVG} = 13.76dBm

CE_{AVG} = 7.92%

EVM = 11.9%

*The EVM performance of high-order and wideband modulated signals is limited by the Tx module.

Outline

- Motivation
- Power Combining Doherty PA Architecture
- Slotline-based Power Combiner
- Circuit Implementation
- Measurements
- **Conclusion**

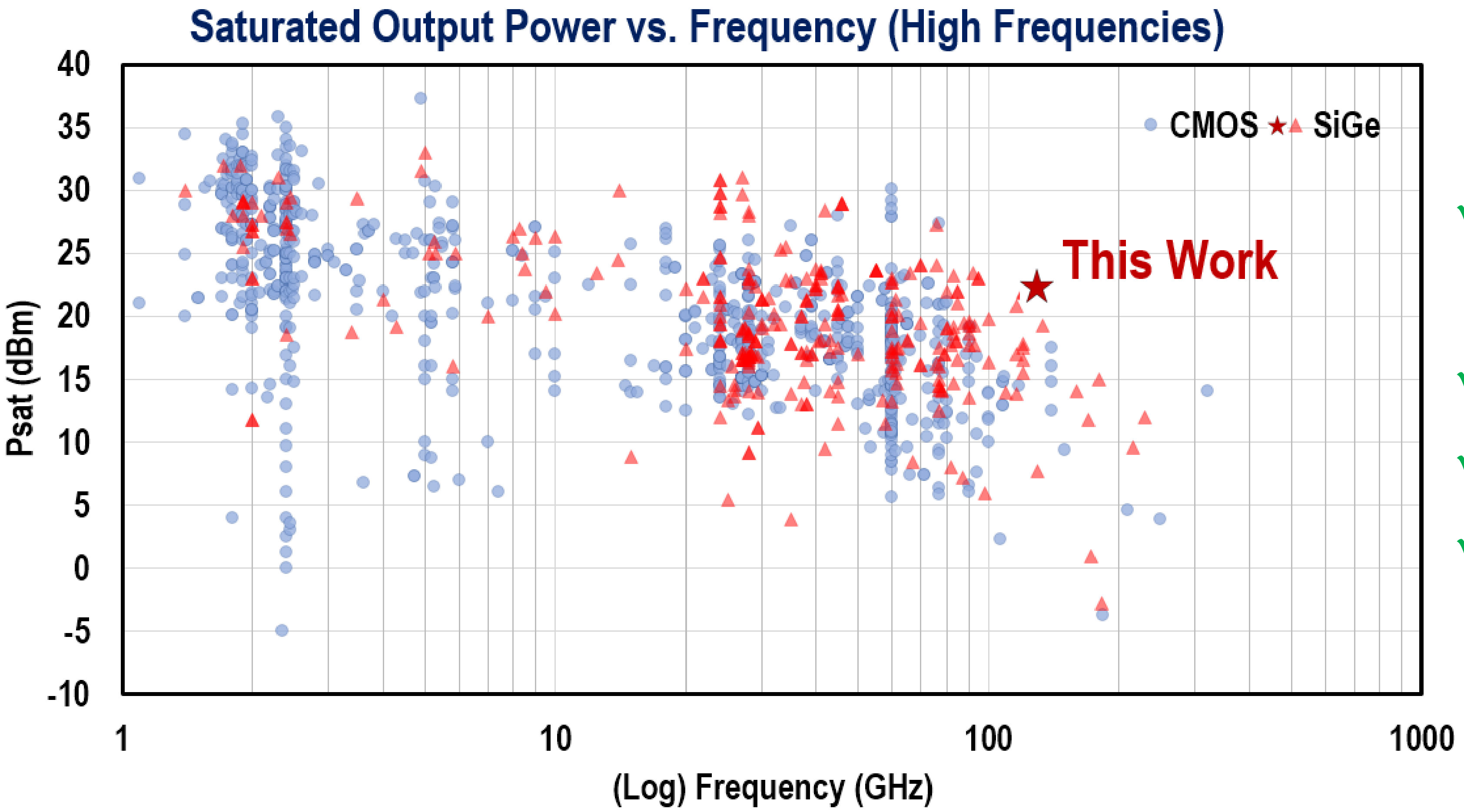
Conclusion

- **Comparison with the state-of-art D-band PAs**

Reference	This Work			Philippe ISSCC'20	Li RFIC'21	Petricli MWCL'21		Rao MWCL'21	Li JSSC'21
Technology	130nm SiGe			16nm FinFET	45nm CMOS SOI	55nm SiGe		90nm SiGe	130nm SiGe
Architecture	8-way Slotline-based Comb. Doherty			4-way TF-based Comb.	8-way TL-based Comb.	Common-base		4-way Wilkioson Comb.	4-way Slotline-based Comb.
Gain (dB)	21.8			25.6	24	24	22.4	18.2	30.7
BW_{-3dB} (GHz)	28 (107 to 135)			22	21 (130 to 151)	34 (125 to 159)	25 (125 to 150)	35 (110 to 145)	40 (142 to 182)
Freq. (GHz)	110	120	130	135	140	135	135	130	161
P_{SAT} (dBm)	22.7	22.6	22.4	15	17.5	17.6	19.3	21.9	18.1
PAE_{MAX} (%)	18.7	17.2	16.1	12.8	13.4	17.5	13	12.5	12.4
PAE at 6-dB PBO (%)	12.1	11.7	9.8	<5*	<5*	8.5	6.7	<5*	<5*
Area (mm^2)	1.11 (0.58**)			0.041**	0.43**	0.18**	0.26**	1.71	0.42

Conclusion

- **Output power comparison with the state-of-art silicon-based PAs**



[H. Wang et al., Power Amplifiers Performance Survey 2000-Present]

- ✓ Silicon-based Doherty PA above 100GHz
- ✓ 22.7dBm P_{SAT}
- ✓ 18.7% Peak PAE
- ✓ 12.1% PBO PAE

Conclusion

- **Comparison with prior mm-wave Doherty PAs and D-band Txs**

Reference	This Work		Wang JSSC'21	Liu IMS'21	Kaymaksut T-MTT'15	Hamani SSCL'20	
Technology	130nm SiGe		130nm SiGe	130 nm SiGe	40 nm CMOS	45 nm CMOS SOI	
Architecture	8-way Slotline-based Comb. Doherty		Multi-Primary DAT-based Doherty	Quadrature-Hybrid Doherty	8-way TF-based Comb. Doherty	Tx Front-End (IF AMP+LO+Mixer+PA)	
Modulation Scheme	64-QAM	16-QAM	64-QAM	64-QAM	64-QAM	16-QAM 8 Channels	64-QAM 8 Channels
Freq. (GHz)	131	131.5	28	54	72	CH5: 150.7	CH5: 150.7
Data Rate (Gb/s)	4.8	8	1.2	6	0.6	7.04	10.56
PAPR (dB)	9	8	6.5	7.35	N.A.	N.A.	N.A.
P_{AVG} (dBm)	13.8	13.7	20.9	14.6	15.9	0.1	0.1
PAE_{AVG} (%)	8 (CE) 7.9 (PAE)	7.9 (CE) 7.8 (PAE)	18.4	21 (CE) 16 (PAE)	7.2	0.24 (P_{OUT}/P_{DC})	0.24 (P_{OUT}/P_{DC})
EVM (%)	10.9	11.6	5.6	4.7	5.5	6.8	8
Area (mm^2)	1.11 (0.58**)		4.19	1.62	0.19**	2.98	

Conclusion

- **Power combining Doherty PA architecture**
  - ✓ Achieves hybrid power combining and broadband active load modulation.
- **8-way low-loss slotline-based power combiner**
  - ✓ A practical alternative to the conventional transformer with a compact layout.
- **The D-band PA**
  - ✓ Achieves 22.7/22.6/22.4dBm P_{SAT} with 18.7/17.2/16.1% peak PAE and 12.1/11.7/9.8% back-off PAE at 110/120/130GHz.
  - ✓ Supports 16-QAM and 64-QAM signals and achieves 13.81/13.74dBm P_{AVG} and 8.01/7.88% CE_{AVG}.

Acknowledgement

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Thanks !