Student Paper Finalist

RMo3A-1

A Sub-THz CMOS Molecular Clock with 20 ppt Stability at 10,000 s Based on Dual-Loop Spectroscopic Detection and Digital Frequency Error Integration

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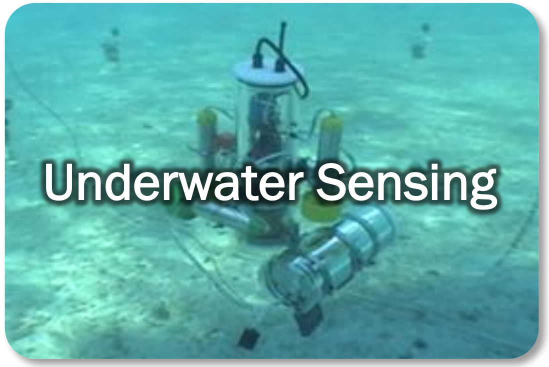
Outline

- Motivation and Background
- Prior Arts
- Proposed Chip-Scale Molecular Clock
- Measurement Results
- Conclusions

Motivation

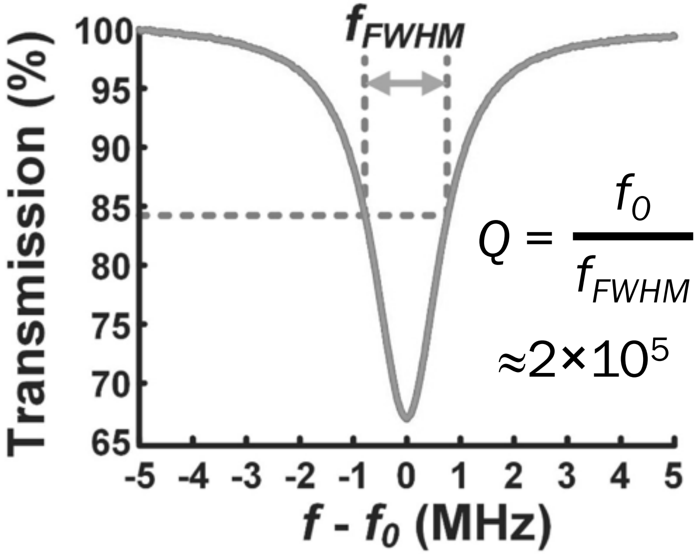
- Highly-stable frequency reference (i.e. clock) is one of the key technologies for a wide range of applications

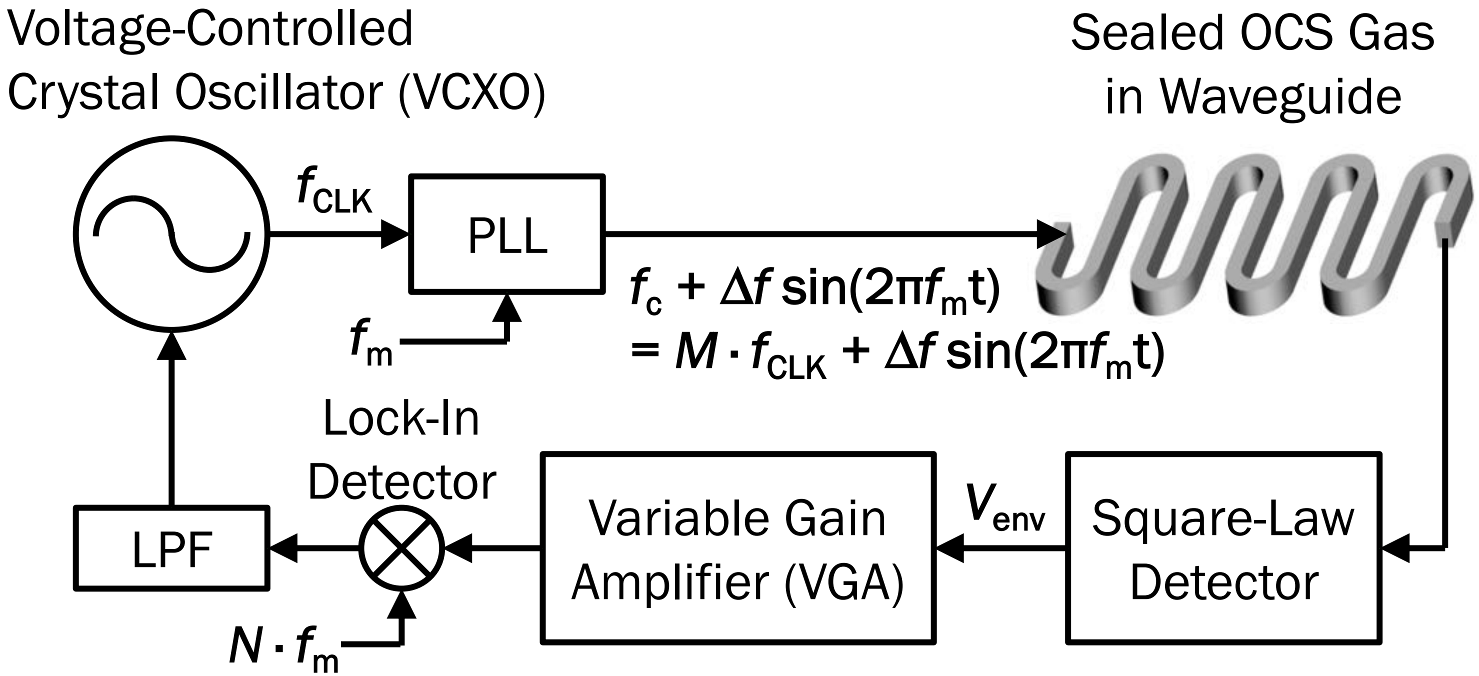


- Chip-scale molecular clocks provide high stability at low cost by using rotational spectrum of molecules in sub-THz range.

	Stability	Cost	Power
Crystal/MEMS Oscillators	10^{-4} – 10^{-8}	< $1	~ 1mW
Oven-Controlled Crystal/MEMS Osillators	~ 10^{-10}	~ $100	~1W
Chip-Scale Atomic Clocks (CSACs)	~ 10^{-11}	> $1000	~100mW
Chip-Scale Atomic Clocks (CSMCs)	~ 10^{-11}	~ $10	~100mW

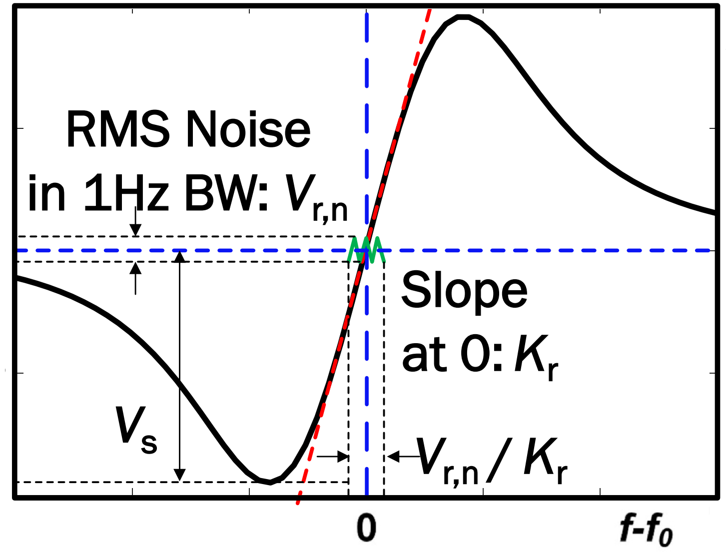
Sub-THz Molecular Clock





- Narrow transition line of carbonyl sulfide (OCS) at f_0 = 231.061 GHz
- High stability against environmental variations
- f_{CLK} inherits the stability of OCS absorption line since f_c is locked to f_0

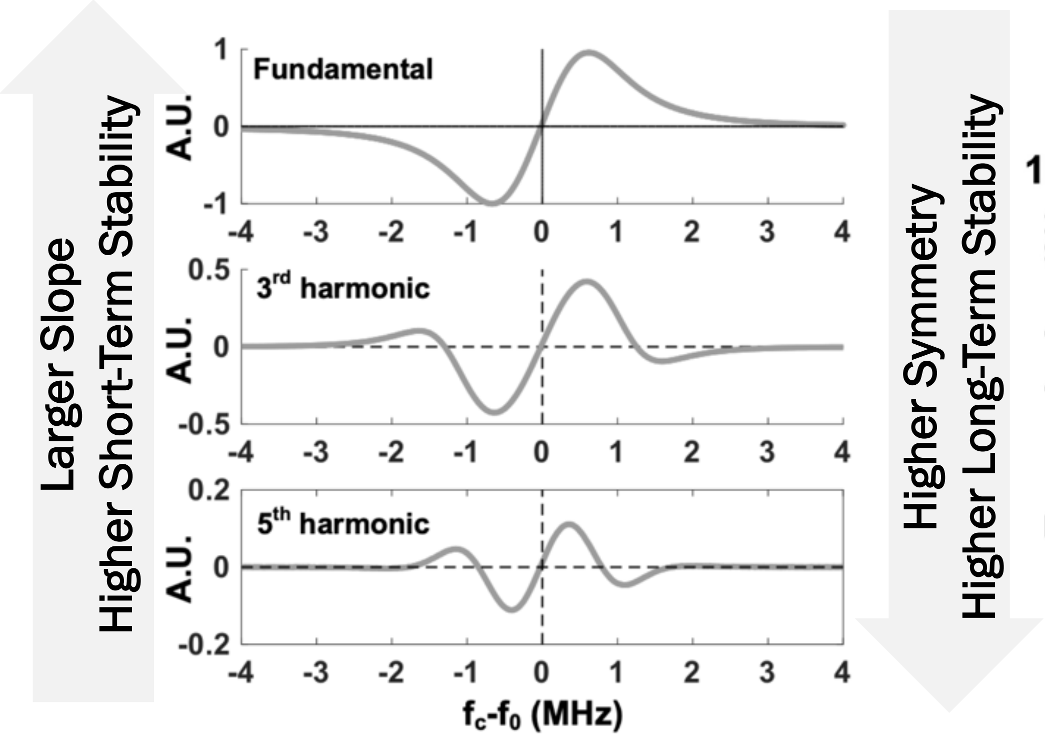
Spectral Curves and Frequency Locking

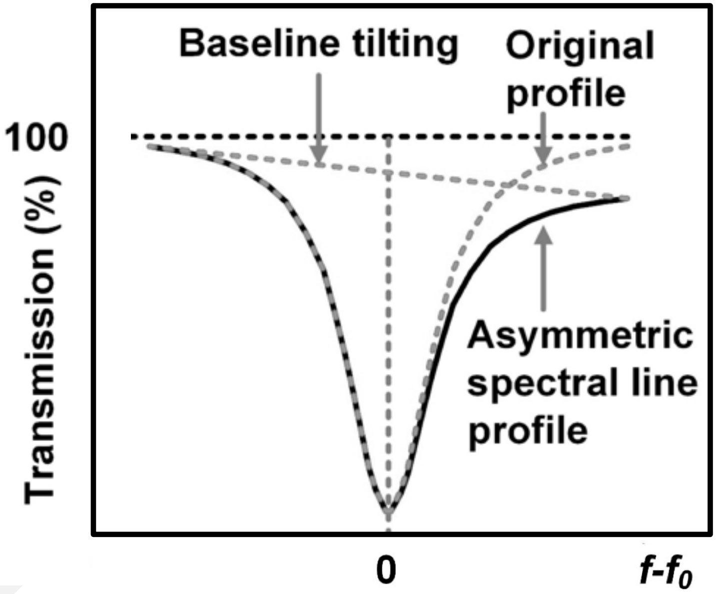


Allan Deviation:

$$\sigma_y(\tau) = \frac{V_{r,n}}{\sqrt{2\tau} \cdot K_r \cdot f_0} \propto \frac{V_{r,n}}{\sqrt{\tau} \cdot V_s \cdot Q}$$

N^th-Order Harmonic Spectral Curves



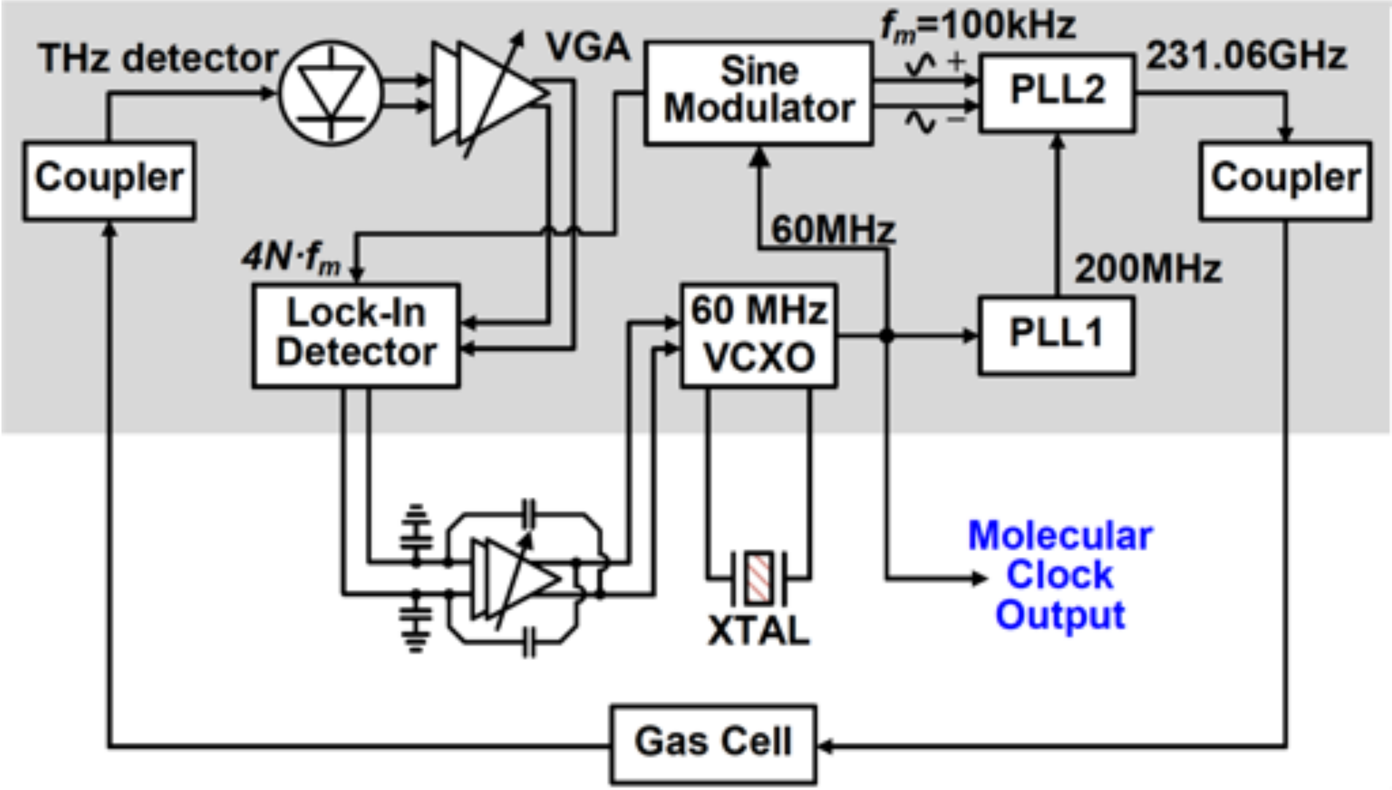


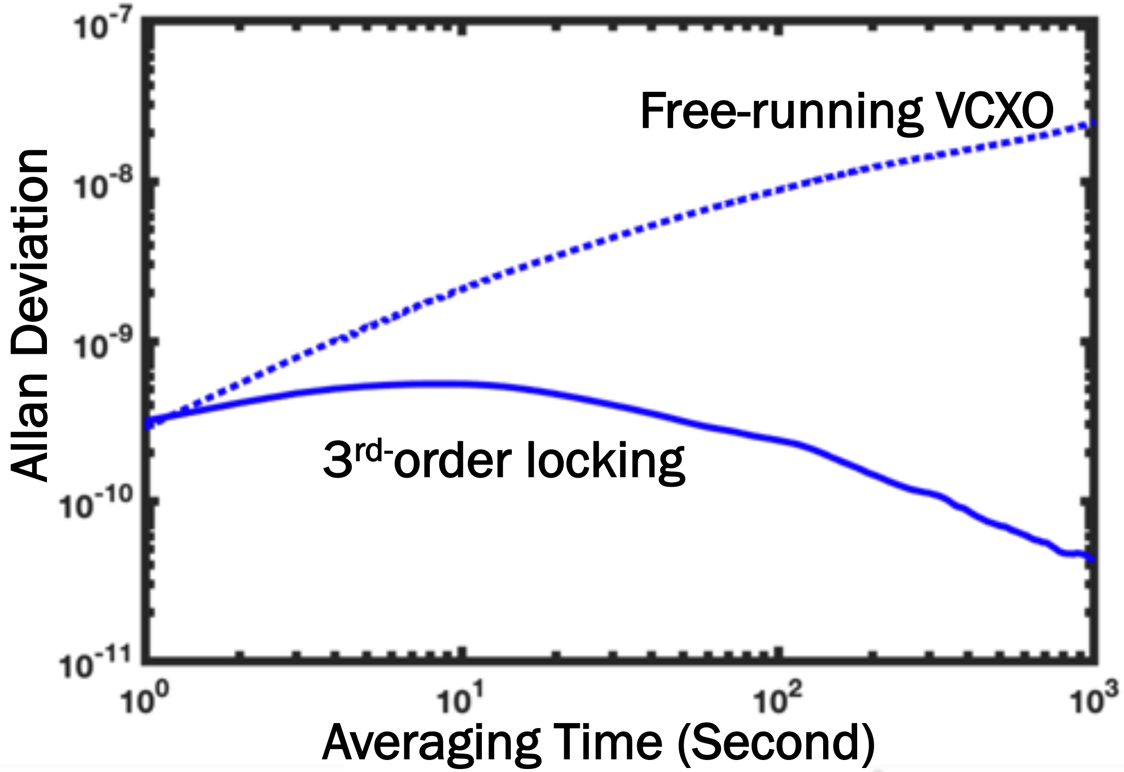
Transmission
= Baseline Tilting
+ Spectral Line Profile

Prior Chip-Scale Molecular Clock (CSMC)

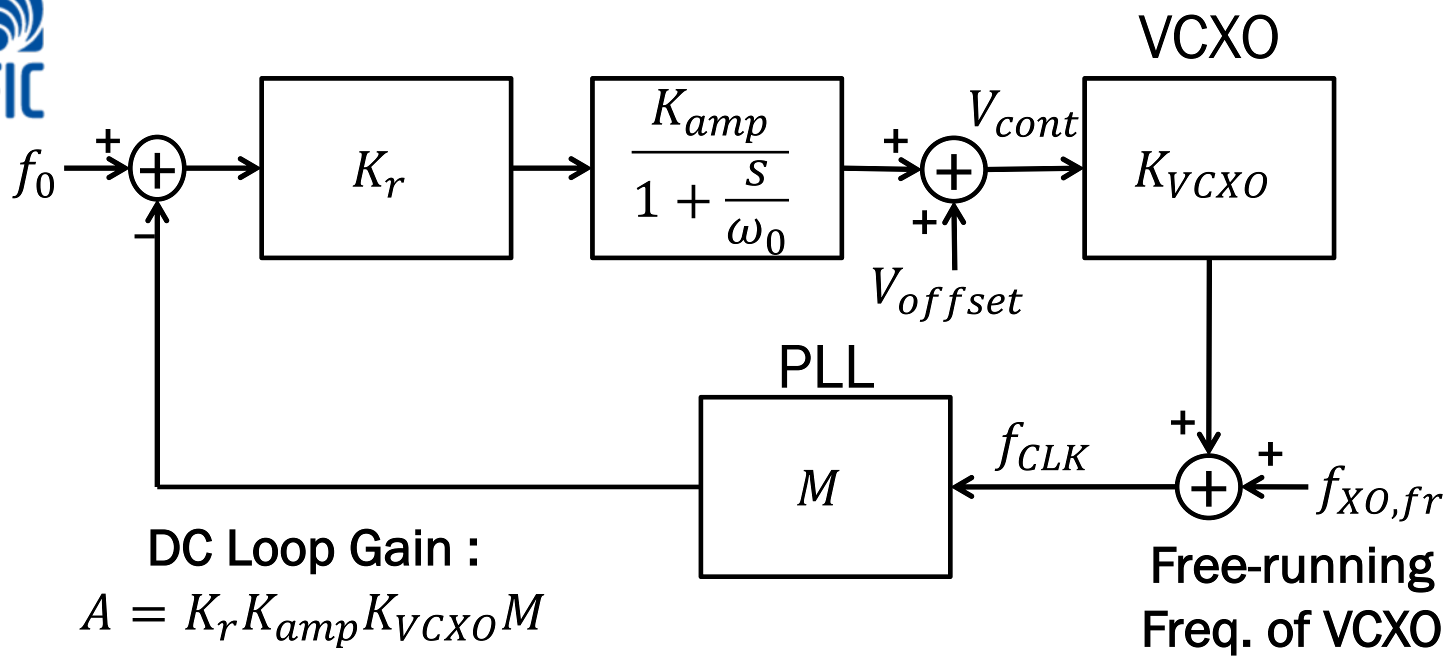
- 3rd-order detection was used for locking
- $\sigma_y = 3.2\times10^{-10}$ @ $\tau = 1$s, $\sigma_y = 4.3\times10^{-11}$ @ $\tau = 10^3$s

[C. Wang, *JSSC*, 2021]





Problems in Prior CSMCs



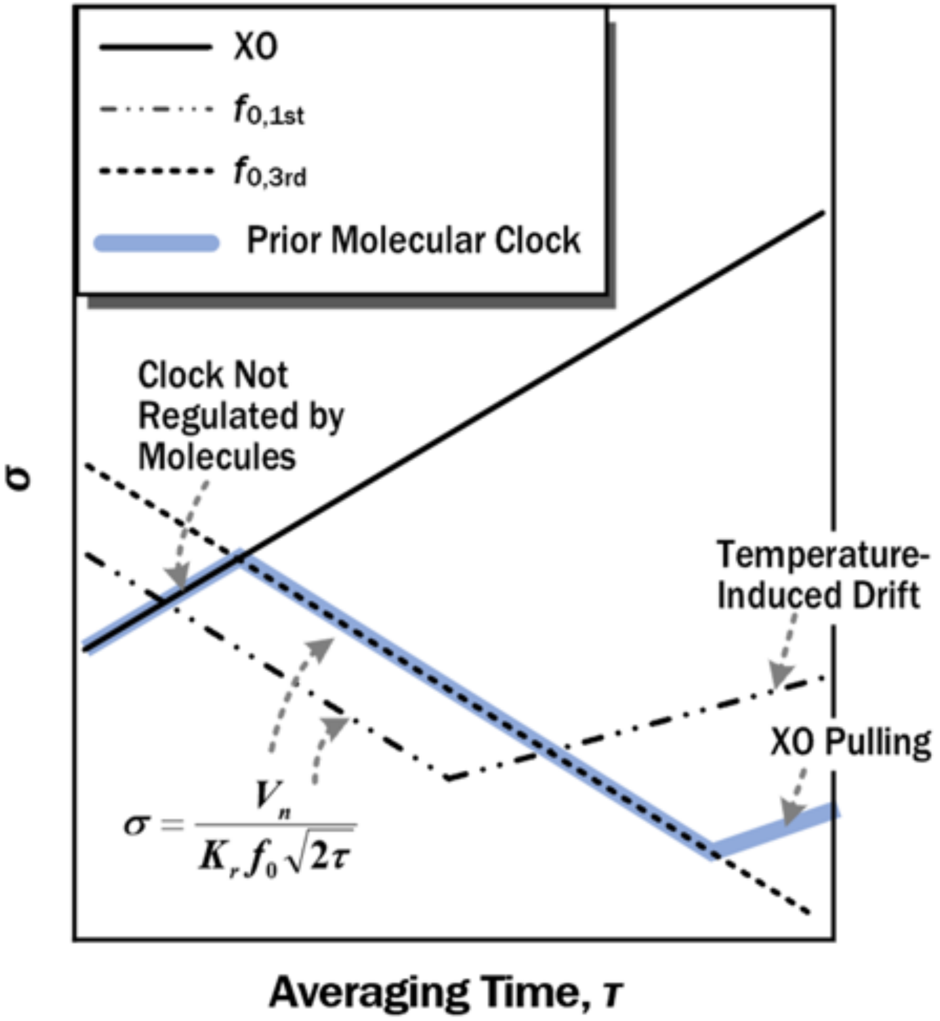
$$\frac{f_{CLK}}{f_{XO,fr}} = \frac{1}{1+A} \cdot \frac{1+\frac{s}{\omega_0}}{1+\frac{s}{\omega_0(1+A)}}$$

$$\frac{f_{CLK}}{V_{offset}} = \frac{K_{VCXO}}{1+A} \cdot \frac{1+\frac{s}{\omega_0}}{1+\frac{s}{\omega_0(1+A)}}$$

- Long-term stability is limited by the finite loop gain
- Large amplifier gain (K_{amp}) is required to suppress the effect of V_{offset} variations, but K_{amp} is limited due to high even-harmonic components
- Lower SNR in high-order detection due to smaller K_r

Problems in Prior CSMCs

- Theoretical stability limit of high-order locking is higher than fundamental locking
- Molecular regulation is not provided for τ < 20 s
- Long-term variation and temperature sensitivity of VCXO affects the clock's long-term stability (XO Pulling)



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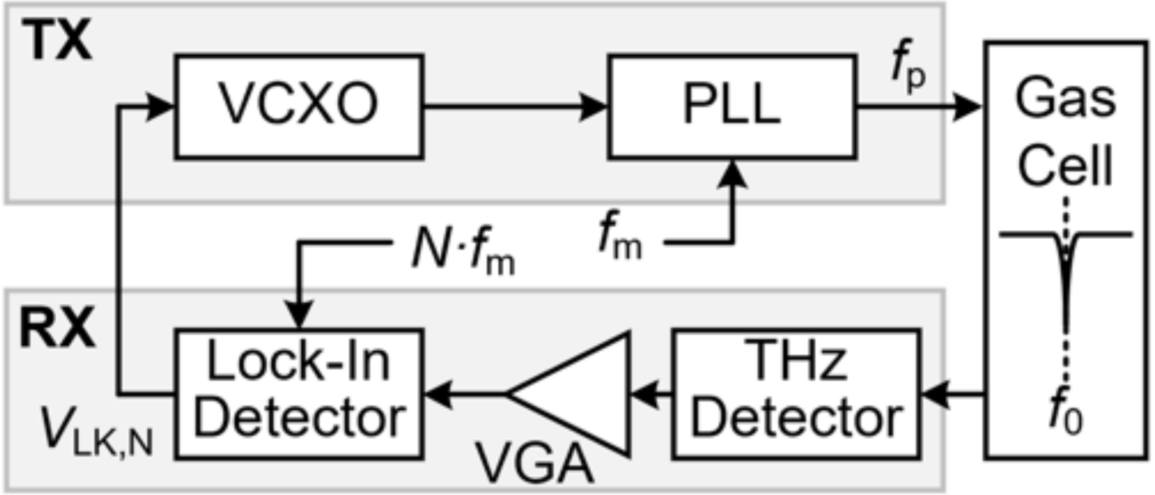
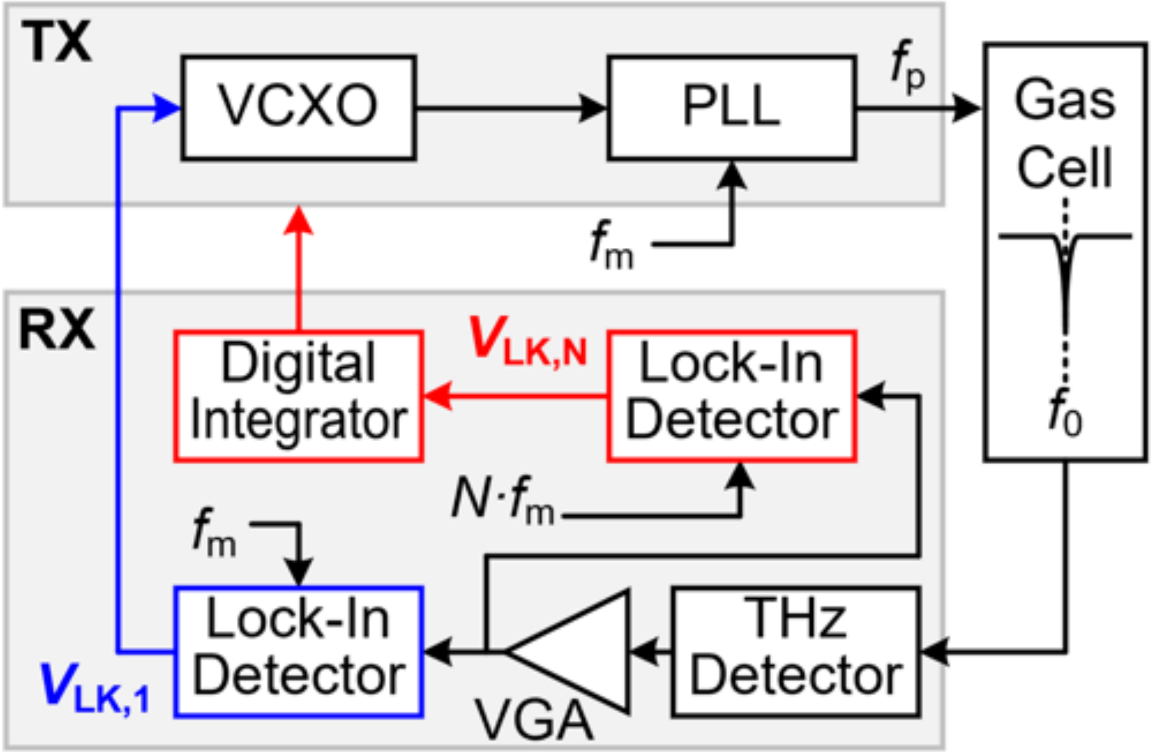
Proposed Chip-Scale Molecular Clock

Prior Architecture

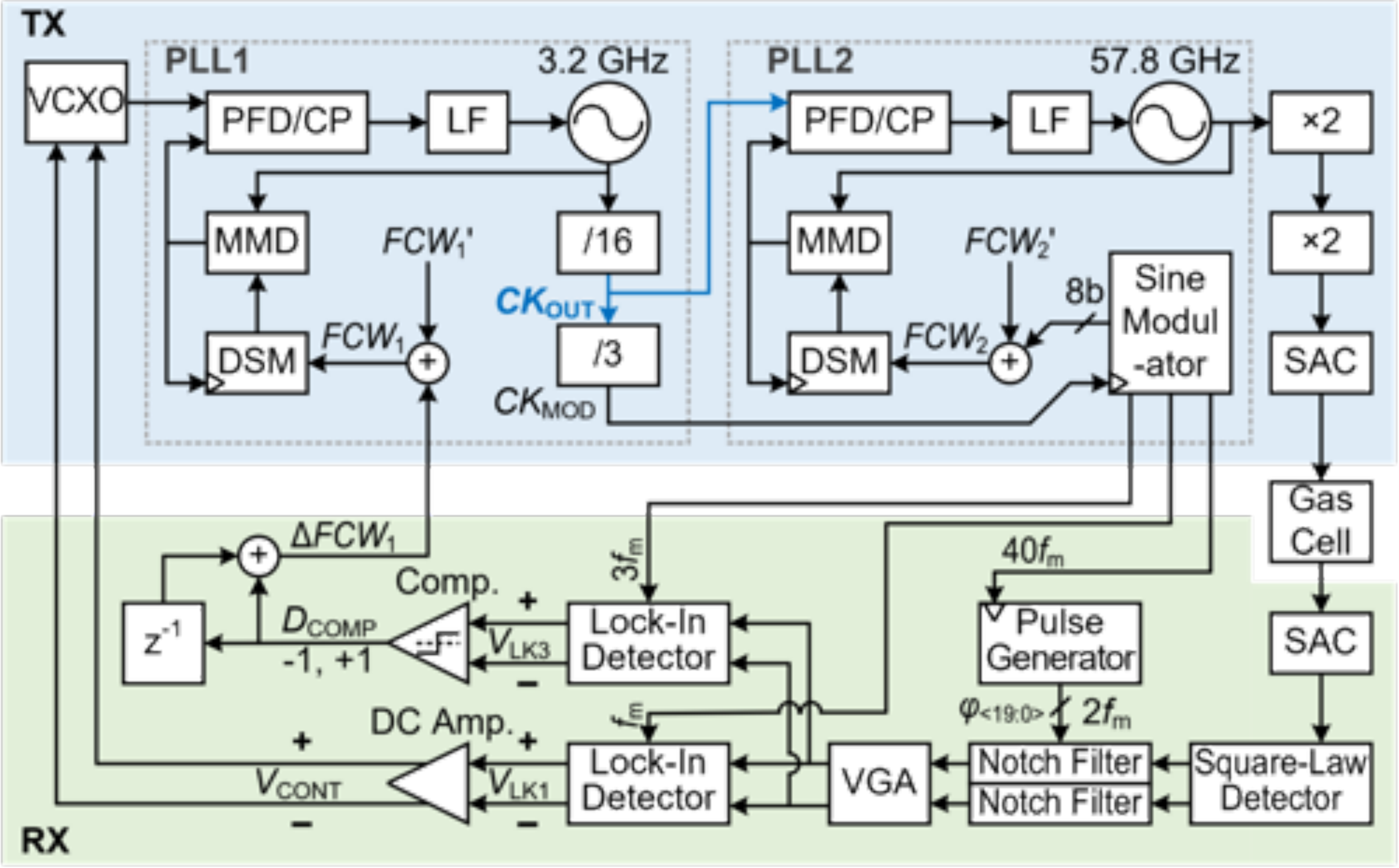


Proposed Architecture

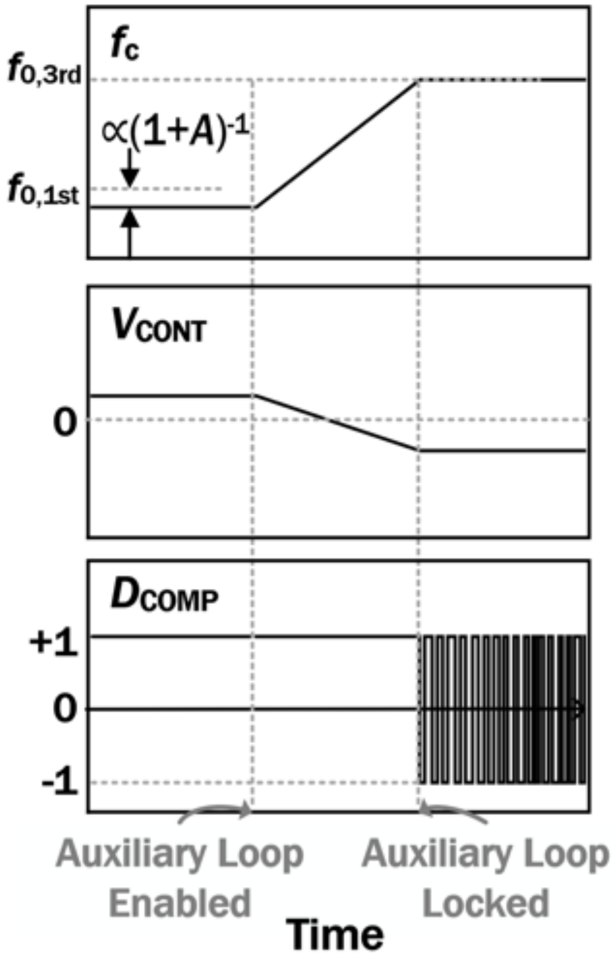


- High SNR from fundamental-mode probing (in the main loop)
- Low long-term drift from high-order probing (in the auxiliary loop)

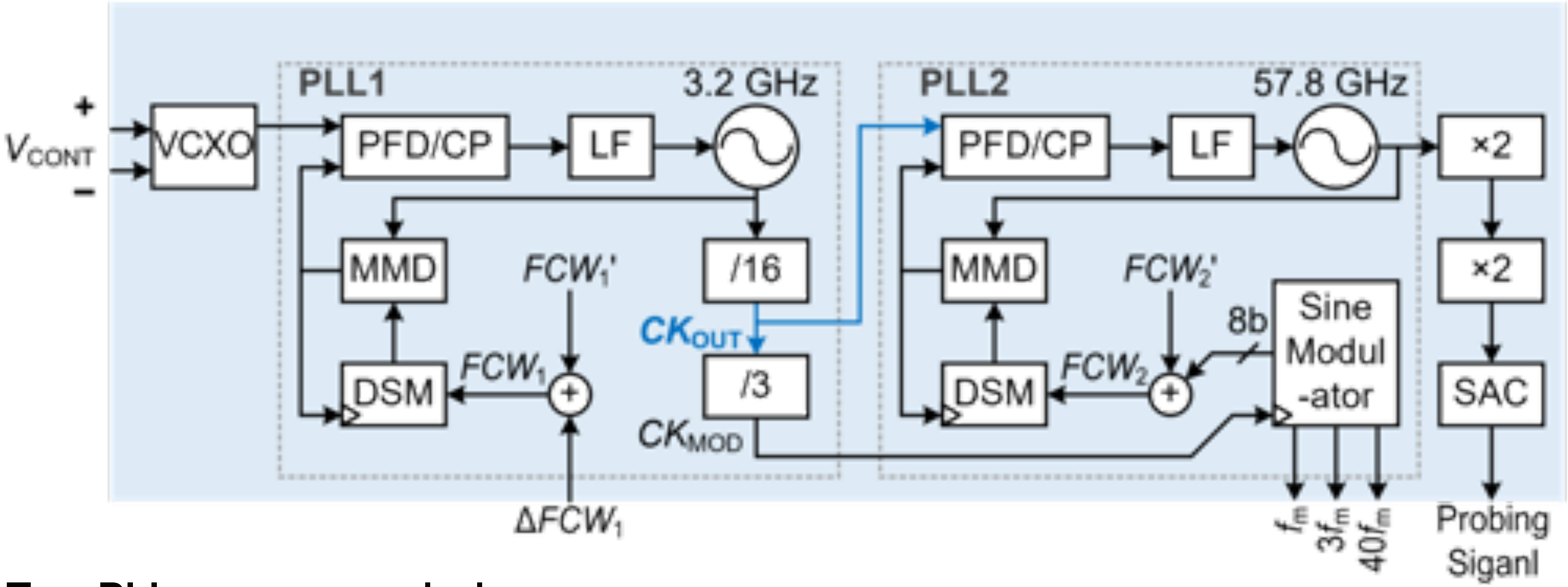
Proposed Architecture



Timing Diagram

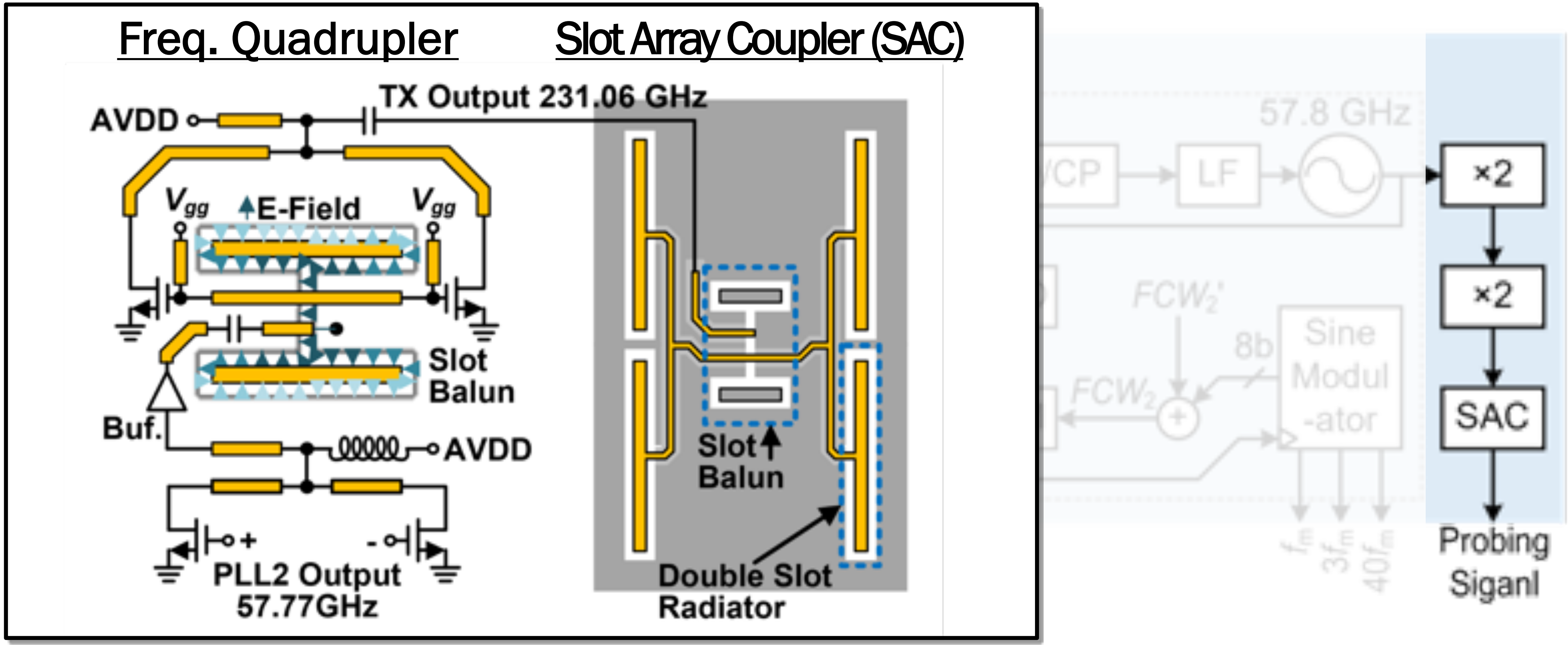


Transmitter (TX) Architecture



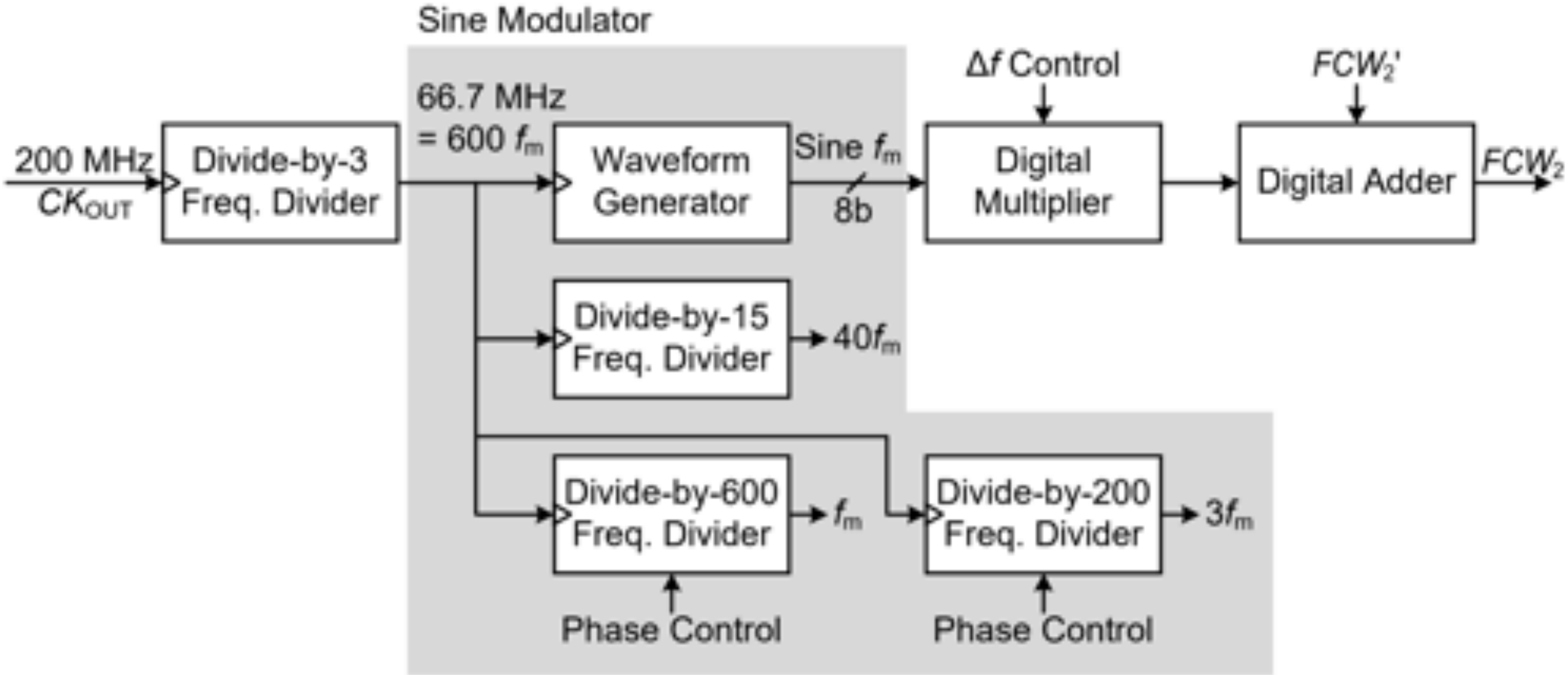
- Two PLLs are cascaded
- 36-bit DSMs are used
- Sine modulation with modulation frequency of f_m is applied in PLL2

Transmitter (TX) Architecture



- Simulated THz power of the quadrupler output = -4.4dBm
- Simulated loss of the SAC = 5.2 dB

Transmitter (TX) Architecture



- Sine modulator generates $40f_m$, $3f_m$, and f_m clocks and 8-bit sine wave
- f_m = 111 kHz

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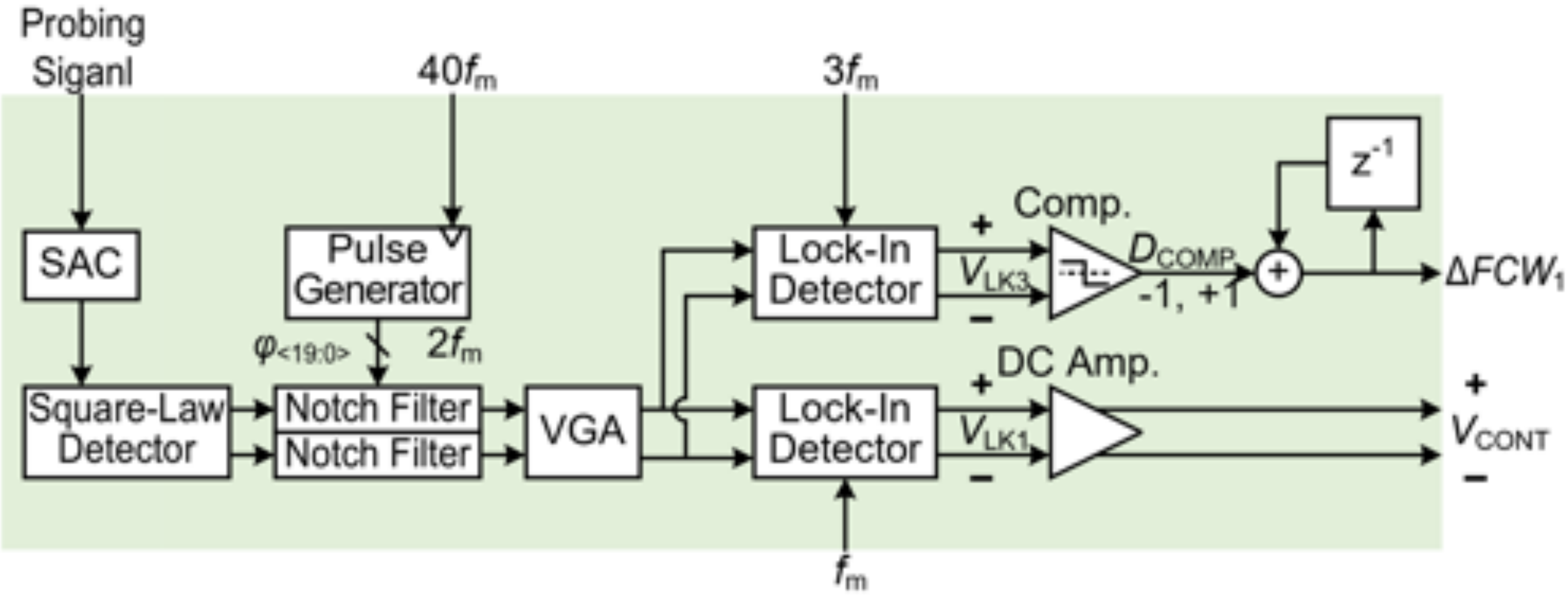
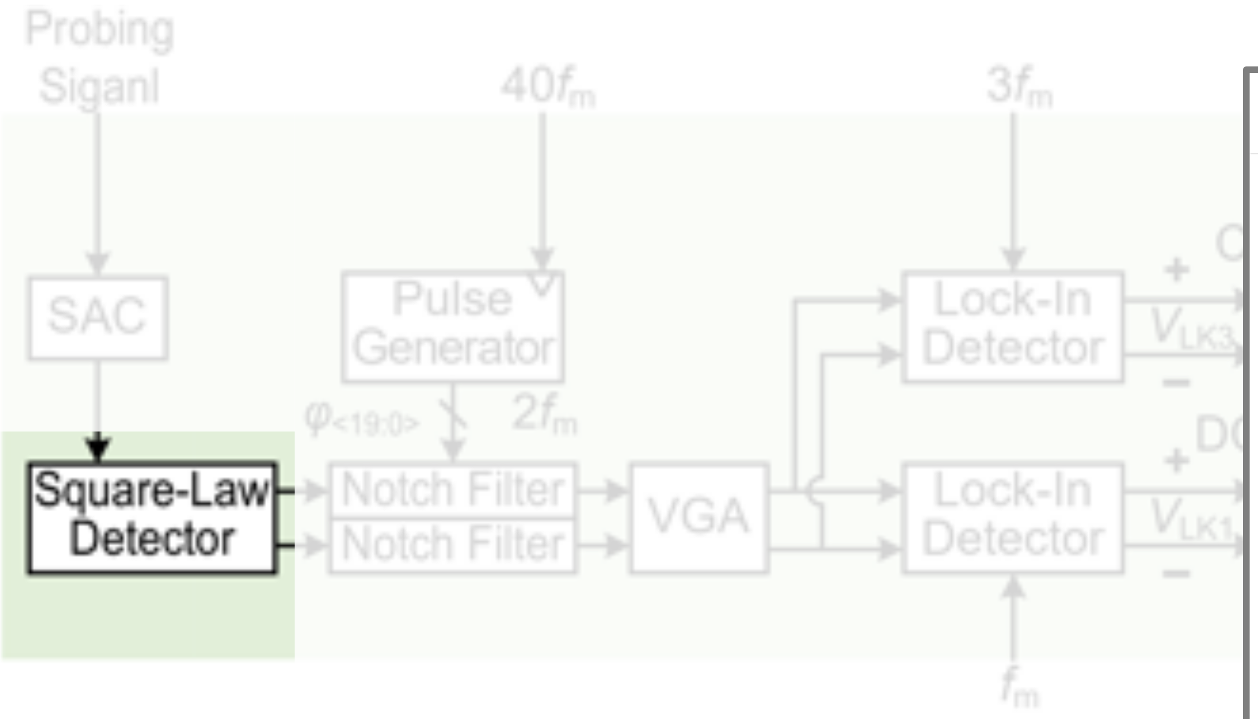
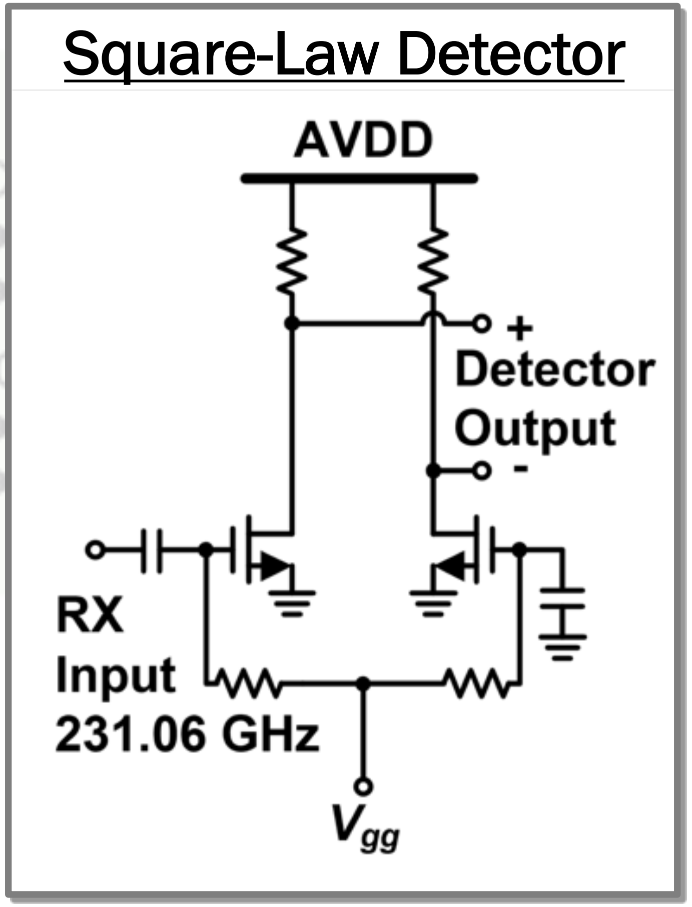
Receiver (RX) Architecture



- Fundamental detection’s output controls the VCXO (main loop)
- 3rd harmonic signal is followed by a comparator and a digital integrator and its output controls the frequency control word of the PLL1. (auxiliary loop)

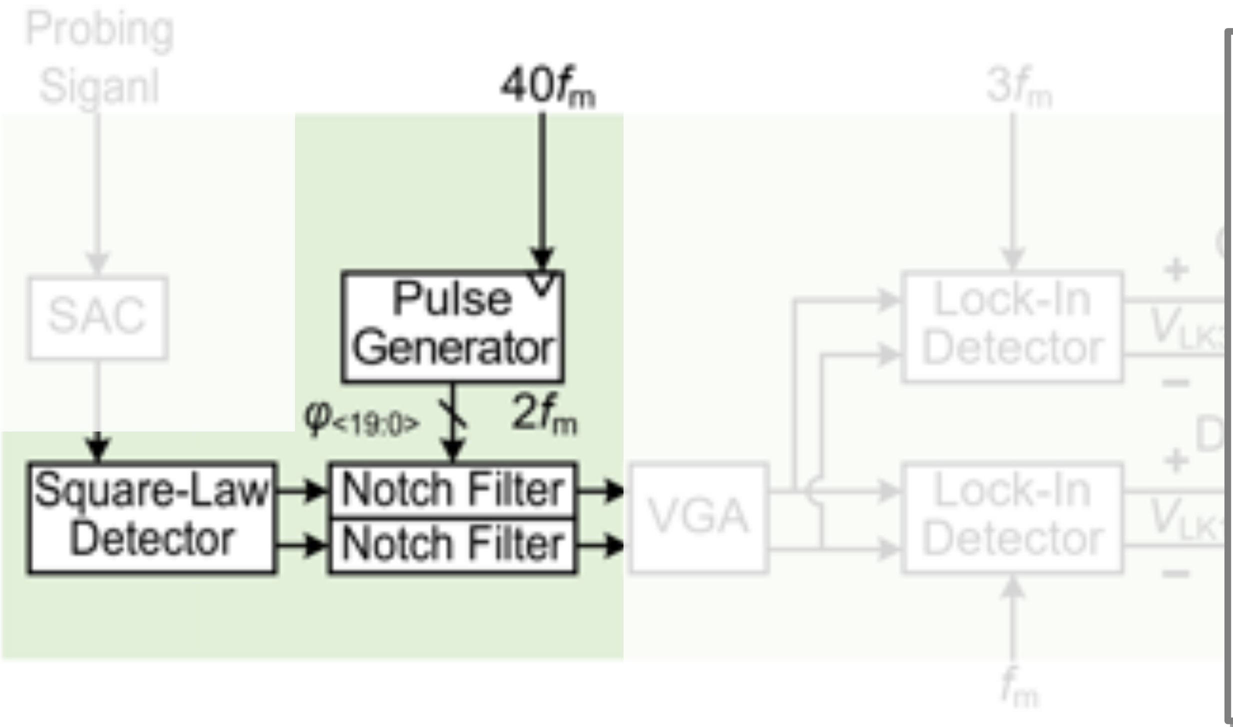
Receiver (RX) Architecture

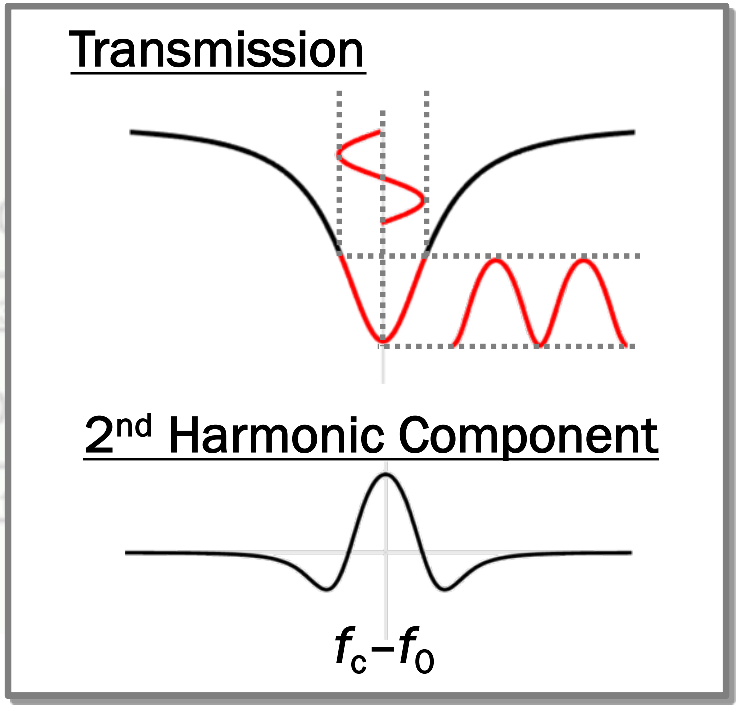




- Sub-threshold NMOS pair is used as a low noise THz square-law detector

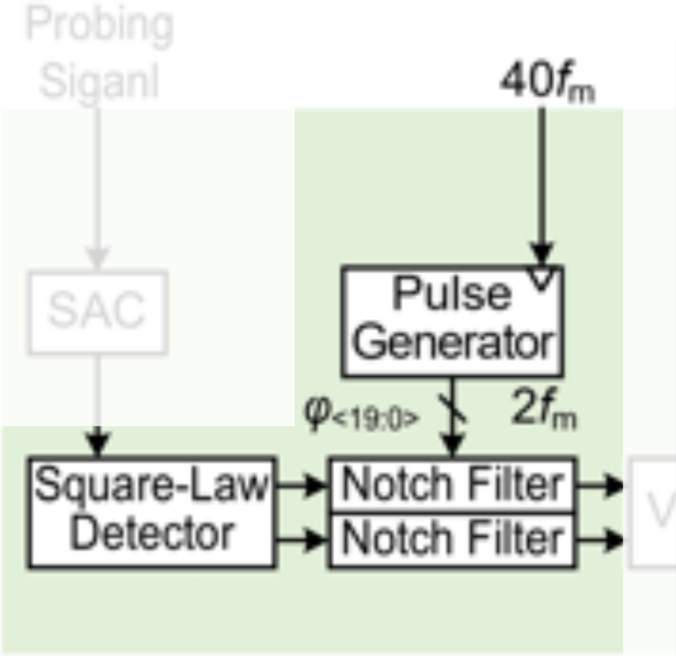
Receiver (RX) Architecture

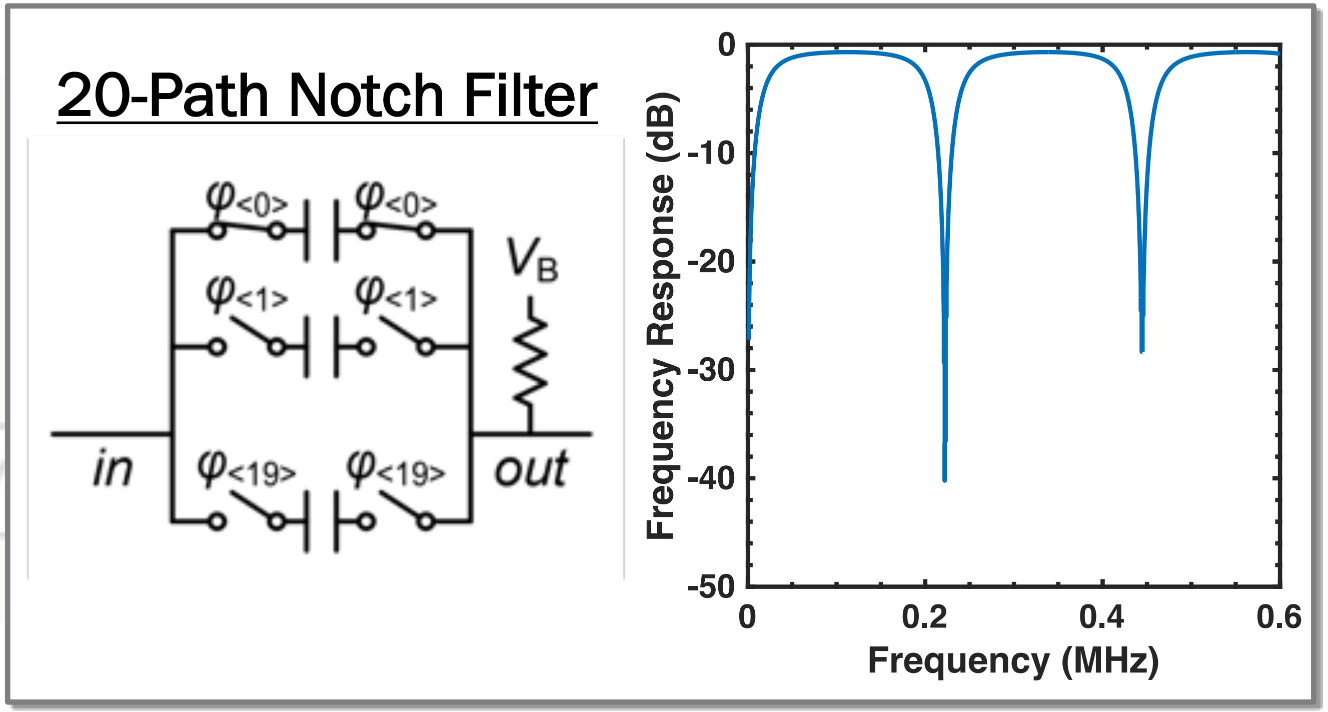




- Even harmonic components have large amplitude and can limit K_{amp}
- Notch filters are used to reject the signal at $2f_m$, $4f_m$, ...

Receiver (RX) Architecture





- Even harmonic components have large amplitude and can limit K_{amp}
- Notch filters are used to reject the signal at $2f_m$, $4f_m$, ...
- 20-phase non-overlapping clock signals generated by a pulse generator drive the switches in notch filters

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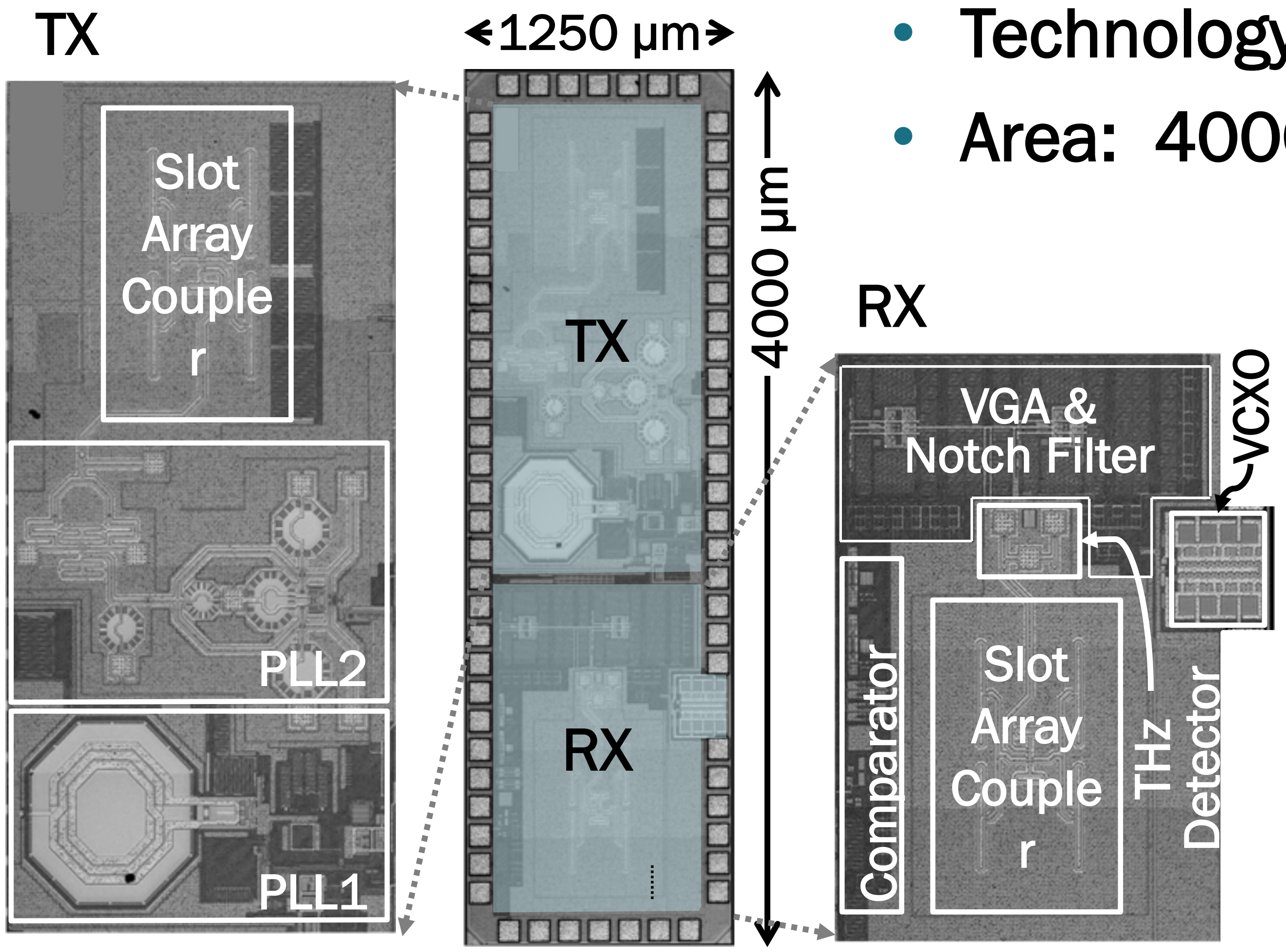
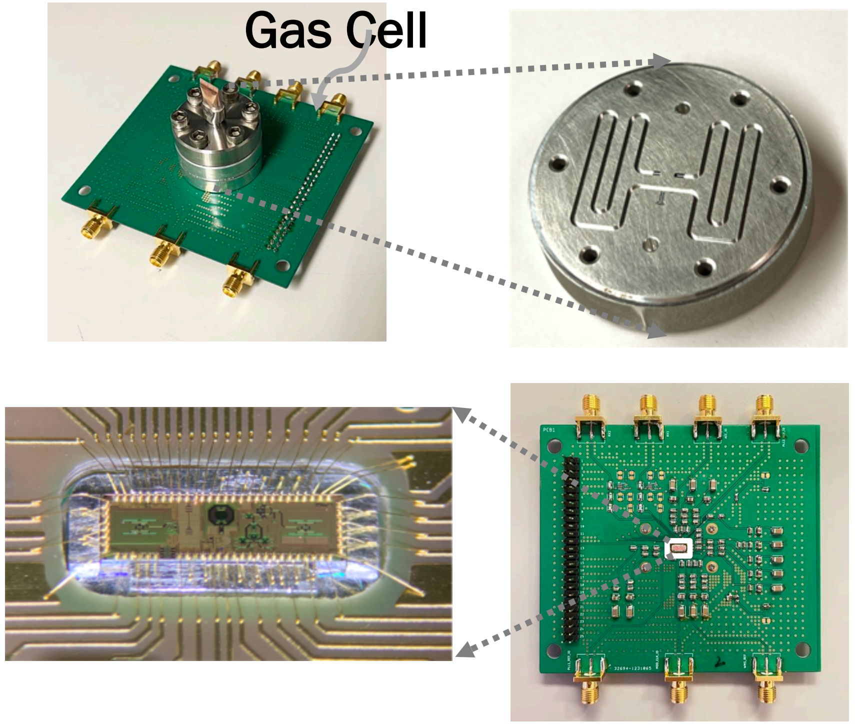
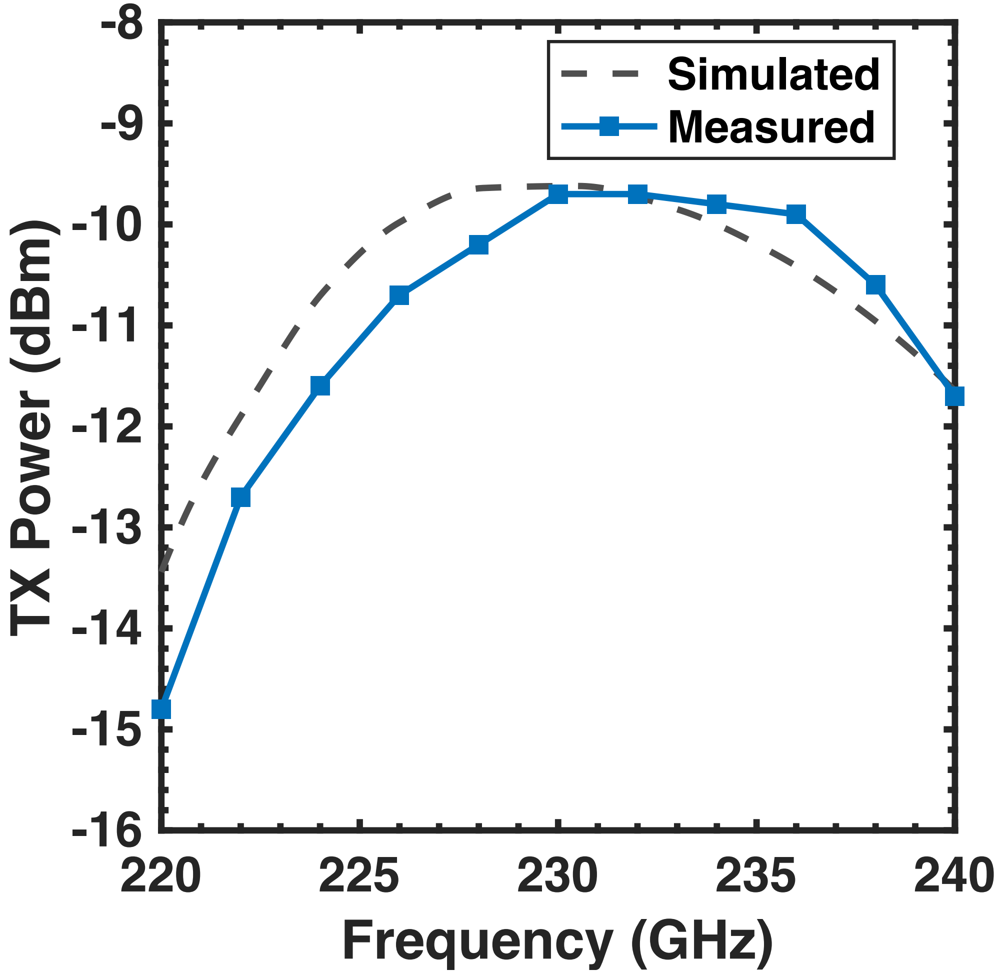
Chip Micrograph and Packaging

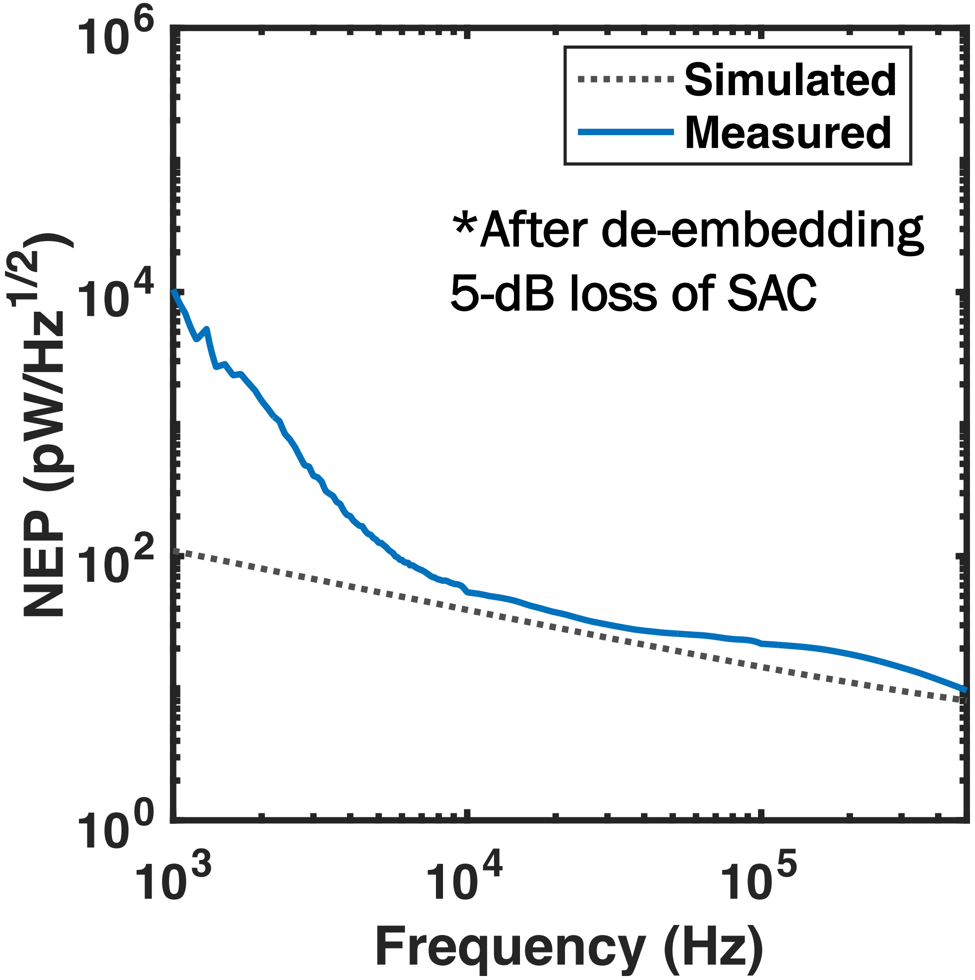
- Technology: TSMC 65 nm CMOS (GP)
- Area: 4000 µm × 1250 µm





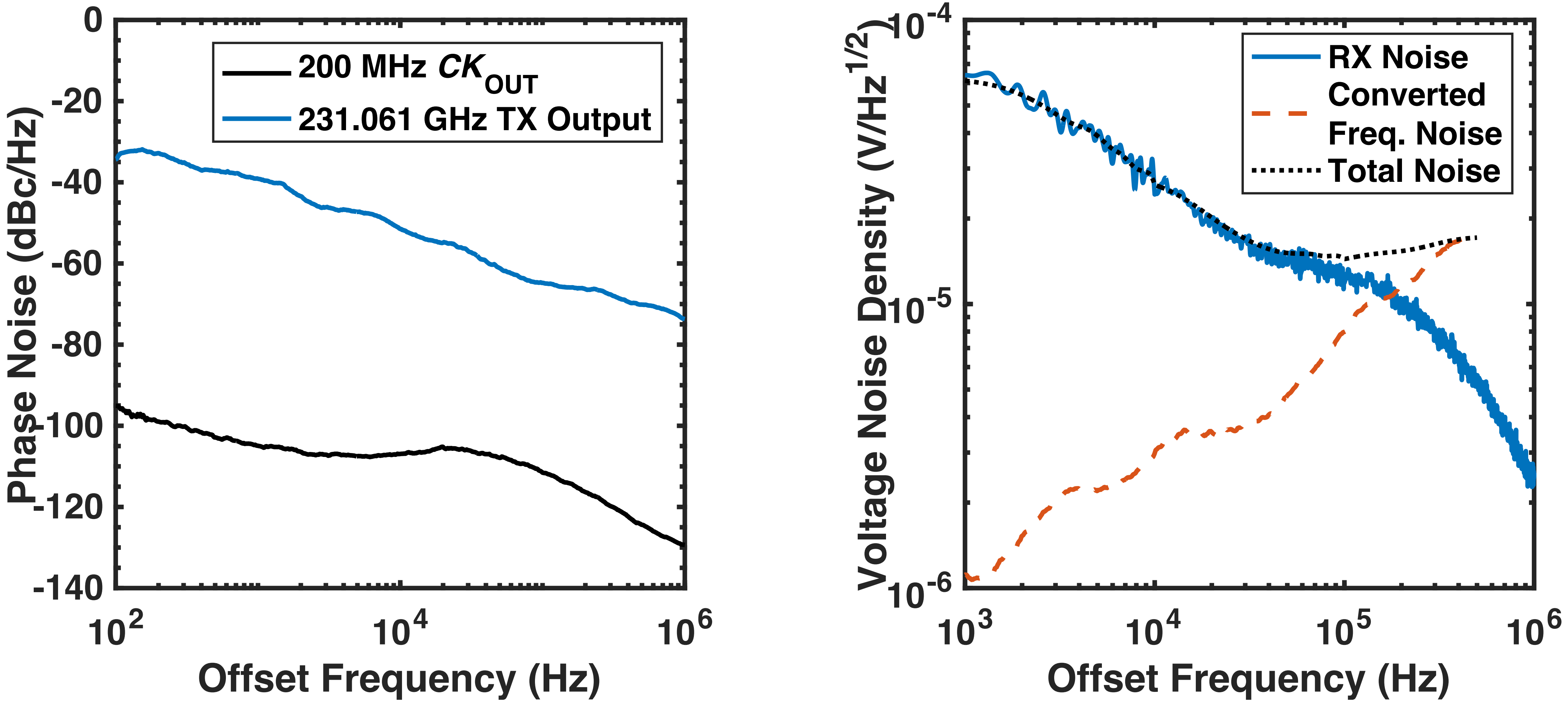
Measurement Results: TX/RX Performance





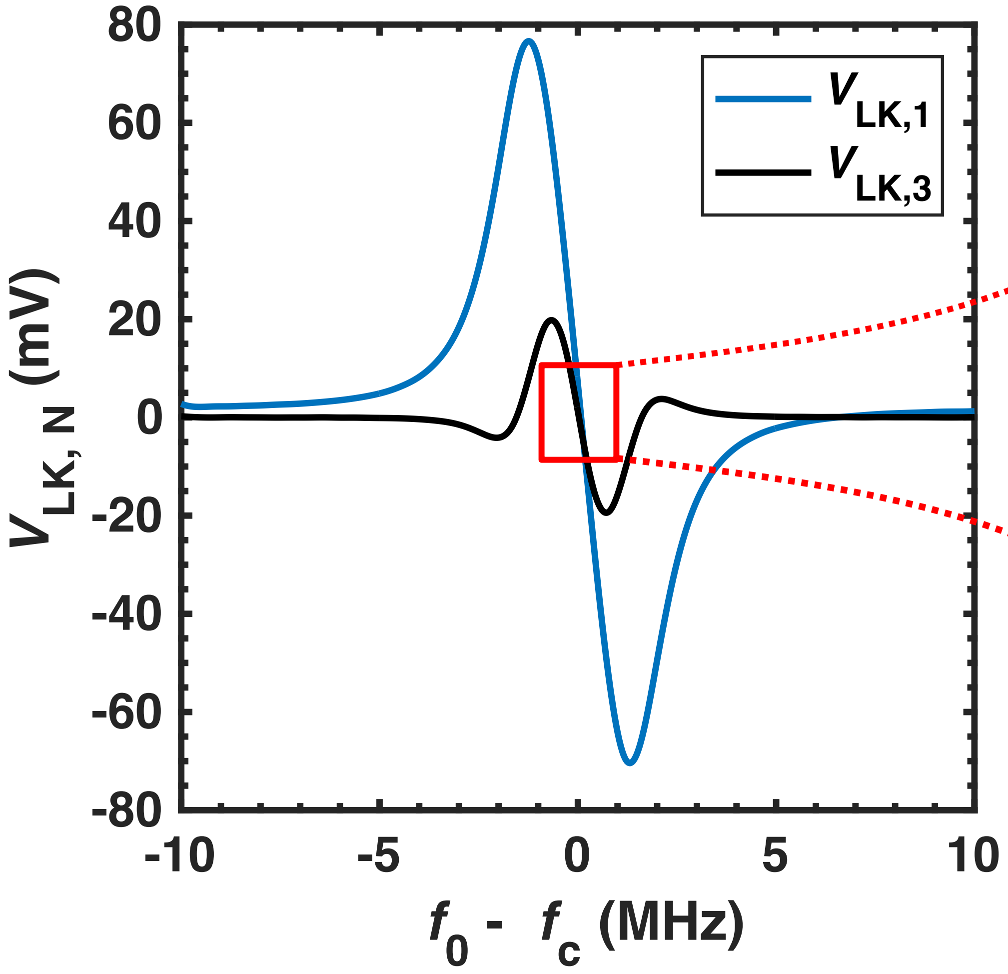
- P_{RF} = −9.7 dBm
- NEP of RX @ f_m = 21.4 pW/Hz$^{1/2}$

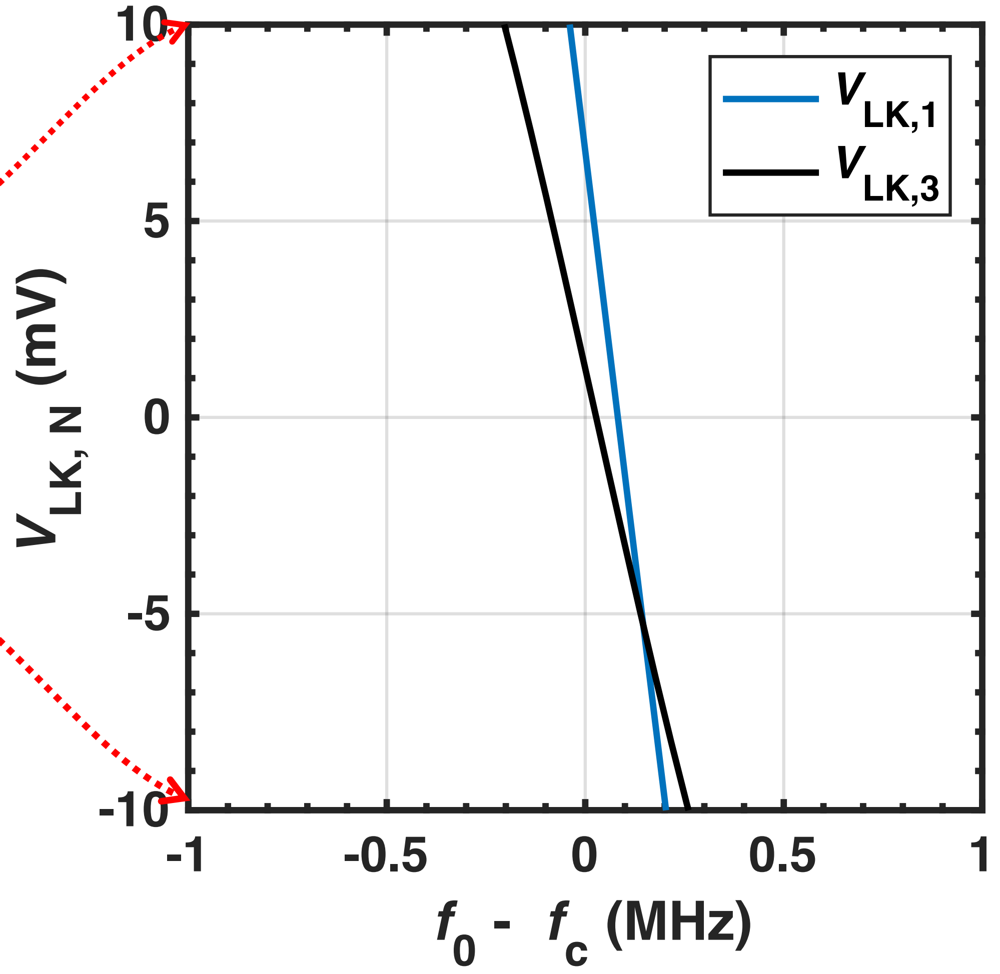
Measurement Results: Phase Noise



- PN_{RF} @ $2f_m$: −65 dBc/Hz, PN_{CKOUT} @ 1 MHz :−129 dBc/Hz

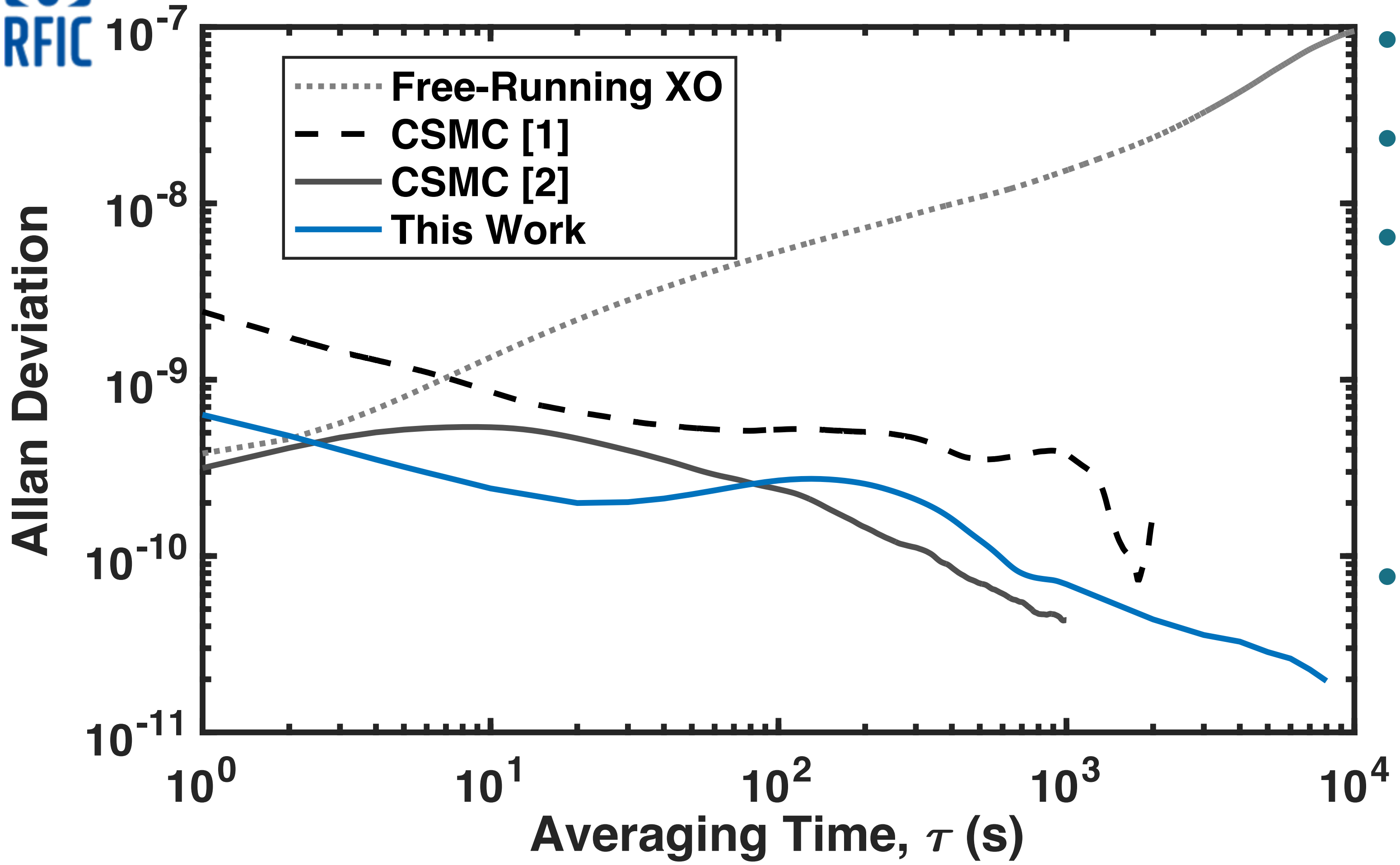
Measurement Results: Spectral Curves





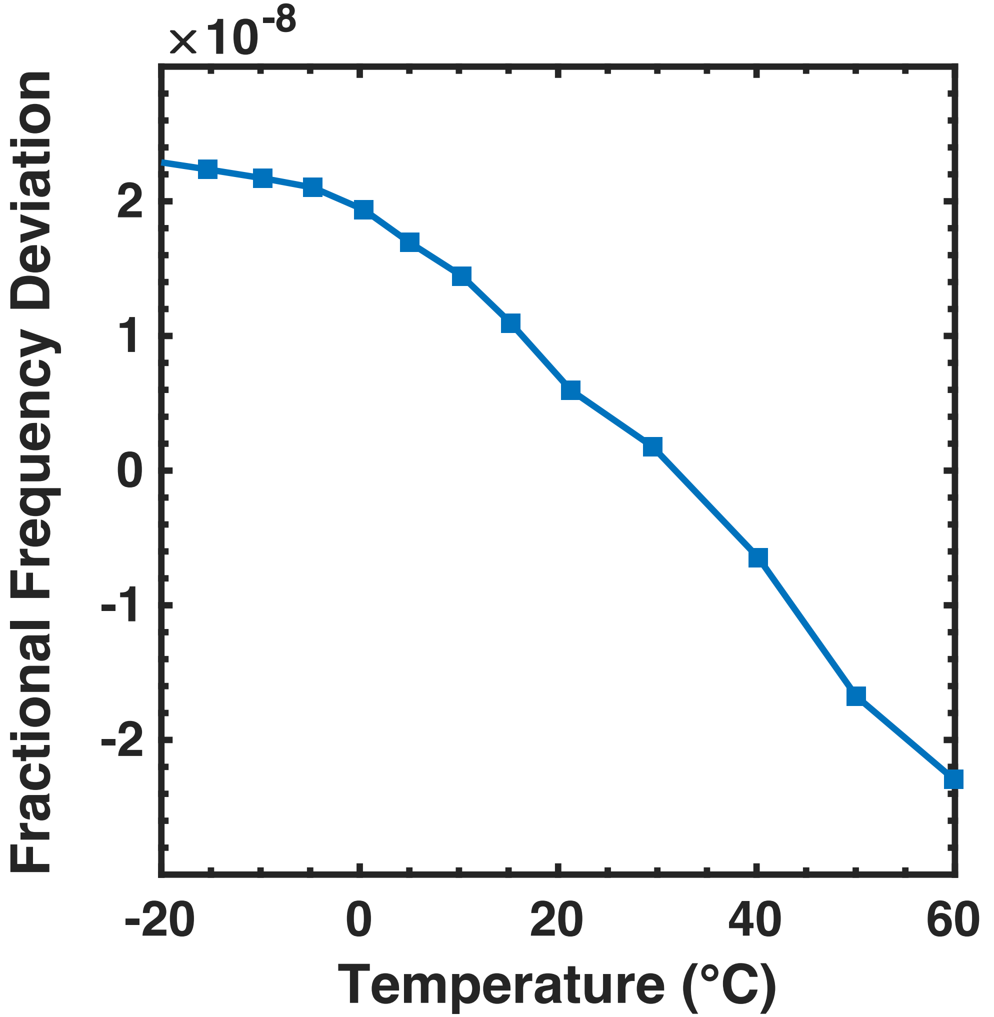
- $K_r = 8.26\times10^{-8}$ V/Hz for fundamental probing
- $K_r = 4.51\times10^{-8}$ V/Hz for 3rd-order probing

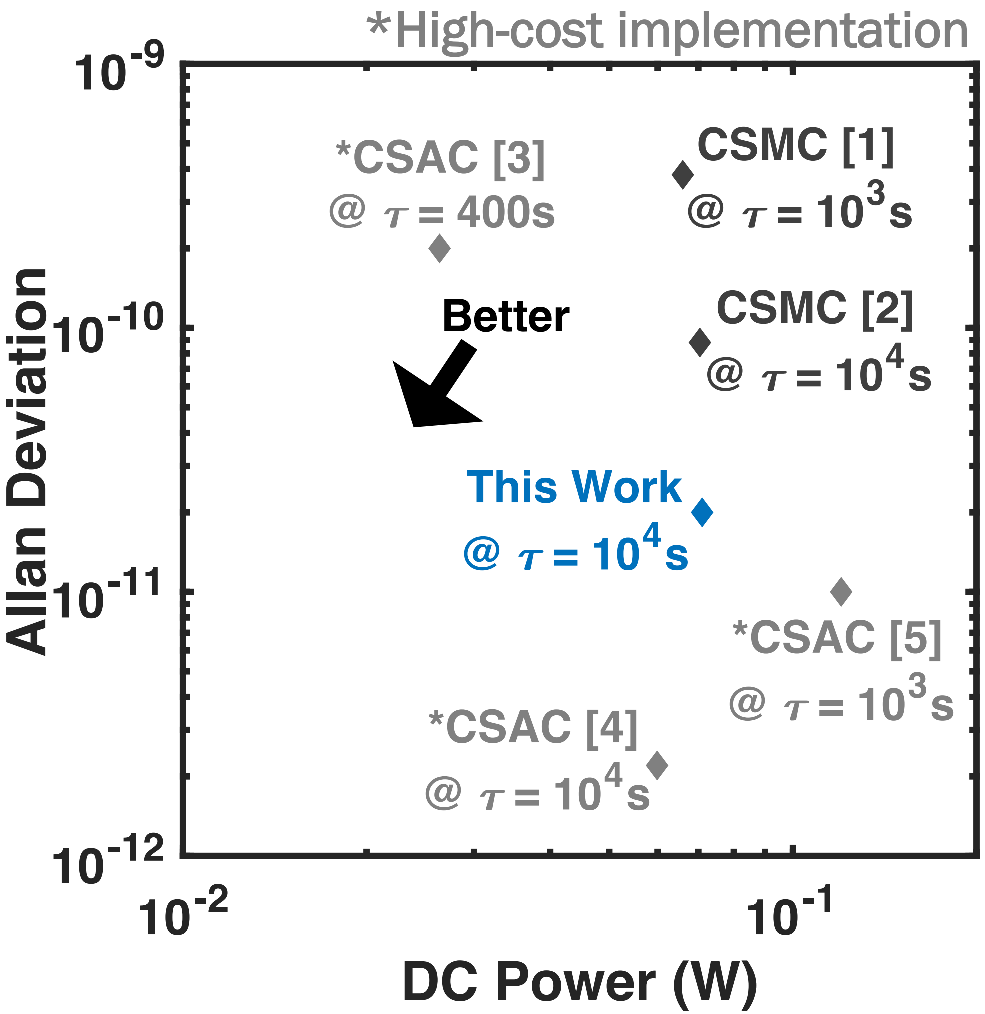
Measurement Results: Allan Deviation



- $\sigma_y = 5.4\times10^{-10}$@$\tau$=1s
- $\sigma_y = 0.2\times10^{-10}$@$\tau$=$10^4$s
- The proposed CSMC is robust against rapid environmental disturbances
- This work achieves high stability in both short-term and long-term

Measurement Results: Allan Deviation





- Average temperature coefficient: 5.8×10^{-10} °C^{-1} without temperature compensation

Performance Summary

[1] C. Wang, *JSSC*, 2019 [2] C. Wang, *JSCC*, 2021 [3] D. Ruffieux, *ISSCC*, 2011 [4] H. Zhang, *ISSCC*, 2019 [5] Microsemi, *SA.45s*, 2019

		[3]	[4]	[5]	[1]	[2]	This Work
Implementation		0.18 µm CMOS + Vapor Cell w/ Integrated Photonics	Discrete Electronics + Vapor Cell w/ Integrated Photonics and Heater + Magnetic Shield	65 nm CMOS + Vapor Cell w/ Integrated Photonics and Heater + Magnetic Shield	65 nm CMOS Chip + Sub-THz Waveguide		
Frequency Reference		Ground-State Hyperfine Transition of Atoms			Rotational Transition of Molecules		
		^{87}Rb	^{133}Cs		^{16}O^{12}C^{32}S		
Probing Freq.		3.417 GHz	4.596 GHz		231.061 GHz		
Order of Locking		N/A			1st	3rd	1st + 3rd
ADEV (10^{-10})	τ=1s	4	0.67	3	24	3.2(Unlocked)	5.4
	τ=10s	1.2	0.6	1	8.6	5.4	2.4
	$\tau=10^4$s	2(@τ=400s)	0.05	N/A	N/A	0.88	0.2
Avg. Temp. Coeff.†		N/A	0.07×10^{-10}/°C	0.13×10^{-10}/°C	N/A	28×10^{-10}/°C††	5.8×10^{-10}/°C††
DC Power		26‡	60	120	66	70	71

†Defined as (Temperature-induced frequency drift)/(Temperature range), ††w/o temp. compensation,
‡The power of the physics package and signal processing is not included.

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Conclusions

- CSMC can provide high stability at low cost
- Dual-loop CSMC improves Allan Deviation by combining high SNR of fundamental transition probing and environmental robustness of high-order transition probing.
- Digital integration in the frequency-locked loop provides high gain.
- Without temperature compensation, Allan Deviation of $\sigma_y = 2\times10^{-11}$ @ $\tau = 10^4$ s was achieved.

Acknowledgement

- This work is supported by JPL and NSF.
- The authors acknowledge Dr. Stephen Coy, Prof. Keith Nelson, and Prof. Robert Field of MIT for technical discussions and assistance.

Thank You