



# Integrable timing on silicon wafer supporting CubeSats-based Communications, Navigation and Radio Science

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**The paper presents the effort of embedding precision timing into silicon integrated chip platforms in the context of CubeSats-based communications, navigation, and radio science missions. The paper also discusses the fabrication and characterization of a terahertz silicon micromachined waveguide, which will serve as the gas cell inside the chip-scale molecular clocks (CSMCs) previously developed by the MIT team. This technology is a critical step for CSMCs to be feasibly integrable into aerospace electronic systems for CubeSats missions.**

## I. Instructions

The temperature-compensated crystal oscillators, known as TCXOs, have been the backbone time-keepers in almost all deep space missions. Most notably, the JPL IRIS deep space transponder relies on the TCXO to provide frequency reference. The time-keeping performance of the electronics system plays important role in science missions that require correlating distributed space assets. Examples include radio interferometry missions like SunRISE [1], FARSIDE [2]; ranging missions like GRACE, GRACE-FO, and LISA; and bistatic/multi-static radar missions. Inter-satellite optical communications [3][4][5] with much higher carrier frequency may further catalyze the fusion of high data rate and high-performance phasing technology that relies on miniaturized timekeeping solutions. Chip-scale atomic clocks (CSACs) [6] emerge as an important timing solution in missions where onboard clocks are needed.

Recently chip-scale molecular clocks (CSMCs) [7][8][9] have demonstrated promise as ultra-stable frequency references that rival the stability of chip-scale atomic clocks (CSACs) with similar size, weight, and power (SWaP). By probing the terahertz (THz) rotational transitions of gas polar molecules, the fully-electronic CSMCs based on a CMOS THz spectrometer chip offer lower construction complexity, less sensitivity to magnetic fields, and most importantly, much lower cost than CSACs due to the silicon platform compatibility with the semiconductor industry. CSMCs achieved an instability of 20 parts per trillion with an averaging time of 10,000s. A simplified schematic of the CSMC is shown in Fig.1a. A probing signal is generated by an on-chip THz phase-locked loop (PLL) referenced to a voltage-controlled crystal oscillator (VCXO). By dynamically monitoring the intensity of the received signal through a carbonyl sulfide (OCS) gas sample, the probing signal is eventually aligned with the OCS transition line

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near 231.060983~GHz. Correspondingly, the VCXO output is also regulated through the PLL and outputs an ultra-stable frequency.

In [7] the OCS gas is sealed inside of a computerized numerical control (CNC) machined aluminum waveguide using pinch-off sealing (Fig.1b). Although the waveguide length is only a few centimeters, such packaging leads to a large volume of 246cc, high cost, and unscalable manufacturing. For the wide adoption of the CSMC technology in the commercial sectors (5G communication, navigation/positioning, networked sensing, etc.), it is critical to developing a fabrication process that can produce miniaturized gas cells in large quantities with high yield and low cost.

Silicon micromachining is an attractive option for the above goal, as it is commonplace for gases to be sealed inside of cavities during wafer bonding, such as in the fabrication of accelerometers. This enables an "all-silicon" clock assembly depicted in Fig. 1c, where the CMOS chip is directly stacked on top of the gas cell waveguide. The THz coupling mechanism is the same as that in [10], in which the wave is launched downward through the chip substrate and then into the openings of two vertical waveguide sections contacting the backside of the chip (see inset of Fig 1b) This introduces a unique need for a pair of waveguide bends to couple to the CMOS chip. Past work has demonstrated the fabrication of micromachined rectangular waveguides operating in either the 220-320GHz or 500-750GHz band [11-15].

This paper introduces a fabrication process of terahertz waveguides tailored toward miniaturized and lower-cost CSMCs, implementing step transition waveguide bends. We also introduce a mounting structure allowing the use of screws and alignment pins for improved ohmic contact and alignment during testing.

## II. Design and Simulation

A step transition is used to achieve broadband impedance matching in the waveguide bend. A depiction of the step transition and its parameters is shown in Fig 2a. The introduction of a step improves impedance matching by mimicking an ideal curved 90deg waveguide bend. The vertical segments of the waveguide have the same dimensions as that of a standard WR-3 (i.e. 220-320GHz) waveguide, with  $w=864\mu\text{m}$ , and  $h_v=432\mu\text{m}$ . The horizontal portion of the waveguide has a reduced height of  $h_h=300\mu\text{m}$ . The step depth  $d_s=150\mu\text{m}$  and height  $h_s=150\mu\text{m}$  are optimized in ANSYS High-Frequency Structure Simulator (HFSS).

The electric field distribution at the step transition is depicted in Fig.2b.

The simulated insertion loss  $S_{21}$  and return loss  $S_{11}$  for a 20mm-long waveguide are presented in Fig.2c and Fig.2d. The simulation assumes a gold coating with a horizontal surface thickness of 1um, sidewall thickness of 300nm, gold conductivity of  $4.1 \times 10^7 \text{S/m}$ , and surface roughness of 300nm RA. Using the step transition, the simulated  $S_{21} > -1.1\text{dB}$  and  $S_{11} < -25\text{dB}$  across the entire 220~320GHz range. Without the step transition, performance is significantly degraded, as the frequency response demonstrates considerable ripples and increased loss ( $S_{21} > -4.5\text{dB}$  and  $S_{11} < -5\text{dB}$ ).

## III. Fabrication Process

The micromachined waveguide is fabricated using two 6" silicon wafers with a thickness of 650um. The detailed process is shown in Fig.3. First, deep reactive ion etching (DRIE) is used to etch 300um-deep trenches into the front side of the handle wafer Fig.3b. The wafer is then etched from the backside 500um to form the waveguide port openings and the step transition (Fig.3c). By etching the ports and trenches on the same wafer, the critical alignment of waveguide trenches and ports occurs during the highly precise lithography phase instead of the more error-prone wafer bonding phase, which is what has been done in past works [12][15]. This DRIE sequence also etches the through-holes in the handle wafer, for mounting and alignment. These same holes are etched in the cap wafer.

For metallization, 1um of gold is sputtered onto the handle and cap wafers (Fig.3d). Sputter deposition is chosen for good step and sidewall coverage. Gold is sputtered onto both sides of the handle wafer to ensure

adequate sidewall and step coverage in the vertical segments of the waveguide. Finally, the two wafers are bonded together using thermo-compression bonding at 300 Celsius (Fig.3e).

#### IV. Results and Discussion

Waveguides with and without step transitions were fabricated for comparison. The handle wafer front- and backside are shown in Fig.4. A waveguide of 3.3~cm length occupies a volume of just  $\sim 0.29\text{cm}^3$ . This is impressive miniaturization, about 850x smaller than the current CNC machined gas cell ( $\sim 246\text{cm}^3$ ). Scanning electron microscope (SEM) images of the waveguide trench after backside DRIE is shown in Fig.5a. The waveguide trench after metallization is shown in Fig.5b. Fig.5c and Fig.5d depict the waveguide cross-section and sidewall. The bottom of the trench could be flatter with further fine-tuning of the DRIE process. Fig.6 and Fig.7 show port openings with and without step transitions, respectively. From Fig.6b it can be seen that there is residual silicon on the step, due to micro masking. Much of such residual silicon was then removed through subsequent sulfur hexafluoride isotropic etches.

The terahertz test setup is shown in Fig. 8. Custom adapters with built-in 90deg waveguide bends connect the fabricated silicon samples to a pair of Virginia Diode Inc. network analyzer frequency extenders. The adapters are 3D printed using stereolithography and electroplated with a nickel-copper alloy of 50um thickness. WR-4 waveguide bends are used in place of WR-3 due to manufacturing constraints. A pair of alignment pins and screws mount each adapter to a waveguide port on the wafer. The average loss of each adapter was 0.095dB/mm; this loss was de-embedded for all measurements.

The measured insertion loss is shown in Fig.9. The average loss of a waveguide with step transition across the 220~320GHz range is 0.31dB/mm. At the frequency of interest (231GHz), the loss of the waveguide with step transition is 0.27dB/mm. A waveguide without the step transition has more than twice the average loss (0.68dB/mm). From Fig.9, the frequency response of the waveguide with a step transition demonstrates clear improvement compared to that without a step transition; this is a result of the broadband impedance matching that is introduced by the step. Sources of loss include surface roughness, the flatness of the trench, and small residual silicon and debris such as that seen on the step transition. This loss can be mitigated by further fine-tuning of the DRIE process or by using a silicon-on-insulator wafer, where the buried oxide acts as an etch stop [11]. Fig. 10 shows the distribution of the average normalized loss of the 20 measured waveguides with step transitions. The figure shows a normal distribution, with the majority of waveguides having losses between 0.4 and 0.5dB/mm.

#### V. Conclusions and Future Work

In this work, we present a silicon micromachined waveguide operating in the 220~320GHz range. A simplified procedure to implement step transitions and mounting structures is described. This work demonstrates the feasibility of a low-cost, ultra-compact ( $\sim 0.29\text{cm}^3$ ) alternative to current CNC-based THz gas cells, and furthers the efforts toward a miniaturized all-silicon chip-scale molecular clock. The measured sample loss is already usable for the clock. Our future fabrication research includes further loss reduction through process tuning and hermetic sealing of carbonyl sulfide gas during wafer bonding.

This work is one of the stepping stones for integrating precision timing solutions directly into semiconductor platforms to greatly miniaturize electronics systems for CubeSats missions.

#### VI. Acknowledgment

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VII. Supplemental materials

A. Figures

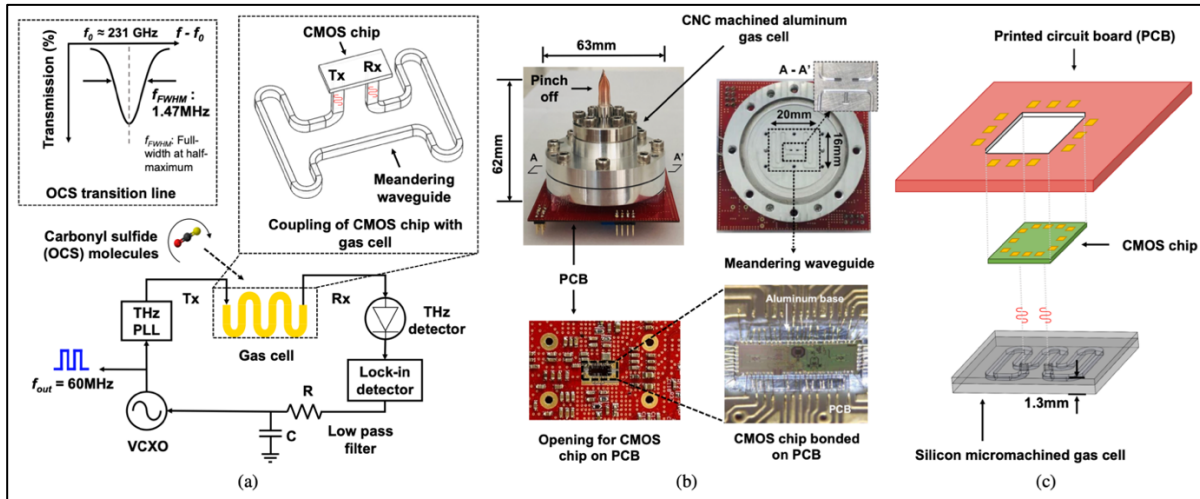
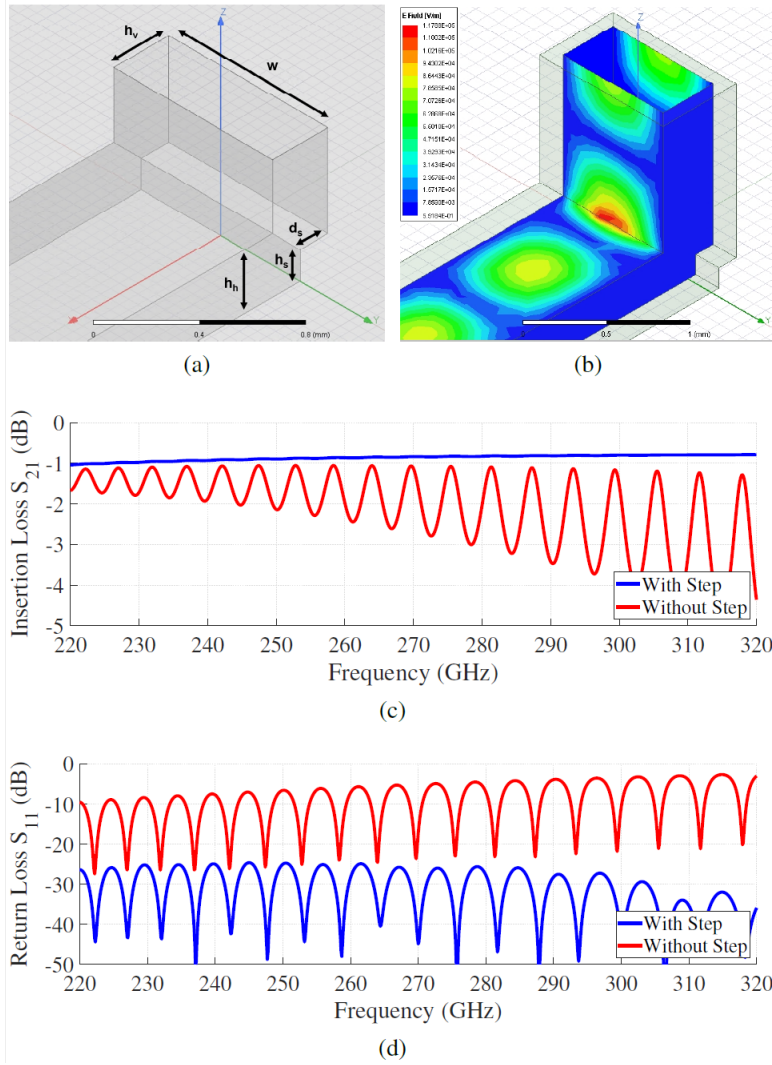
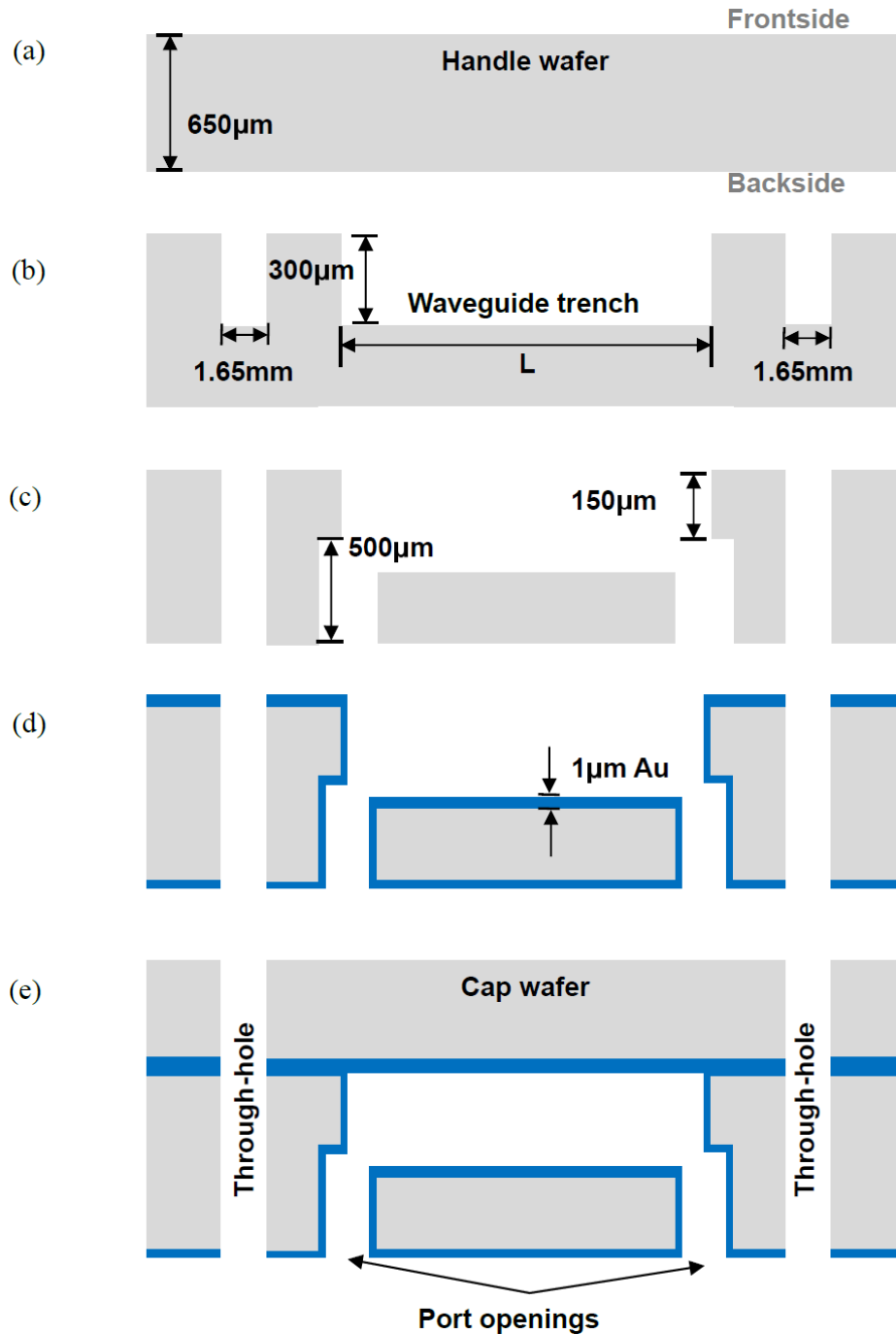


Fig. 1 (a) Simplified schematic of chip-scale molecular clock (CSMC). (b) The previous implementation of CNC machined aluminum gas cell using pinch-off sealing with a volume of 246cc. (c) Proposed 3D stack using silicon micromachined gas cell.



**Fig. 2 Simulation results. (a) Depiction of waveguide step transition and associated parameters. Final chosen parameters of  $w=864\mu\text{m}$ ,  $h_v=432\mu\text{m}$ ,  $h_n=300\mu\text{m}$ ,  $d_s=150\mu\text{m}$ ,  $h_s=150\mu\text{m}$ . If without step**

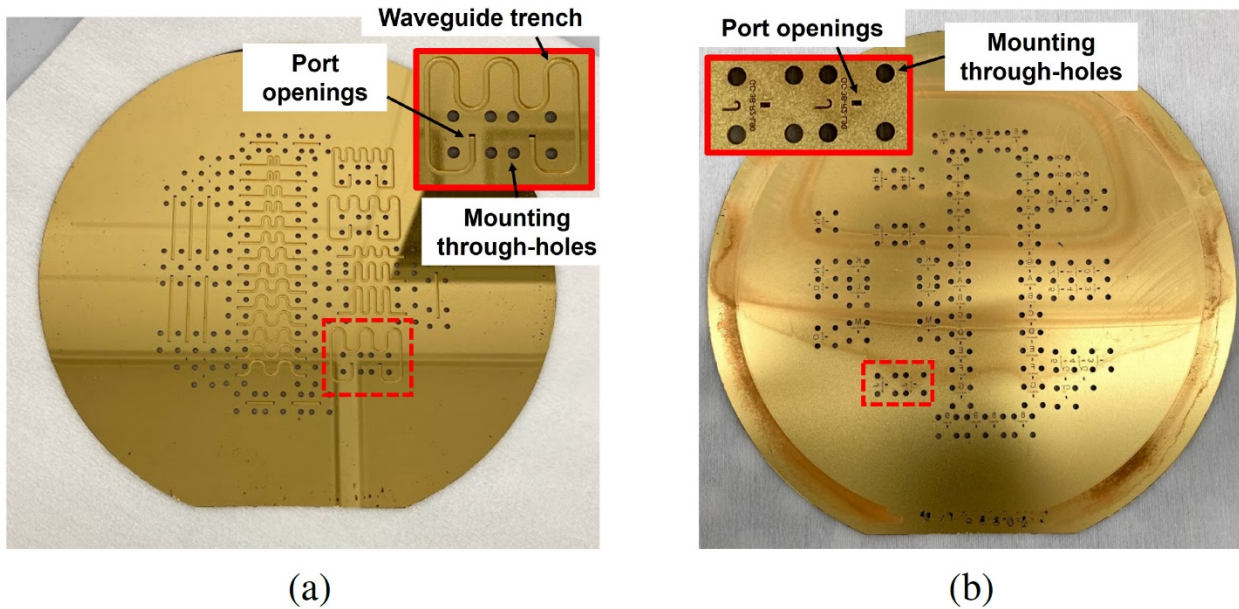
transition,  $h_s=0$ . (b) Electric field distribution at step transition. (c)  $S_{21}$  and (d)  $S_{11}$  simulation results of a 20mm-long micromachined waveguide.



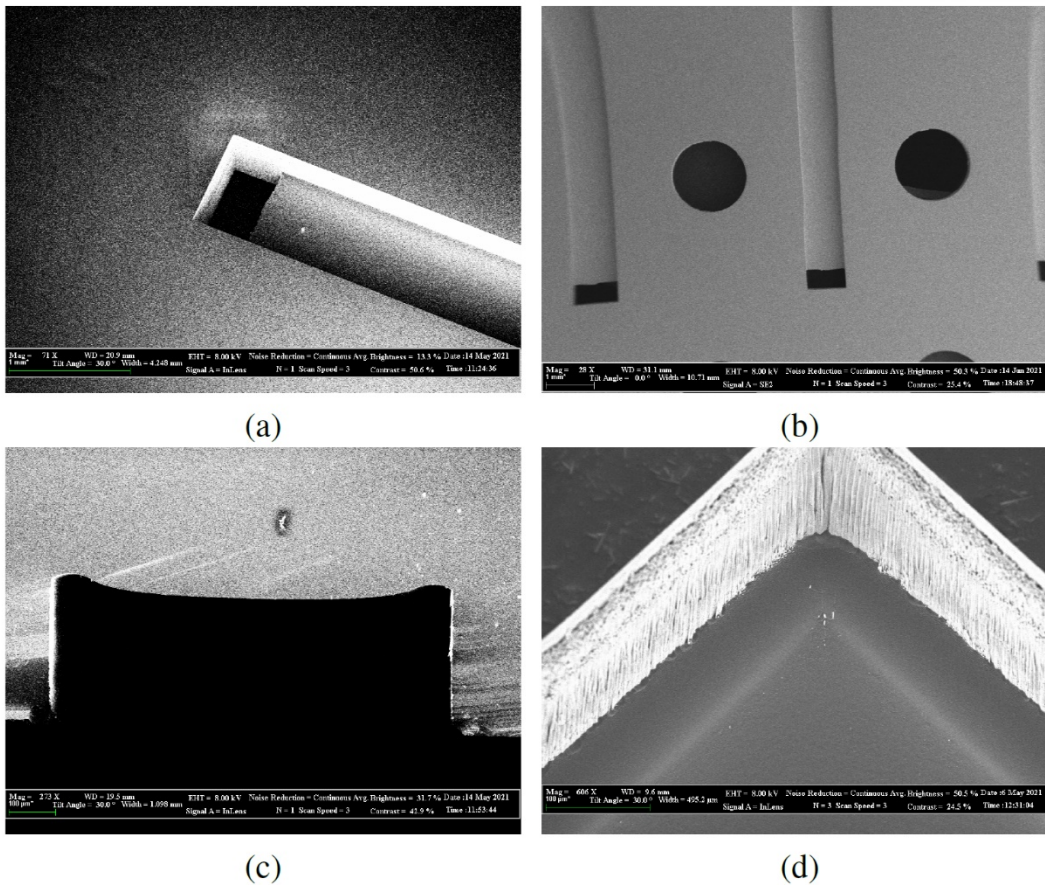
**Fig. 3** Fabrication process. (a) Bare handle wafer. (b) Frontside DRIE to form trenches and begin through-hole etch. (c) Backside DRIE from to form port openings and step transition bend, and



finish through-holes. (d) Metallization by sputtering 1um of gold on both sides of the handle wafer and on one side of cap wafer. (e) Thermo-compression bonding with cap wafer.

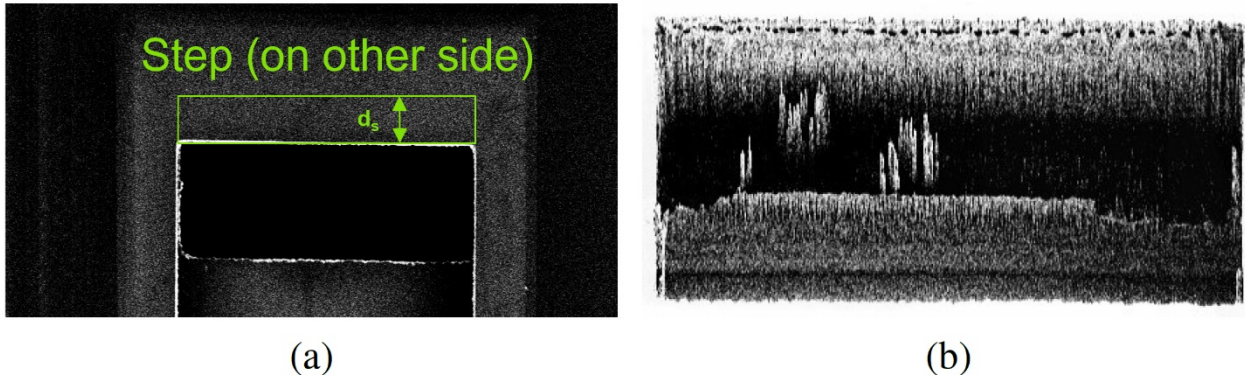


**Fig. 4 (a) Frontside of handle wafer with waveguide trenches. Inset: meandering waveguide with the shape of the proposed gas cell. (b) The backside of the handle wafer. Inset: close up of port openings and mounting holes.**

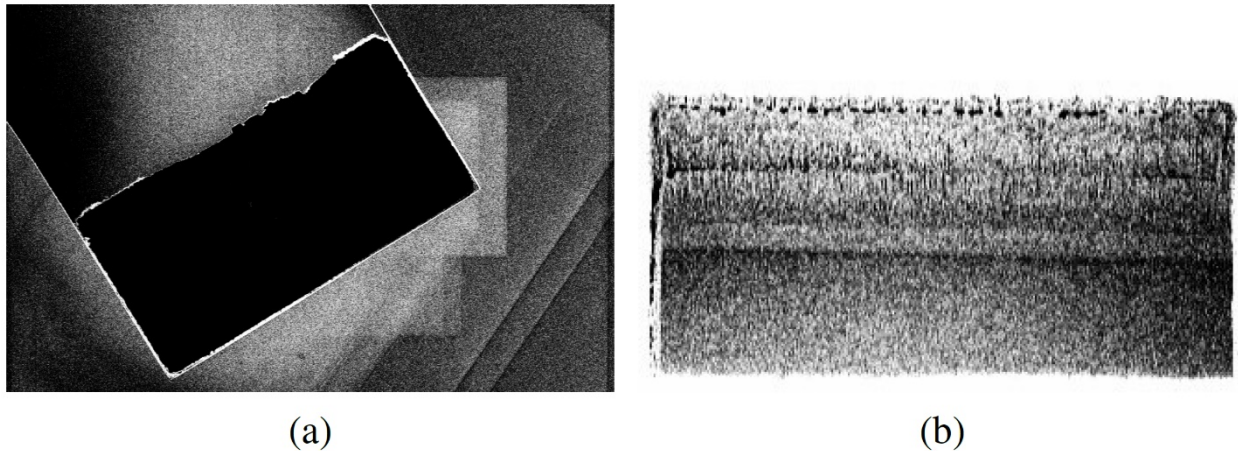


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**Fig. 5 (a) Waveguide after backside etch. (b) Waveguide after metallization. (c) Waveguide cross-section. (d) Sidewall profile.**

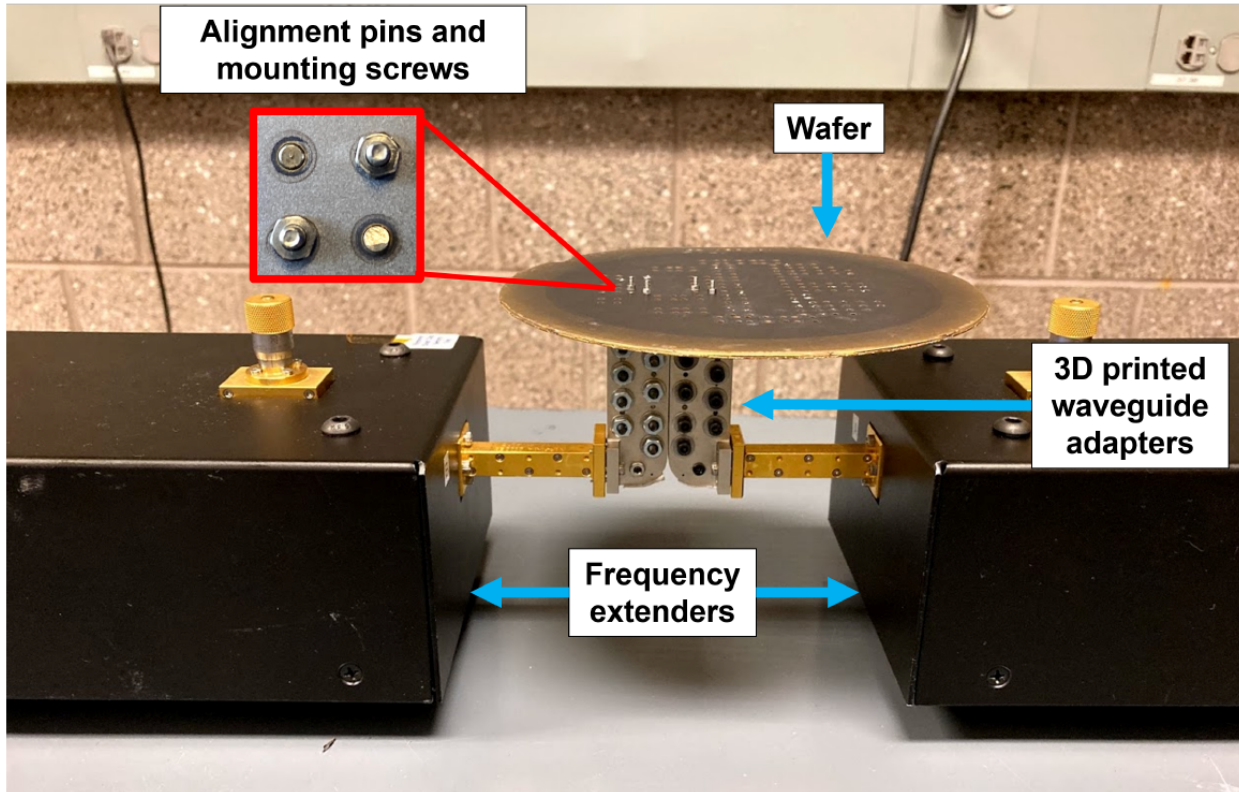


**Fig. 6 Port with step transition. (a) Frontside view. (b) Backside view showing step.**



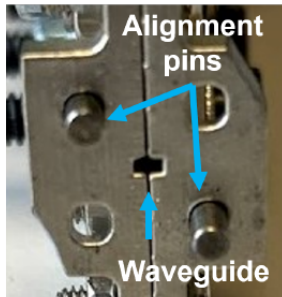
**Fig. 7 Port without step transition. (a) Frontside view. (b) Backside view.**



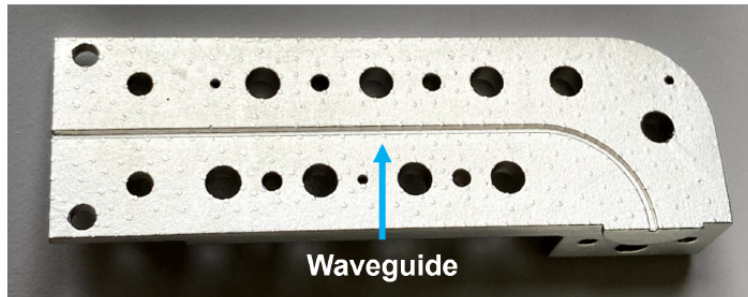


(a)

Adapter-to-wafer connection



Waveguide adapter cross section



(b)

Fig. 8 (a) Terahertz test setup. (b) Cross-sectional views of 3D printed waveguide adapters.

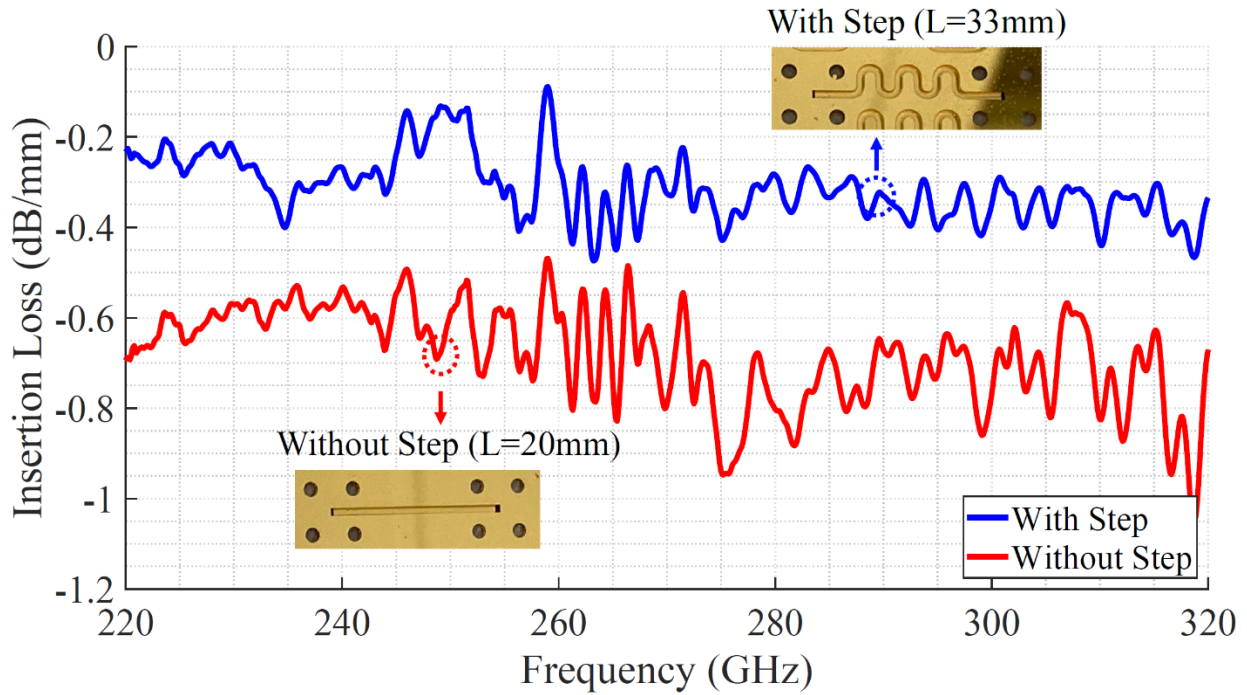


Fig. 9 Normalized insertion loss of waveguides with and without step transition.

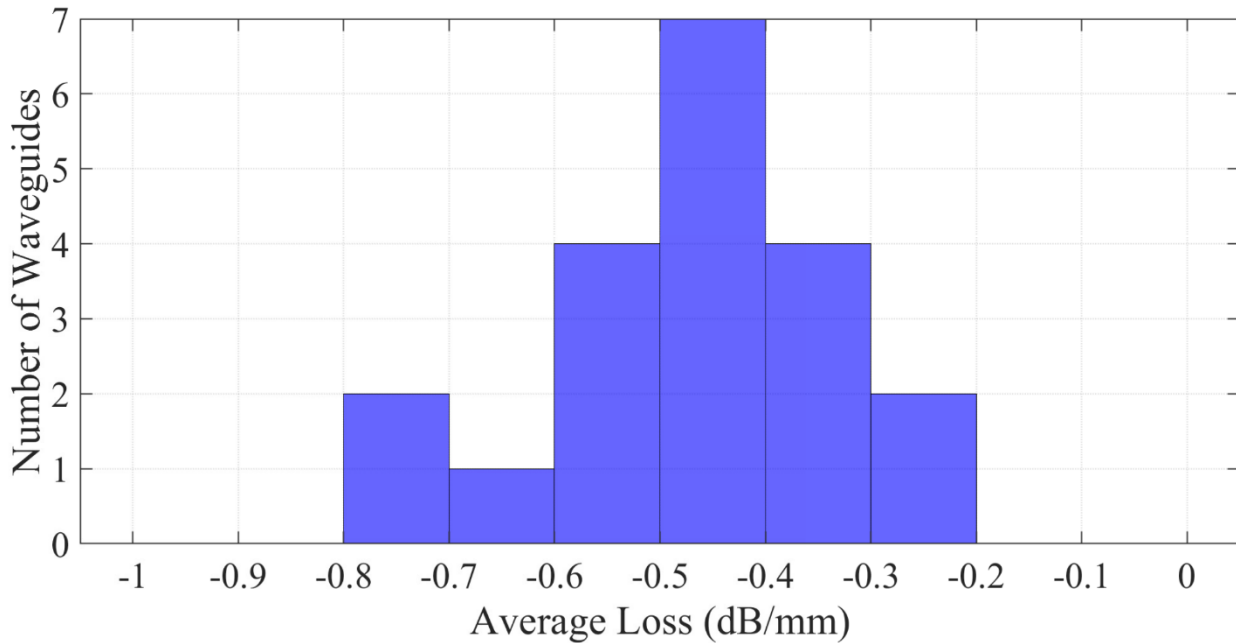


Fig. 10 Distribution of average normalized loss from 220~320 GHz for 20 fabricated waveguides with step transition.

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